LatticeSC™ SERDES Jitter

March 2008 Technical Note TN1084

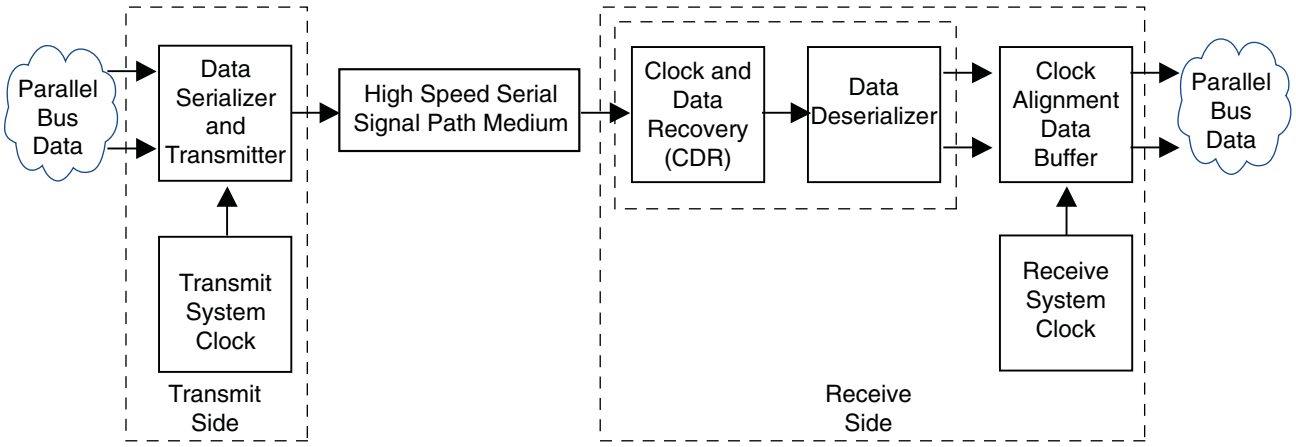
Abstract

This document addresses several topics related to SERDES jitter. First it provides a simple system view for high-speed serial data link (physical layer). It describes some basic jitter definitions and concepts needed to understand the roll of the SERDES elements in data link performance. A first-order model to aid in understanding the relationship between jitter and bit-error-rate is described. Critical SERDES jitter characterization parameters and measurement methods used by Lattice are defined and discussed. Some insights relating SERDES design and good jitter performance are also given.

Introduction

The benefits of using high-speed serial data links across PCBs and backplanes have become quite apparent to equipment and system developers. A growing number of ASICs and programmable ICs provide integrated SERDES interfaces. A typical high-speed serial data link using SERDES is shown in Figure 1.

Figure 1. Typical SERDES Application



Its purpose is to quickly and reliably transfer data from one physical location to another. The data, often in parallel bus form, is serialized to a single high-speed signal. This signal is transferred across a path medium that is ideally a high quality transmission line path to the new location. Included in the SERializer and DESerializer functions are embedded clock and clock-recovery circuitry, needed to create a high-speed serial data path.

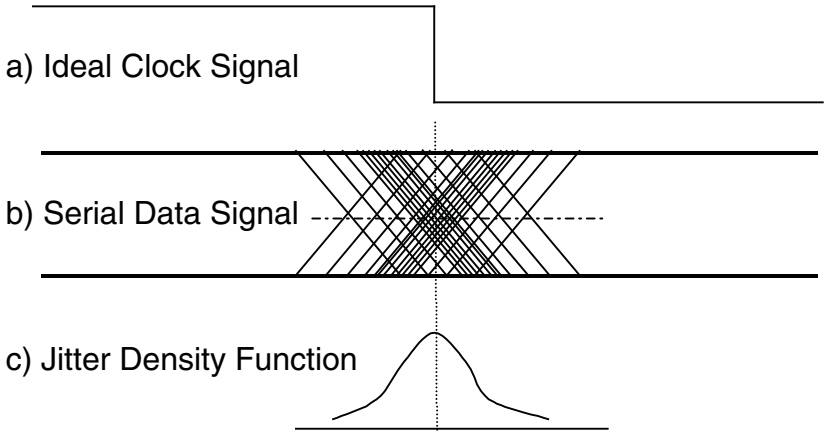
This path may be across a printed circuit board (PCB), a backplane with multiple PCBs, or through cabling connected to another equipment shelf. At the receive end of the path, a clock and data recovery circuit receives the signal and extracts a properly timed bit clock from the data flow. The data signal is then deserialized down to a lower speed parallel data interface. The parallel data is clock aligned to the local system clock. This is typically done with a dual port FIFO memory buffer.

This provides an effective solution to the difficult timing problems associated with transferring high bandwidth data across PCB, backplanes and even equipment frames. As this class of product evolves with increasing speed and density, so does the importance of understanding the jitter characteristics and limitations of the SERDES high-speed serial interfaces.

Jitter Fundamentals

In simple terms jitter can be defined as the timing error of a digital signal. Most digital signals have regular time intervals at which level transitions can occur. When a digital signal waveform is compared to the ideal periodic clock waveform, as shown in Figure 2, the effects of jitter can be seen.

Figure 2. Data Timing and the Jitter Function

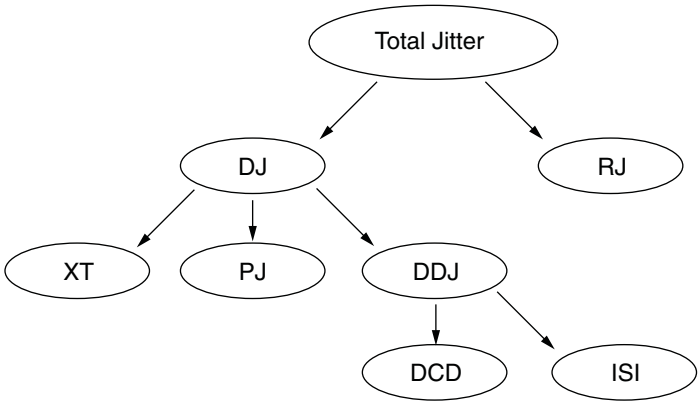


The signal level transition occurrences will vary as seen in Figure 2b, relative to the ideal clock edge (Figure 2a). This variation is often characterized with a histogram or jitter density function, as shown in Figure 2c. Slow timing variations, occurring at rates below 10 Hz are usually classified as wander. This is another term for low frequency jitter.

Types of Jitter

When dealing with jitter in a real system, it is often useful to classify the different types of jitter that can occur. This process often helps identify the root causes of problematic jitter. The composite, overall jitter associated with a data signal is called total jitter (TJ). TJ may be thought of as a composite function, composed of a number of different components resulting from various noise and signal sources within the system. These jitter components are general classified into two major categories: deterministic jitter (DJ) and random jitter (RJ). Most jitter components are not truly random in the statistical sense and are therefore classified as deterministic jitter (DJ). Figure 3 shows the hierarchy of these and some additional jitter component classifications.

Figure 3. Jitter Decomposition



Deterministic jitter components can be categorized into specific types, including periodic (PJ), inter-symbol interference (ISI), duty-cycle distortion (DCD), and cross talk (XT). Discussion of these jitter components and their probable sources with a system follows.

Periodic jitter is commonly introduced by clock and carrier signals within equipment. Typical asynchronous clocks of virtually any frequency can be offenders. Their frequency components couple into data signal paths and devices. To a large extent, differential data signal paths and interconnections receive these periodic components as common mode signals and reject these periodic components. The non-linear nature of semiconductor devices however allows some degree of signal mixing to occur, usually at the differential line receiver. The result is signal inter-modulation that translates to added data signal jitter.

Cross talk (XT) induced jitter on a signal is caused by cross coupling between data or control signals paths within a system. Again, it is the inter-modulation occurring in the semiconductor devices that translates the cross talk energy into signal jitter. Cross talk coupling can occur at any point along a signal path. Connector and package capacitance and mutual inductance between pins is a common source of this coupling. Significant levels of cross coupling can occur on PCBs where parallel data line segments have insufficient spacing or ground structures.

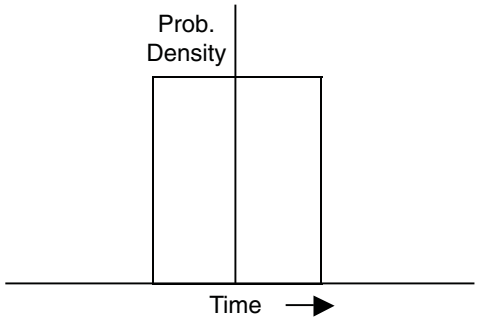
Inter-symbol interference (ISI) describes the situation where signal energy associated with one data bit in time is temporarily stored and then released at a later time, during another bit period. The result is data bits interfere with each other creating distortion and possibly corruption of the data bits. The effect of this signal degradation on digital signals can be seen as increased signal jitter. This situation most often occurs as a result of bandwidth limitations or other frequency dependent loss functions are introduced in signal connection paths, specifically at frequencies below the Nyquist limit of one-half the data clock frequency. Typical system transmission line interconnections create ISI from frequency dependent line losses. Another major source of this problem are transmission line impedance discontinuities. These occur at various points along the signal path, such as at connectors, PCB layer vias and device packages.

Duty cycle distortion (DCD) refers to unequal bit periods for 1 versus 0 data bits occurring in a data stream. This is often caused by high speed digital circuits that exhibit unequal rise and fall times or unequal delays associated with rising and falling edges. Differential digital signals can create this problem when dc voltage offsets occur between the P and the N signals. Very high-speed circuitry is sometimes designed to trigger on both the rising and falling clock edge. Clock signal duty cycle variations (from 50 percent) will give rise to data signal DCD in these circuits.

Jitter and Probabilities Functions

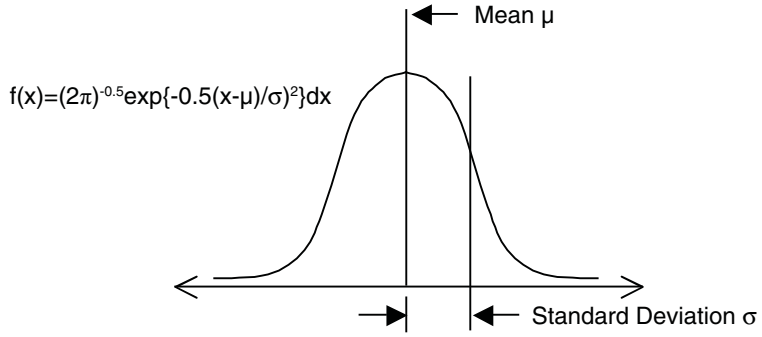
DJ includes most man-made signals and sources of energy that can inadvertently couple and translate into signal jitter. A common characteristic of all types of DJ is that they are amplitude bounded. This is a very important jitter characteristic that will be discussed later. An example of a deterministic jitter signal probability function is shown in Figure 4.

Figure 4. DJ Probability Function



Conversely, random jitter signal is assumed to have an unbounded amplitude probability function that extends out indefinitely. The generally accepted mathematical model for this is the Gaussian probability function, shown in Figure 5.

Figure 5. Gaussian Density Function



The bounded versus unbounded distinction is very important when considering jitter types. It will be discussed further when bit error rate and jitter measurement methods are described.

Combining Jitter Components

Since at least some jitter components are a result of random device processes, combining them in the correct mathematical sense requires the use of stochastic calculus. Assuming the jitter sources come from independent processes, which is often the case, their probability density functions may be added together using convolution techniques. In practice, jitter components and sources are often characterized much less rigorously, in terms of a maximum peak-to-peak value. When doing this it is a reasonable approximation to simply sum the numerical peak-to-peak values of the components. Note that assigning a peak-to-peak value to an unbounded random jitter signal is somewhat arbitrary and assumes the probability function tail is ignored above a certain level (for example 3-sigma or 6-sigma is often assumed to be an upper limit for the Gaussian function).

SERDES Jitter Parameters

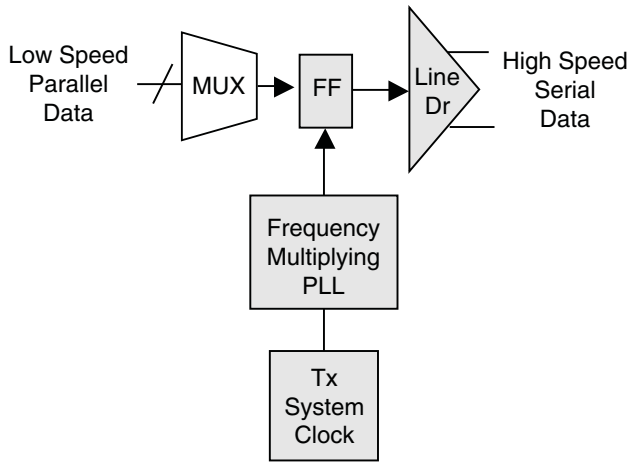
Overall jitter performance of a high-speed serial data link is affected by the SERDES elements at each end of the link. These are discussed in this section.

Transmitter Jitter Generation

The high-speed data line driver output should ideally generate a differential data signal which is timed to the transmit side system clock with no timing jitter. In reality the SERDES transmit and drive circuitry cannot avoid adding some amount of jitter to the data signal. Specifying a limit on the allowable amount of jitter at this point in a data link is an excellent way to insure overall Tx jitter performance. This parameter is typically specified for SERDES devices.

A typical SERDES transmitter/driver circuit block diagram is shown in Figure 6.

Figure 6. Typical SERDES Transmitter

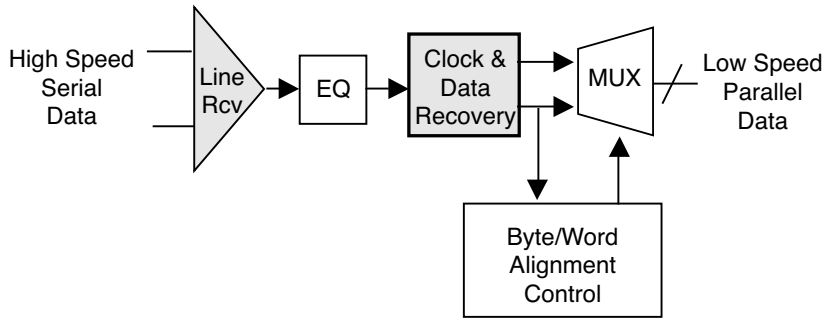


The Tx system clock is typically a sub-multiple of the serial data rate. This clock signal must be frequency multiplied to create the data rate clock signal that performs the data output timing function. Jitter present on the Tx system clock will transfer through the SERDES frequency multiplying phase locked loop and the data timing flip-flop, at some level. The result is added jitter at the line-driver circuit. The shaded boxes in Figure 6 have certain analog properties in play that will always add some degree of jitter to the overall jitter level of the output signal. The MUX element, on the other hand, is a true digital element and should add no jitter to the output signal.

Receiver Jitter Tolerance

The SERDES receiver's ability to tolerate some amount of jitter on the incoming signal, without the occurrence of bit detection errors, is critical. A typical SERDES receiver circuit block diagram is shown in Figure 7.

Figure 7. Typical SERDES Receiver



The inherently jitter sensitive circuit blocks that determine the overall jitter tolerance characteristics are shaded in Figure 7. The unshaded blocks are synchronous clock digital circuits which will cause no additional degradation of overall jitter tolerance, when driven by the freshly clock aligned data from the CDR.

The line receiver (buffer amplifier) must receive the incoming differential data signal with both timing and amplitude impairments. It functions to translate it to internal logic levels, with no amplitude impairments. Jitter on the incoming data signal will transfer right through this stage. A well-designed buffer amplifier will add only a very small amount of jitter to the data signal and it will reject common mode noise and extraneous signals.

In addition to transmit emphasis, the SC device provides three levels of programmable receive equalization (0,6db,and 12db) to further compensate for the effects of channel attenuation. Receive equalization is a function applied at the receiver which essentially counteracts signal degradation caused by PCB traces, vias, connectors and long transmission lines. Using one of the three EQ settings provides sufficient receiver equalization flexibility for most applications.

The clock and data recover circuit (CDR) has the difficult task of reconstructing the incoming data bit clock signal. It must do this with only the information contained in the edge timing of the incoming data transitions. This circuit is typically a very carefully designed phase-locked loop. In fact, it is typically the most critical element in setting the overall receiver jitter tolerance performance.

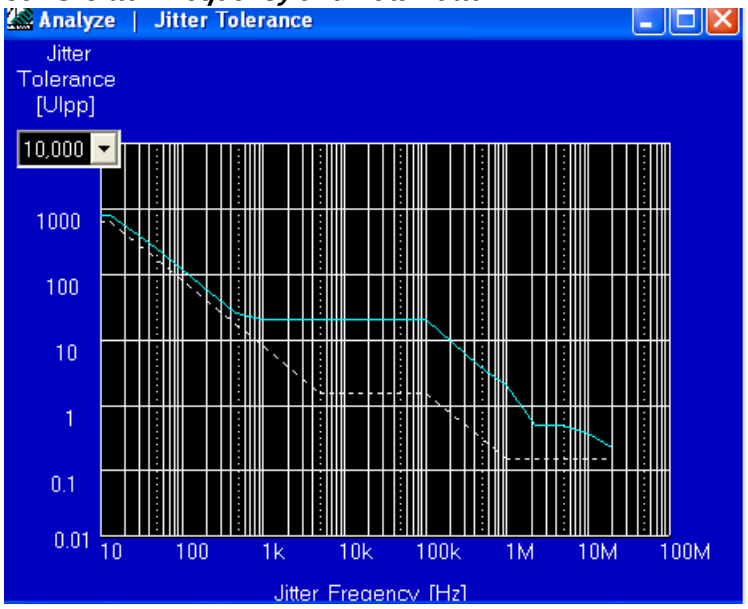
The CDR circuit's timing precision in recovering the clock has a strong dependence on the data transition density and on the data signal 1 or 0 state maximum run length. Data encoding schemes and data scrambling algorithms used with a SERDES data link can significantly increase the data pattern transition density and thereby improve Rx jitter tolerance.

These methods are included in virtually all standards that specify SERDES data links.

The frequency content of the incoming data jitter is another important variable. Generally jitter tolerance to low frequency types of jitter is much greater than for higher frequencies. The key parameter affecting this phenomenon is the closed loop bandwidth of the clock recovery PLL. Jitter with frequency content below the closed loop bandwidth will actually be cancelled out. This is because the recovered clock will track the shift in data timing caused by the low frequency jitter. This can allow the receiver bit detector to correctly read the data bit, even when its timing has been shifted more than one bit period, due to the jitter.

Figure 8 shows the jitter tolerance vs. jitter frequency and data pattern for a nominal LatticeSC device, running at 3.125GBbps. Sinusoidal jitter was injected onto the test pattern, at increasing levels until bit errors were observed. As was discussed in the previous section, the jitter tolerance level can be seen to be above one unit interval (UI) at jitter frequencies below approximately 2 MHz.

Figure 8. Jitter Tolerance vs. Jitter Frequency and Data Pattern



Power Supply Noise Tolerance

Power supply noise is a possible source of jitter. Digital switching elements and switching power supplies in a system typical create high levels of noise voltage on dc power supply lines. SERDES Tx and Rx circuits can potentially translate this noise voltage to jitter in the serial data link. Noise filtering at the PCB level is an effective way to control this problem. Vendors often provide specific power decoupling recommendations in the datasheet. Some SERDES product providers, such as Lattice, design critical circuits within the IC to have high supply voltage noise tolerance. This is done with internal filtering by using differential circuits with high common mode rejection characteristics.

Jitter and BER

A key measure of a digital system performance is bit error rate (BER) across data transfer links. System designers often consider BER to be the most important measure of overall system performance. Most system designers have a qualitative understanding of the relationship between BER and jitter. As jitter levels increase on any given data signal, a point is reached where bit errors will begin to occur at an objectionable rate. While this level of understanding is valuable, it provides little quantitative guidance to the hardware and system designers.

A precise mathematical relationship between BER and jitter within a system is quite complicated. A significant modeling effort would be needed just to identify and relate all the device and system variables that come into play. Given the statistical nature of data and the many jitter producing noise processes within a system, the stochastic calculus and other math tools needed to create a precise model are beyond the resources of most design projects.

Making some simplifying assumptions and approximations, a simple first-order model is proposed. This model builds on the Gaussian model assumption for R_J (used by most jitter measurement equipment makers), and additionally assumes a simple timing-error threshold model to represent the data detection/refresh process of the SERDES receiver. With these assumptions the mathematical relation between bit error rate and jitter is as follows:

$$BER = (R_S / D_J) \times \text{erf}^{-1} \{ (J_T - D_J) / R_S \}$$

Where BER = expected bit error rate
J_T = Rx device jitter tolerance range (peak to peak)
D_J = deterministic jitter (rms) amplitude at the Rx input
R_S = random jitter (1-sigma) amplitude at the Rx input
erf^{-1} is the standard inverse Gaussian error function

Model assumptions:

1. R_J follows the Gaussian function model
2. D_J PDF is bounded
3. Rx data-bit detection process deterministic (receiver generated R_J is small)
4. Most of the jitter spectral energy is above the CDR closed loop bandwidth

A closed form expression for the inverse Gaussian error function does not exist but it can be approximated with standard Gaussian probability tables such as provided in Table 1.

Table 1. BER Performance vs. Rx Input Jitter

BER	T_J Intercept
1.3E-3	6 σ
3.17E-5	8 σ
2.87E-7	10 σ
9.87E-9	12 σ
1.28E-12	14 σ
1E-12	14.1 σ
1E-14	15.3 σ
1E-16	16.4 σ
1E-18	17.5 σ
1E-20	18.5 σ

SERDES Device Jitter Measurement Methods

Accurate and repeatable jitter measurement of SERDES devices can be a challenging task. The rapid growth of device applications at multi-gigabit data rates combined with emerging new hardware interface standards has created a void for many engineering organizations. Significant resources are needed to fill this need and adequately support the latest SERDES device applications. Lattice has recognized this need and worked to establish effective laboratory test methods and characterization procedures. Some of the test methods used are described in this section.

Three types of multi-gigabit jitter measurement equipment are commonly available today. They include Agilent's Infinium DSO 81204A Real Time High-Speed Oscilloscope with jitter analysis capabilities, Agilent's 86100C Digital Communication Analyzer with jitter analysis capabilities (DCA-J) and Wavecrest's SIA3000 Time Interval Analyzer (TIA). These are high-speed oscilloscope and time interval measurement (TIM) instruments. All three products use the latest in high speed measurement technology and both provide DSP intensive data processing and extensive SW systems to perform very sophisticated statistical data analysis and total jitter decomposition. These programs can break down a total jitter measurement into RJ and DJ components and even further decomposition of DJ into its various subclasses.

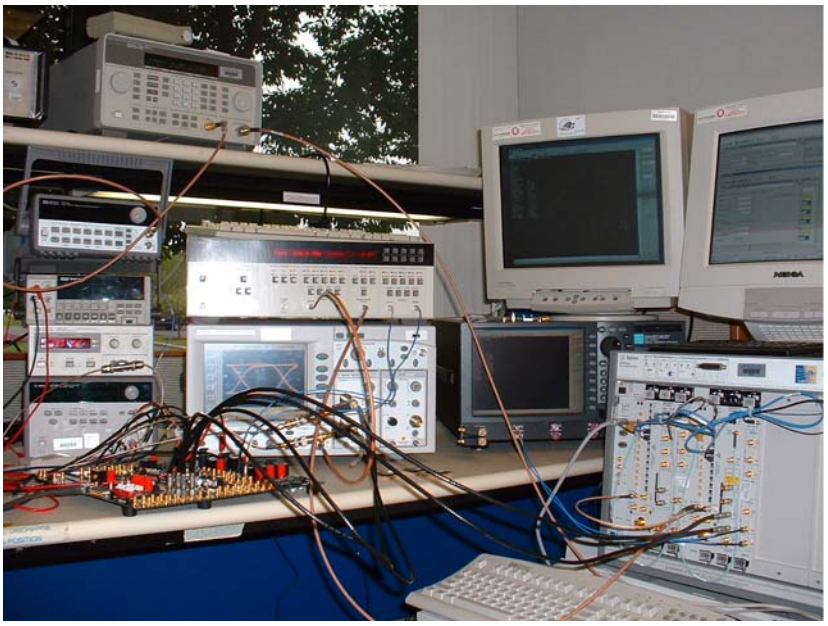
While accurate jitter measurement is a key element in jitter testing and device characterization, other test functions including BER testing and test signal generation are equally important parts of an overall test system. This is especially true for jitter tolerance characterization, which requires that a test data signal be generated with controllable, stable amounts of jitter added. The jitter signals needed include some of the jitter types discussed earlier. Recent jitter standards call for a composite jitter test signal made up of random jitter and two other types of deterministic jitter (ISI and periodic jitter types). The amount of each jitter component must be independently controllable.

Lattice has invested substantial time and effort in performing SerDes TX jitter measurements on the LatticeSC 3.7 GB/s SerDes using three specific pieces of compliant high-speed jitter test equipment currently available today. Tests on the Lattice SC were performed using an Agilent Infinium DSO 81204A 12GHz real time oscilloscope, an Agilent 86100-C DCA-J, and a Wavecrest SIA3000. The majority of our measurements were done using the Agilent 12 GHz real time scope. Two options are offered on this scope for separating DDJ and RJ/PJ. One is periodic mode, the other, arbitrary mode. Periodic mode was used for all SerDes measurements except for PRBS patterns larger than 2^7-1.

For DDJ extraction, Periodic mode uses the repeating data in a pattern to determine the average deviation for any given bit. Arbitrary mode uses a filter based on leading and lagging bits to determine the average deviation per bit.

For RJ/PJ separation, periodic mode takes data from the entire data run and makes computations based on the Average Power Spectral Density (APSD) in the frequency domain. Arbitrary mode keeps data in the time domain and either decimates the function for narrow RJ bandwidth mode or segments the function for wide RJ bandwidth mode.

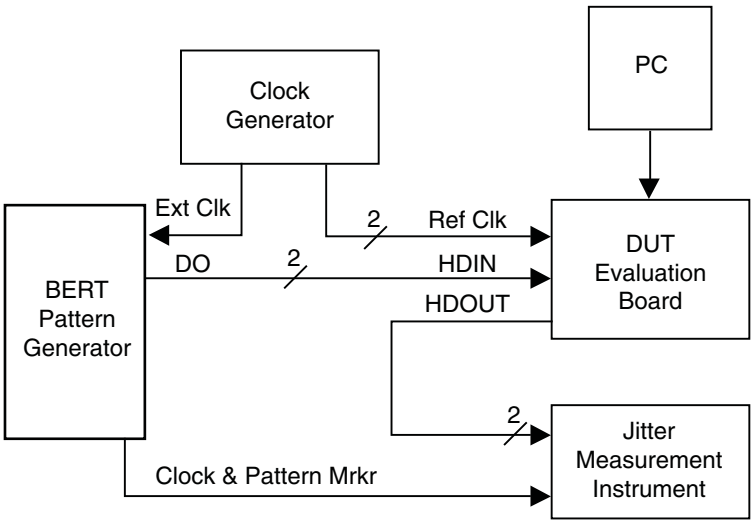
Figure 9. SERDES Jitter Test Station



Tx Jitter Generation

The standard test configuration used to measure LVDS & CML output jitter generation is shown in Figure 10.

Figure 10. Tx Jitter Generation Test Setup



The SERDES device under test (DUT) is placed in a socket on a custom evaluation/test board. This allows testing of multiple SERDES devices under identical test conditions such as those at various processing corners. Note: At high frequencies a socket will contribute slightly to the overall total jitter (TJ) due to insertion losses.

The evaluation board has a PC interface, which allows complete configuration and control of the all SERDES channels. The Tx channel under test is placed in parallel-side loop back configuration with the channel Rx section. The evaluation board provides 50-ohm SMA interfaces to the high speed SERDES clock and data I/O ports. A test data pattern from a bit-error-rate tester (BERT) is applied to Rx serial input. It passes directly through the SERDES to the Tx output port where it is applied to the jitter measurement instrument.

Delay matched 50 ohm cables are used to all differential I/O connections on the test equipment. Clock and pattern marker signals, needed for the jitter measurement are generated at the BERT. A variable frequency clock generator with low jitter is used to synchronize the BERT and DUT. It should be noted that measured output jitter will include the transferred jitter coming from the clock generator signal. For the clock generators used for SerDes measurements, typical cycle to cycle clock jitter at 156.25 MHz was 30-60 ps(pk-pk).

Given that the various pieces of equipment used to perform jitter measurements all use proprietary algorithms and different sampling methods to perform the calculations, results will vary slightly between measurements. For LatticeSC devices, typical TX total jitter (TJ) values observed at 3.125GB/s were .24UI. Best case and worst case results will differ from typical values.

In order to show the affects that a socket has on TX jitter at high frequencies, Lattice conducted tests using the same devices and evaluation board. Initially, the device was placed in a socket on the evaluation board and then the same device was soldered onto the same evaluation board. Measured results show that at data rates of 3.125GB/s, total jitter (TJ) had decreased by as much as .05UI when using the soldered device, see Table 2. For Table 3 below, typical TX jitter results are shown for the various pieces of equipment used for jitter measurements. Table 4 shows the comparison of the Agilent 12G real time scope periodic and arbitrary modes.

All Tx jitter measurements were taken at 25˚C using a PRBS 2^7-1 pattern.

Table 2. Typical Tx Results of Socket Vs. Soldered Devices (Same Device, Same Board)

Agilent 12G Real Time Scope-Periodic mode-Wide Band-CDR = Datarate/1667													
Channel Tested	Refclock	Speed	VDDOB	VDDRX /TX/P	VDDAX 25	TJ (p-p)ps	TJ (p-p)UI	RJ (1sig)	RJ	PJ (&-&)	PJ (rms)	DDJ (p-p)	ISI (p-p)
Soldered	312X10	3.125GB/s	1.5	1.2	2.5	81.61	0.25	5.18	72.52	2.02	1.52	13.32	12.17
Socketed	312X10	3.125GB/s	1.5	1.2	2.5	93.64	0.29	5.42	75.88	4.16	1.30	22.5	22.50

Table 3. Typical Tx Results of Soldered Devices (Jitter Analysis Equipment Comparison)

Agilent 12G Real Time Scope-Periodic mode-Wide/Narrow Band-CDR= Datarate/1667													
Ref-clock	Mode	Speed	VDDOB	VDDRX/ TX/P	VDDAX25	TJ(p-p) ps	TJ(p-p)UI	RJ(1sig) ps	RJ(UI)	PJ (&-&)	PJ (rms)	DDJ(p-p)	ISI (p-p)
312X10	Wide	3.125GB/s	1.5V	1.2V	2.5V	87.11	0.27	4.93	69.02	6.11	1.97	20.48	19.50
312X10	Narrow	3.125GB/s	1.5V	1.2V	2.5V	81.61	0.26	5.18	72.52	2.02	1.52	13.32	12.17
Agilent 86100C DCA-J													
Ref-clock	Mode	Speed	VDDOB	VDDRX/ TX/P	VDDAX25	TJ (p-p)ps	TJ(p-p)UI	RJ(1sig) ps	RJ(UI)	PJ (&-&)	PJ (rms)	DDJ(p-p)	ISI(p-p)
312X10	N/A	3.125GB/s	1.5V	1.2V	2.5V	97.30	0.30	5.97	83.58	8.20	2.74	16.40	15.30
Wavecrest SIA3000													
Ref-clock	Mode	Speed	VDDOB	VDDRX/ TX/P	VDDAX25	TJ (p-p)ps	TJ(p-p)UI	RJ(1sig) ps	RJ(UI)	PJ (p-p)	DDJ (p-p)	DJ(p-p)	
312X10	N/A	3.125GB/s	1.5V	1.2V	2.5V	104.90	0.33	4.94	69.16	4.90	37.48	42.39	

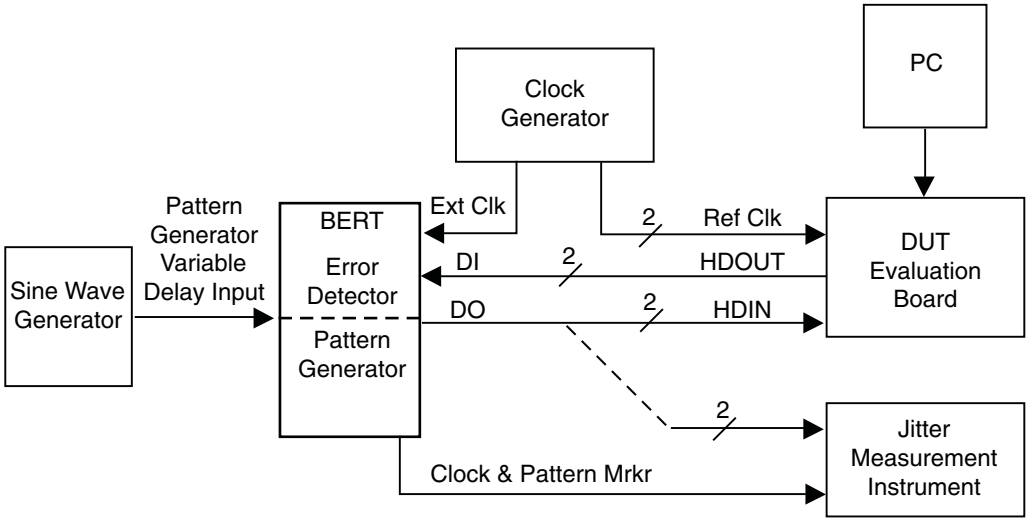
Table 4. Typical Tx Results measured with Agilent 12G Real Time Scope Comparing Arbitrary and Periodic Modes – Socketed Device

Periodic Mode													
Refclock	Mode	Speed	VDDOB	VDDRX/ TX/P	VDDAX25	TJ	TJ(UI)	RJ (1SIG)	RJ	PJ(&-&)	PJ(rms)	DDJ(p-p)	ISI(p-p)
156X20	Wide	3.125GB/s	1.5V	1.2V	2.5V	107.46	0.33	6.12	85.68	11.07	4.31	18.50	18.47
312X10	Wide	3.125GB/s	1.5V	1.2V	2.5V	87.11	0.27	4.93	69.02	6.11	1.97	20.48	19.50
156X20	Narrow	3.125GB/s	1.5V	1.2V	2.5V	105.76	0.33	5.97	83.58	12.05	4.37	18.34	18.17
312X10	Narrow	3.125GB/s	1.5V	1.2V	2.5V	86.97	0.27	5.17	72.38	4.65	1.66	21.02	20.07
Arbitrary Mode													
Refclock	Mode	Speed	VDDOB	VDDRX/ TX/P	VDDAX25	TJ	TJ(UI)	RJ (1SIG)	RJ	PJ(&-&)	PJ(rms)	DDJ(p-p)	ISI(p-p)
156X20	Wide	3.125GB/s	1.5V	1.2V	2.5V	73.28	0.23	1.52	21.28	39.81	6.90	20.10	20.10
312X10	Wide	3.125GB/s	1.5V	1.2V	2.5V	62.09	0.19	1.51	21.14	33.43	5.74	15.48	13.78
156X20	Narrow	3.125GB/s	1.5V	1.2V	2.5V	108.27	0.34	6.38	89.32	7.54	3.02	20.10	20.10
312X10	Narrow	3.125GB/s	1.5V	1.2V	2.5V	91.91	0.29	5.58	78.12	6.51	1.59	16.37	14.40

Rx Jitter Tolerance (Sinusoidal)

The test configuration previously described is modified for CML Rx sinusoidal jitter tolerance measurement. The new test configuration is shown in Figure 11.

Figure 11. Rx Jitter Tolerance Test Setup (Basic)



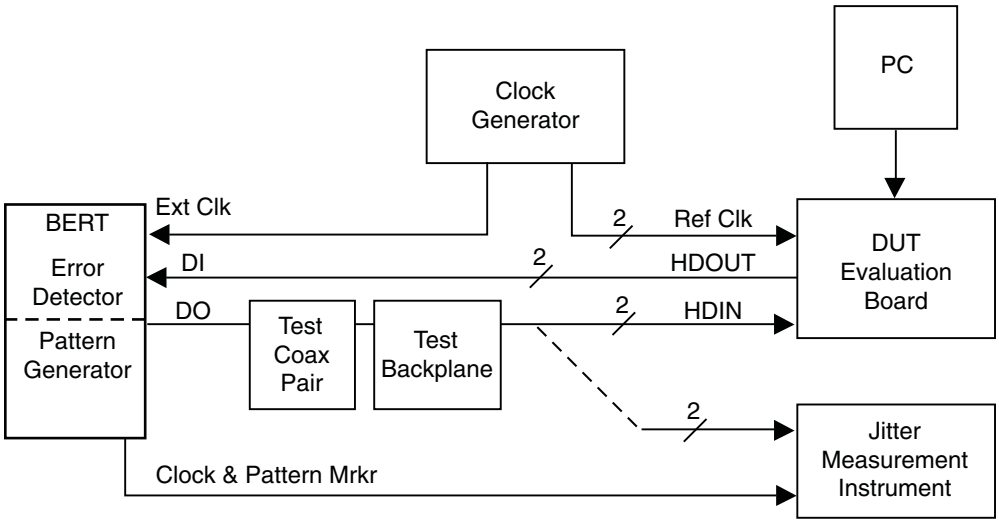
The variable delay input feature of the BERT pattern generator provides a means of adding a controlled level of jitter to the data pattern output. The amplitude of the sine wave generator signal applied to the variable delay input determines the jitter level on the data output of the BERT. This signal is applied to the DUT Rx serial input. The SERDES channel under test is configured in the loop back mode as was described in the prior section. The DUT Tx output is connected to the data input of the Error detector section of the BERT. With these connections, the BERT can now compare the outgoing and incoming data patterns and accurately measure the bit-error-rate (BER) of the DUT SERDES channel.

Testing involves varying the jitter level of the pattern generator output, which is applied to the Rx input, while monitoring the BER. The jitter level is slowly increased until the BER test criteria (usually BER=1E-12) is reached. The BER pattern generator output signal is then connected to the jitter measurement instrument. The level of jitter measured is the jitter tolerance of the DUT SERDES Rx input.

Rx Jitter Tolerance (ISI)

The test configuration is modified for LVDS Rx DDJ jitter tolerance measurement. The new test configuration is shown in Figure 12.

Figure 12. Rx Jitter Tolerance Test Setup (ISI)



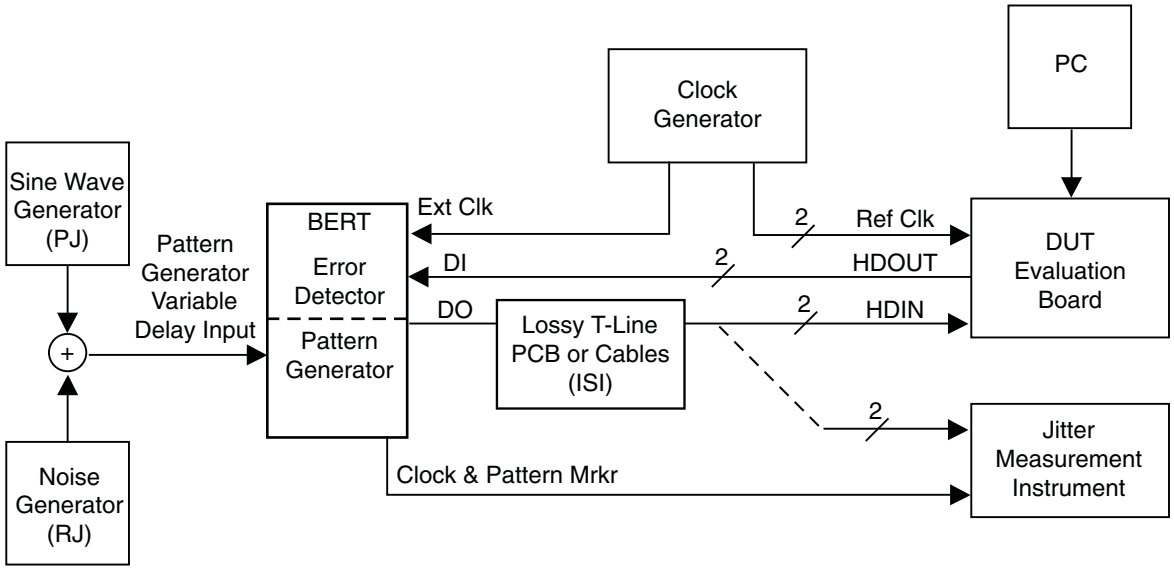
The test signal coming from the BERT pattern generator is passed through some long test coax cables and a test backplane. The frequency dependent loss of these elements adds inter-symbol interference (ISI) jitter to the test signal. Different length cables and PCB line segments are inserted to vary the amount of jitter on the data test signal applied to the SERDES inputs. The SERDES channel under test is configured in the loop back mode as was described in the prior section. The DUT Tx output is connected to the data input of the Error detector section of the BERT. With these connections, the BERT can now compare the outgoing and incoming data patterns and accurately measure the bit-error-rate (BER) of the DUT SERDES channel.

Testing involves varying the jitter level of the pattern generator output, which is applied to the Rx input, while monitoring the BER. The jitter level is increased until the BER test criteria (usually BER=1E-12) is reached. The BER pattern generator output signal is then connected to the jitter measurement instrument. The level of jitter measured is the jitter tolerance of the DUT SERDES Rx input.

Rx Jitter Tolerance (Compound Jitter)

The test setup of Figure 13 is modified to allow testing with a compound mix of jitter types, as might be found in a typical system application. The compound jitter setup is shown in Figure 15.

Figure 13. Rx Jitter Tolerance Test Setup (compound jitter)



The sine wave jitter signal source is combined with a random noise source before being applied to the BERT. This produces a jitter signal with two components (RJ and PJ) at the pattern generator output. A lossy transmission line (matched pair) is inserted in the data signal connection to the DUT. This acts as a frequency bandwidth-limiting filter, producing a third type of jitter called intersymbol interference (ISI). The three types of jitter may be independently controlled to accommodate different application scenarios or different industry standard test conditions.

The same test procedure described in the previous section is followed. Normally two of the jitter component levels are set to designated levels and the third is gradually increased until the BER criteria are reached. Table 5 below shows typical Rx jitter tolerance results with 6db of equalization applied. As described above,RJ and PJ are applied to BERT delay control. This jittered signal is then generated from the BERT through 40 inches of FR-4 backplane (ISI) before being sent to the DUT receiver. Sinusoidal (PJ) is then increased until the BERT error detector fails. The pattern used for this test is CJPAT.

Table 5. Typical RX jitter Tolerance for Lattice SC Device

Data rate	EQ	TJ(UI) p-p	DDJ(UI)p-p	PJ(UI)p-p	DJ(UI)p-p	RJ(1sig)	RJ(UI)p-p
3.125GB/s	6db	0.85	0.43	0.20	0.63	0.02	0.26

Test Methodology

SERDES device jitter characterization is a very important issue to system designers. The success and robustness of new systems and equipment depends on the jitter performance, as has been discussed in the preceding sections. The complex nature of high-speed signal interfaces makes modeling and simulation efforts useful but limited, in assuring desired device performance. Testing is the most important means of assuring device quality and performance. The jitter testing methods described can be very arduous and time consuming. An efficient yet comprehensive test methodology is needed to insure high quality product with low customer cost.

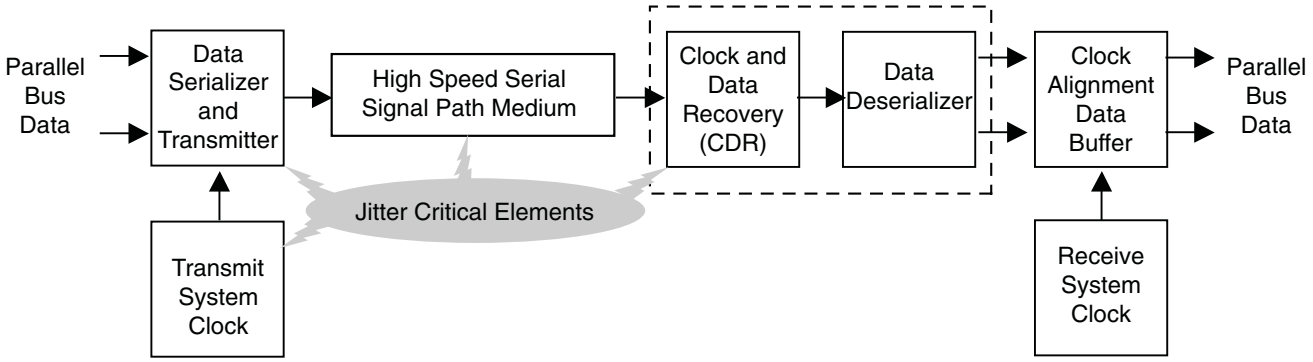
At Lattice, the jitter characterization testing described above is done on a sample basis, across all products containing high-speed SERDES interfaces. To make this testing as efficient as possible, it is conducted over a number of product and environmentally extreme conditions. For example, intentionally processed devices representing worst-case manufacturing conditions are often included in our device testing. In addition, temperature and supply

voltage levels are moved to the specified limits of the product. As new product versions emerge, regression jitter tests are routinely performed.

Conclusion

The SERDES application diagram described earlier is redrawn in Figure 14, showing critical elements, where jitter is normally generated and accumulated.

Figure 14. Jitter Critical Physical Link Elements



Many of the jitter critical elements are integral circuits of SERDES interface subsystems. These parts were discussed in detail. The importance of the jitter performance of these parts was emphasized. This performance can only be achieved if good chip design practices are followed. Also of importance is laboratory characterization and verification, at both the development and production levels. Basic jitter test methods used by Lattice to characterize our SERDES products were described. Worst-case jitter test result data for a typical application is shared for our products. Selection of IC products with known good jitter characteristics is crucial in most new applications. System designers who understand the roll of the SERDES elements in their system and how they can affect overall performance will be able to provide the reliable and robust performance that their customers demand.

Jitter performance is highly system dependent. Lattice offers device evaluation boards with high-speed SMA connector interfaces. These test boards are available to customers so they may evaluate product performance in their specific application environments. In addition extracted HSPICE buffer models are available to allow system simulation of the critical high-speed serial system interfaces in an application. For detailed jitter characterization data, please contact your local Lattice sales representative.

Revision History

Date	Version	Change Summary
–	–	Previous Lattice releases.
April 2007	01.0	Typographical corrections.
March 2008	01.1	Corrected Typical SERDES Receiver diagram and fixed jitter frequency value on page 7.
March 2008	01.2	Moved Jitter Tolerance vs. Jitter Frequency diagram closer to related text and modified text description of the diagram.