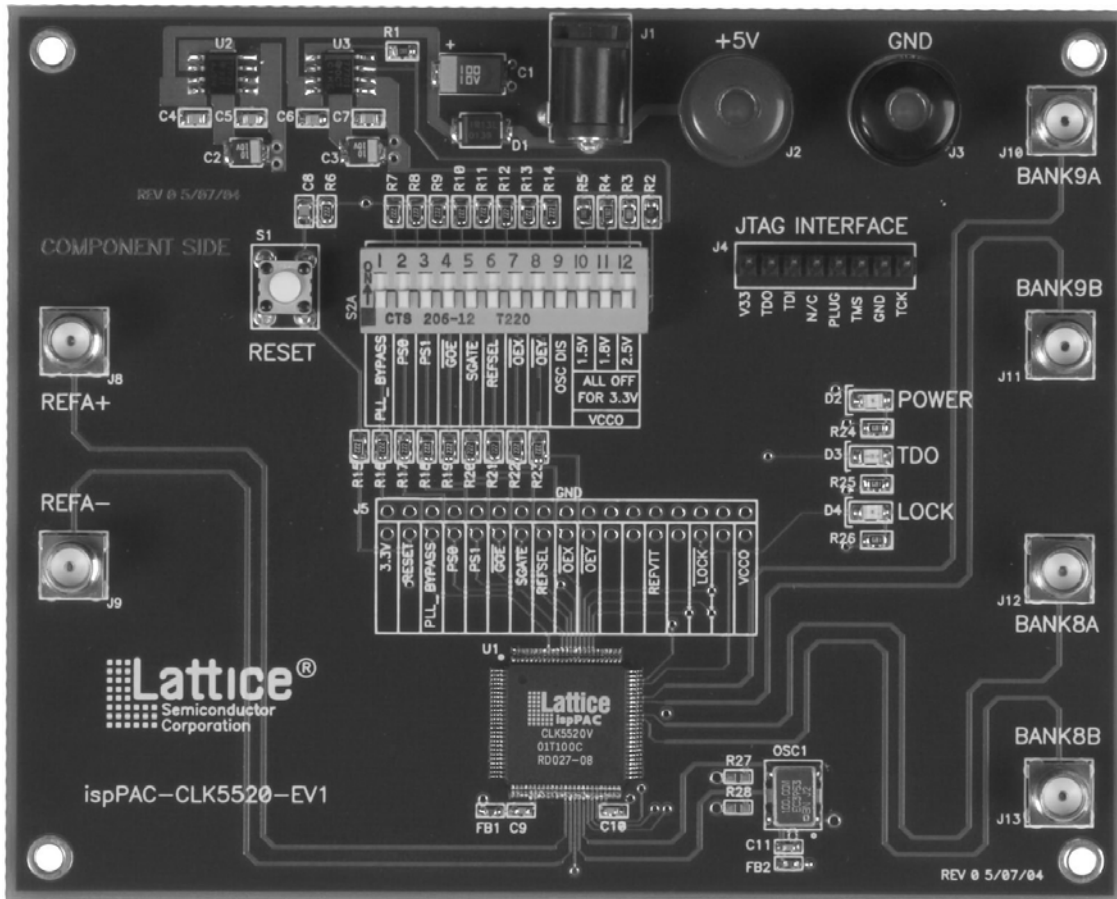# ispClock5520 Evaluation Board: ispPAC-CLK5520-EV1

Introduction

The Lattice Semiconductor ispClock™5520 In-System-Programmable Analog Circuit allows designers to implement clock distribution networks supporting multiple, synchronized output frequencies using a single integrated circuit.

By integrating a Phase-Locked Loop (PLL) along with multiple output dividers, the ispClock5520 can derive up to five separate output frequencies from a single input reference frequency. To facilitate the implementation of wide-fanout clock trees, the ispClock5520 provides up to 20 single-ended outputs or 10 differential outputs, organized as ten banks of two. Each output bank may be independently programmed to support different logic standards and operating options. Additionally, each single-ended output or differential output may be skew-adjusted to compensate for the effects of propagation delay along the PCB traces used in the distribution network. All configuration data is stored internally in E^{2}CMOS® non-volatile memory. Programming a configuration is accomplished through an industry-standard JTAG IEEE 1149.1 interface.

Figure 1. ispPAC-CLK5520-EV1 Evaluation Board

ispPAC-CLK5520-EV1 Evaluation Board

The ispPAC-CLK5520-EV1 evaluation board (Figure 1) allows the designer to quickly configure and evaluate the ispClock5520 on a fully assembled printed-circuit board. The four-layer board supports a 100-pin TQFP package, a header for user I/O and a JTAG programming cable connector. SMA connectors are installed to provide high-signal

Lattice Semiconductor

ispClock5520 Evaluation Board:
ispPAC-CLK5520-EV1

integrity access to selected high-speed I/O signals. JTAG programming signals can be generated by using an isp-DOWNLOAD® programming cable connected between the evaluation board and a PC's parallel (printer) port. All user-programmable features of the ispPAC-CLK5520 can be easily configured using Lattice Semiconductor's PAC-Designer® software.

Programming Interface

Lattice Semiconductor's ispDOWNLOAD cable can be used to program the ispClock5520 which is provided on the evaluation board. This cable plugs into a PC-compatible's parallel port connector, and includes active buffer circuitry inside its DB-25 connector housing. The other end of the ispDOWNLOAD cable terminates in an 8-pin 0.100" pitch header connector which plugs directly into a mating connector provided on the ispPAC-CLK5520-EV1 evaluation board.

Power Supply Considerations

The ispClock5520 operates with analog and digital core power supplies of 3.3V, while each output driver has a dedicated power supply pin which may be driven with supply voltage of 1.5V, 1.8V, 2.5V or 3.3V, depending on the logic standard which it has been configured to drive.

To simplify evaluation work, the ispPAC-CLK5520-EV1 board was designed to operate from a single 4.5V-5.5V power supply, which may be brought in through either a pair of banana plugs (J2 and J3), or a standard 5mm power plug (J1 - center tip positive). The evaluation board provides two linear regulators to provide the appropriate operating voltages for the ispClock5520. One of these regulators provides a fixed 3.3V for the analog and core functions, while the other regulator is dipswitch-programmable to provide 1.5V, 1.8V, 2.5V and 3.3V to power the BANK8 and BANK9 output drivers.

Input/Output Connections

Connectors are provided for key functions and test points on this evaluation board, as shown In Figure 2. Power may be supplied in one of two ways; either through two color coded (RED = +, BLACK = -) banana jacks in the upper right corner of the board or through a 5mm (center pin +) DC power connector (J1), The JTAG programming cable is connected to a keyed header (J4) in the upper right corner of the board.

Access to a subset of the ispClock5520's I/O pins is available at J5, which is a 2x17 row of pads to which one may attach test probes or a ribbon-cable connector. At this point most of the device's non-RF control pins (except those required for the JTAG programming interface) are accessible.

SMA connectors are provided along the left and right edges of the board to support access to key high-speed I/O pins. Pairs of connectors are provided for the BANK8 and BANK9 outputs (J10-J13). Additional pairs of connectors are provided for REFA(+/-) clock reference inputs (J8, J9). On this evaluation board design the REFB(+/-) clock inputs are dedicated to supporting an on-board crystal oscillator. Because this board was designed to maintain high levels of signal integrity at the edge rates at which the ispClock5520 operates, it is strongly suggested that the user do not attempt to access any of the device's high-speed I/O except through the provided SMA connectors and supporting impedance-controlled printed-circuit traces.

Figure 2. I/O Connections, Controls and Indicators
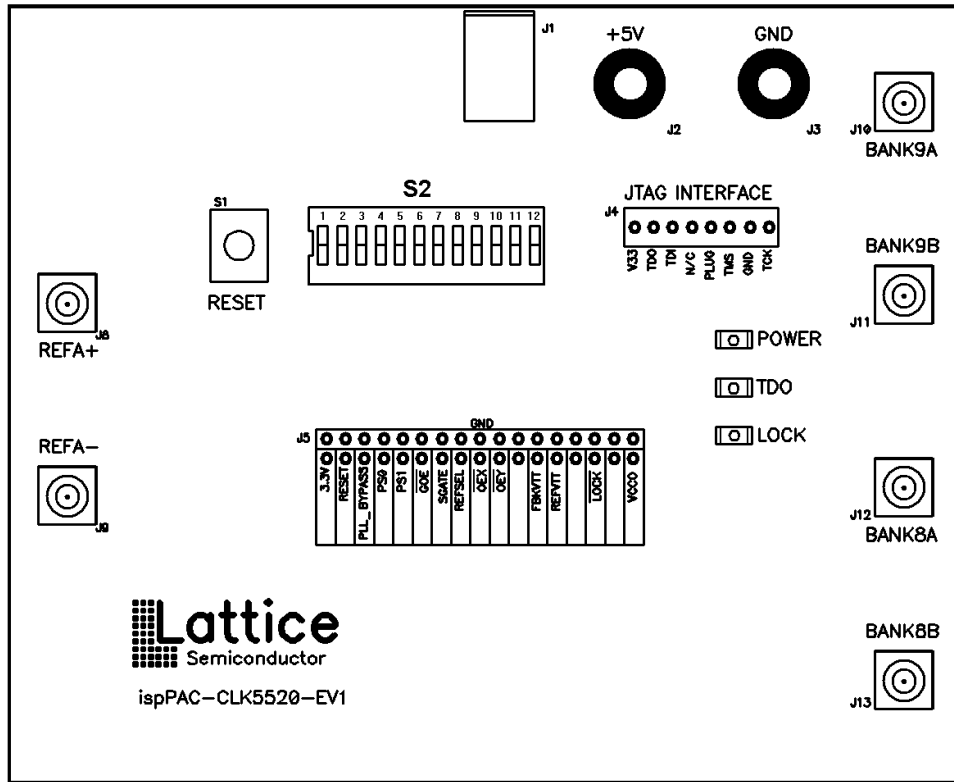
Controls and Indicators

A 12-position dipswitch (S2) is provided on the evaluation board (Figure 2) for the purpose of setting device inputs and programming the VCCO power supply for the BANK8 and BANK9 outputs. The following table shows the options controlled by each switch:

Table 1. User Configuration Functions

Position	Function (when ON)
1	PLL_BYPASS
2	PS0
3	PS1
4	$\overline{\text{GOE}}$
5	SGATE
6	REFSEL
7	$\overline{\text{OEX}}$
8	$\overline{\text{OEY}}$
9	OSC DIS
10	BANK8 and BANK9 VCCO Programming
11	
12	

Each of the switch positions used to control logic inputs (positions 1-8) pulls its respective control signal HIGH when it is turned on. Each of these switch outputs is connected to the device through a 1KΩ resistor. This feature allows external CMOS logic control signals applied to the J5 header connector to over-ride the on-board switch settlings.

Switch position 9 (OSC DIS) is used to control the evaluation board's on-board clock oscillator. When this switch is set to the OFF position the on-board 100MHz oscillator is active and when it is the ON position it is disabled. Disabling the on-board oscillator is desirable when an external clock source is used as an input reference signal because doing so reduces the jitter measured at the board's output. Note that if the on-board source is selected (REFSEL switch = ON) the on-board clock must not be disabled.

Switch positions 10-12 are used to program the VCCO supply for output banks 8 and 9. When all of these switches are OFF, the default supply VCCO supply is 3.3V. The following table shows the switch configurations needed to develop standard supply voltages:

Table 2. VCCO Programming Switch (S2) Configurations

S2 Switch Position			
10	**11**	**12**	**VCCO**
OFF	OFF	OFF	3.3V
ON	OFF	OFF	1.5V
OFF	ON	OFF	1.8V
OFF	OFF	ON	2.5V

A reset switch (S1) is provided on the evaluation board which pulls the RESET input pin HIGH when it is depressed, re-initializing the ispClock5520. After changing profiles or reprogramming the ispClock5520 it is necessary to reset the device to obtain a stable clock output.

Several LEDs are also provided on the evaluation board to indicate proper function and as aids to debugging. LED D2 (red) indicates that the on-board 3.3V supply is powered up. LED D3 (yellow) is connected to the ispClock5520's TDO line, and will briefly flash when downloading, indicating that download data has made it to the device. Finally, when LED D4 (green) is lit, this indicates that the ispClock5520's PLL is in a 'locked' state.

Schematics

The following three figures comprise the schematics for the ispPAC-CLK5520-EV1 evaluation board. Figure 3 shows the on-board power-conditioning circuitry, Figure 4 shows the high-speed interconnects and on-board oscillator circuitry, while Figure 5 shows all the logic control signals and indicators.

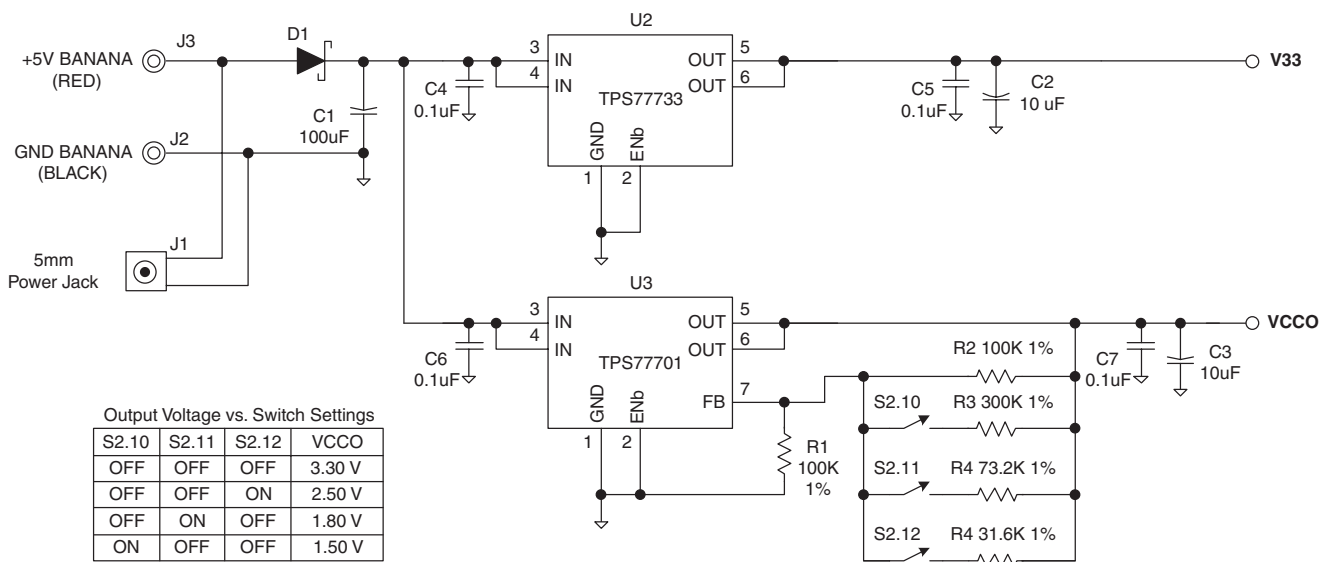*Figure 3. On-Board Power Supplies*

S2.10	S2.11	S2.12	VCCO
OFF	OFF	OFF	3.30 V
OFF	OFF	ON	2.50 V
OFF	ON	OFF	1.80 V
ON	OFF	OFF	1.50 V

Figure 4. Oscillator and High-Speed I/O

Notes:
1. If OSC1 is LVCMOS type, omit R27,R28
   If OSC1 is DPECL type, for external termination install R27,R28
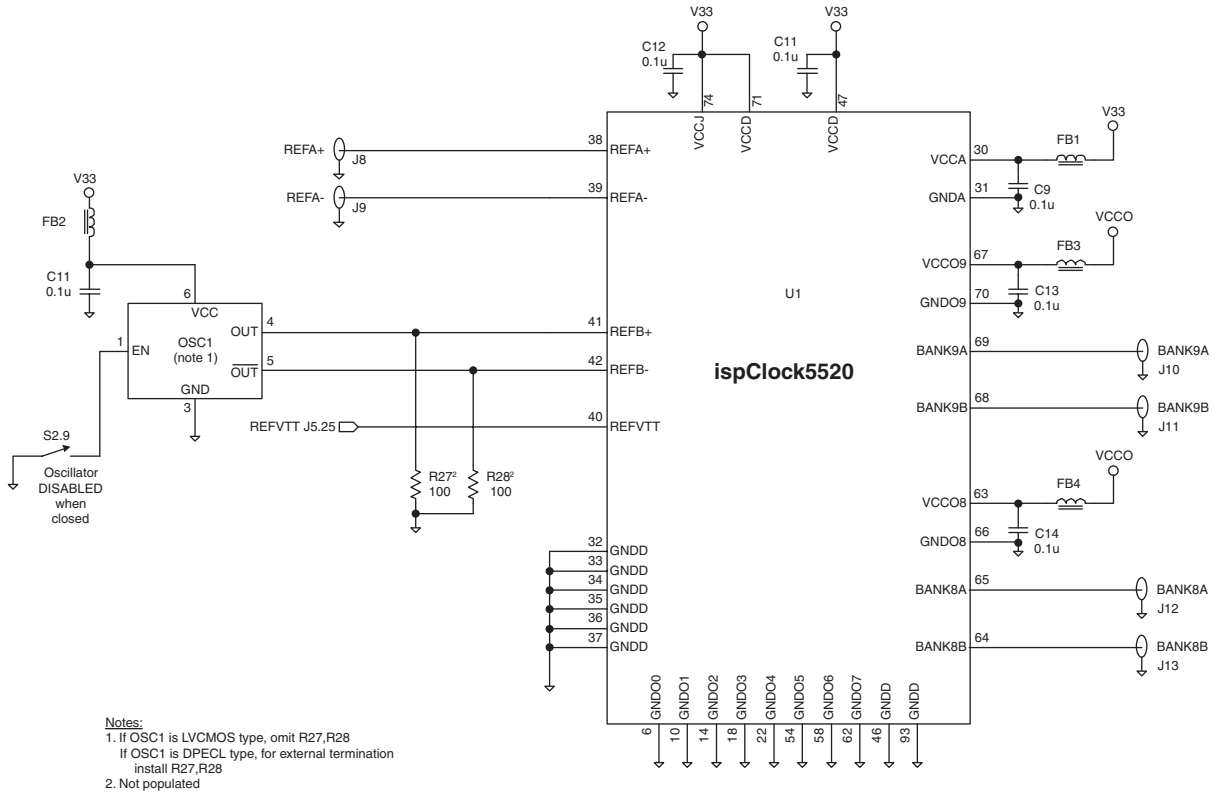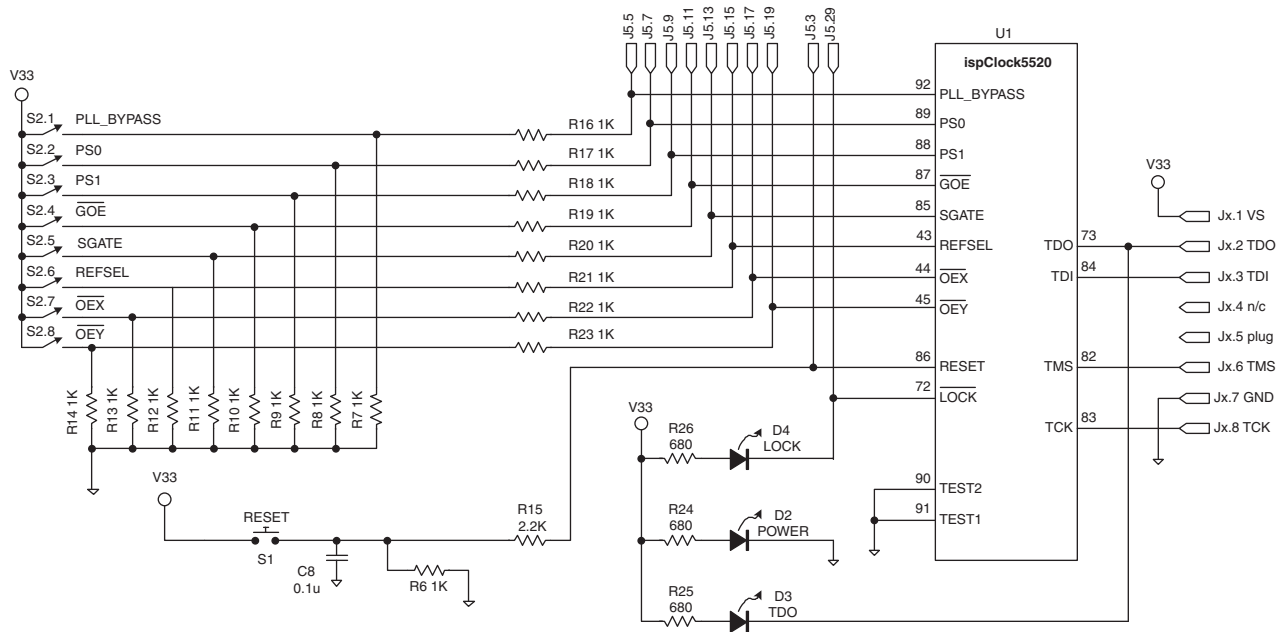2. Not populated

Figure 5. User Controls and Miscellaneous I/O
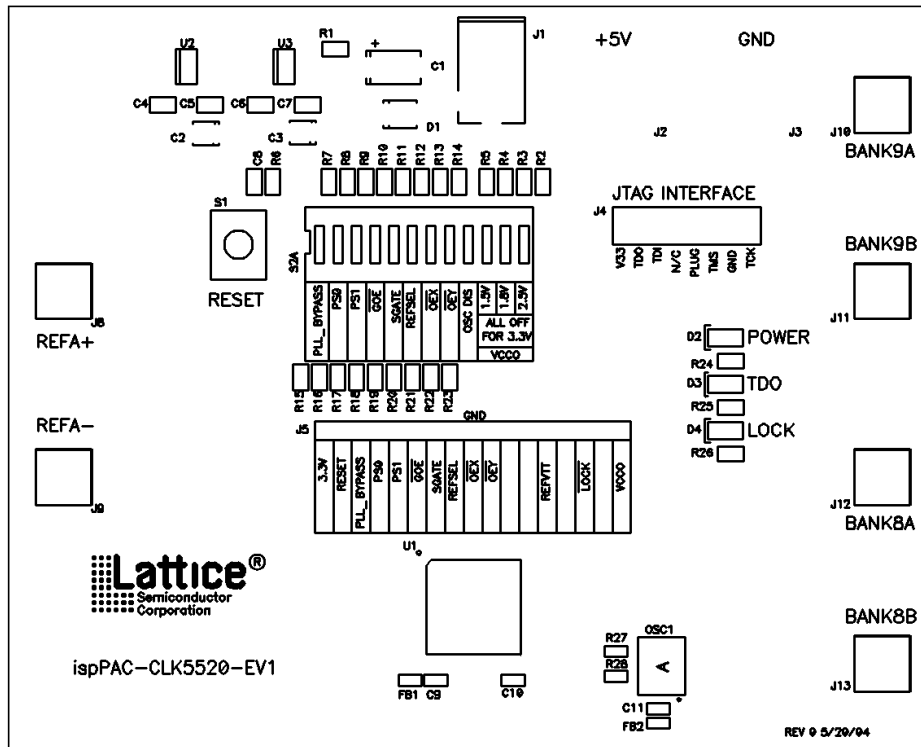
PCB Artwork

Figure 6. Silk Screen
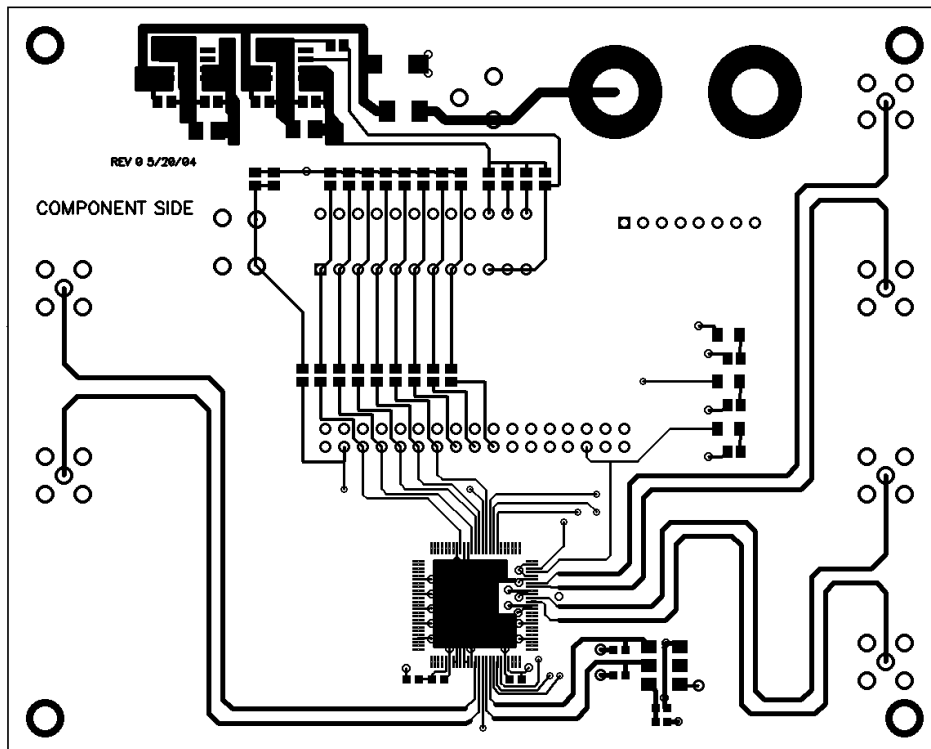

Figure 7. Component Side Copper (Layer 1)
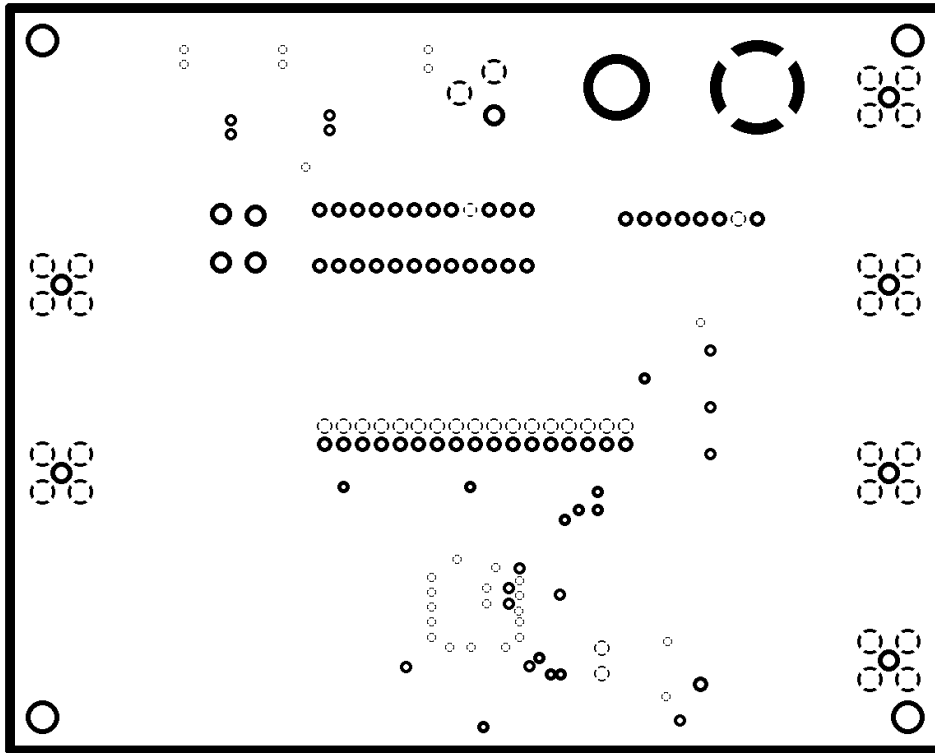
Figure 8. Ground Plane (Layer 2)

Figure 9. Power Plane (Layer 3)
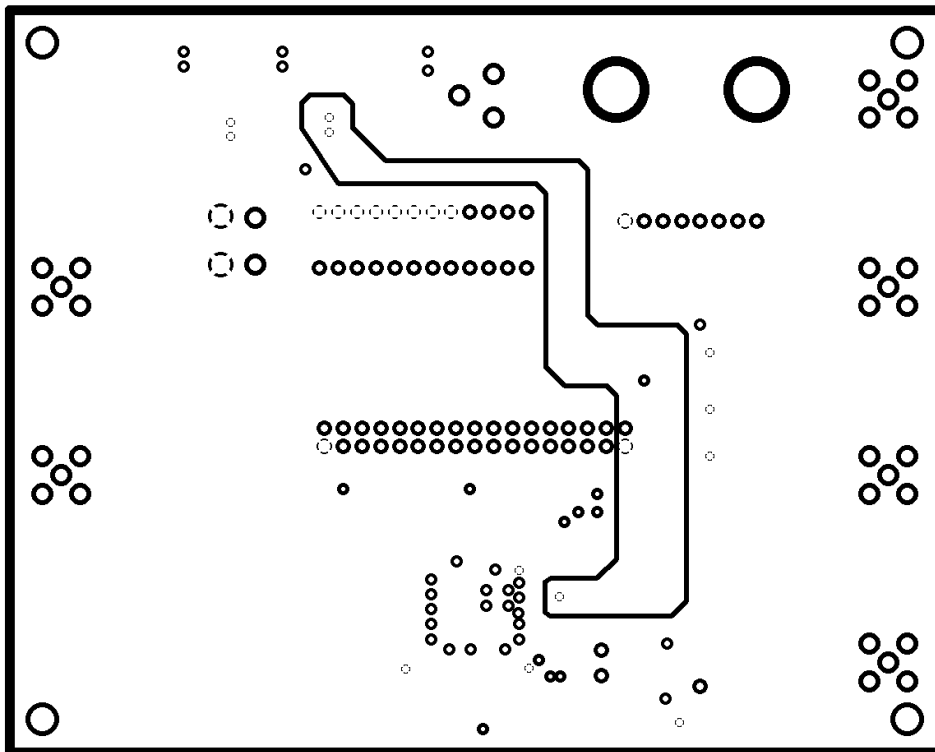
Figure 10. Solder-side Copper (Layer 4)
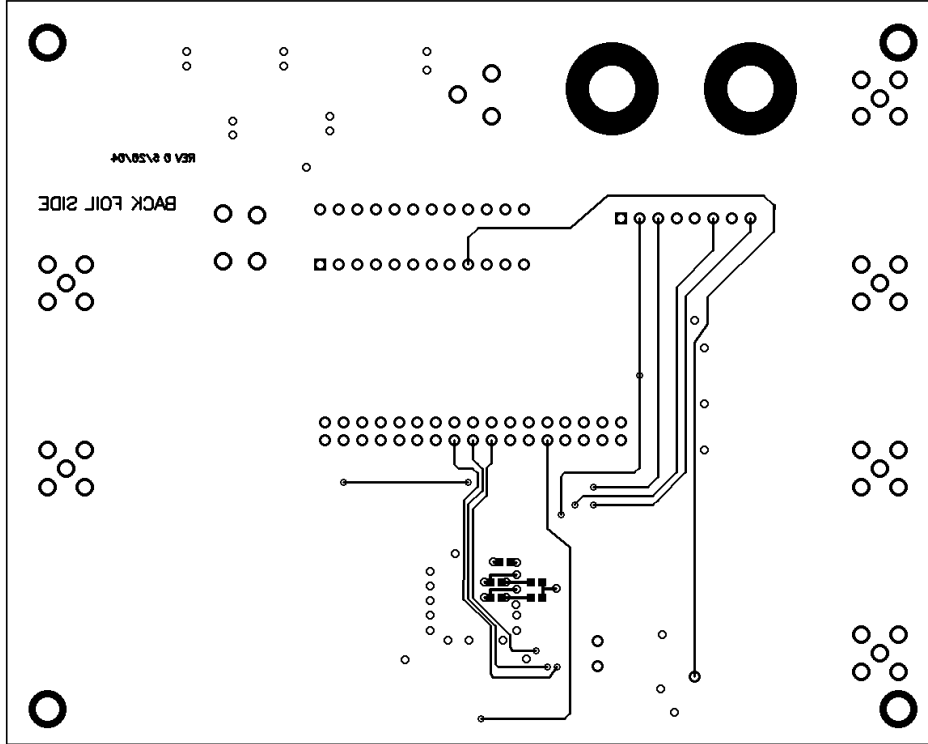
Component List

Quantity	Reference Designators	Description
1	n/a	ispPAC-CLK5520-EV1 Printed Wiring Board
1	C1	100µF 10V tantalum capacitor, Panasonic ECS-T1AD107R
2	C2, C3	10µF 10V tantalum capacitor, Panasonic ECS-T1AX106R
5	C4, C5, C6, C7, C8	0.1µF 16V capacitor SMD0805, Panasonic ECJ-2VB1C104K
6	C9, C10, C11, C12, C13, C14	0.1µF 16V capacitor SMD0603, Panasonic ECJ-1VB1C104K
1	D1	Schottky rectifier, International Rectifier MRBS130LTR
1	D2	Red LED SMD1206, LiteOn LTST-C150KRKT
1	D3	Yellow LED SMD1206, LiteOn LTST-C150KYKT
1	D4	Green LED SMD1206, LiteOn LTST-C150KGKT
4	FB1, FB2, FB3, FB4	SMD0603 Ferrite Bead, Steward MI0603J600R-00
1	J1	DC Power Connector, CUI PJ-102BH
1	J2	Banana Jack Red, SPC Technologies 845-R
1	J3	Banana Jack Black, SPC Technologies 845-B
1	J4	8-Position Single-Row Header, Molex 22-28-4084
1	J5	34-position Dual Row Header (Not Populated), Molex 10-88-1341
6	J8, J9, J10, J11, J12, J13	SMA Connector, Amphenol 901-144-8RFX
1	R1	100k 1% SMD0805 Resistor, Yageo 9C08052A1003FKHFT
1	R2	178k 1% SMD0805 Resistor, Yageo 9C08052A1783FKHFT
1	R3	300k 1% SMD0805 Resistor, Yageo 9C08052A3003FKHFT
1	R4	73.2k 1% SMD0805 Resistor, Yageo 9C08052A7322FKHFT
1	R5	31.6k 1% SMD0805 Resistor, Yageo 9C08052A3162FKHFT
18	R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23	1K 5% SMD0805 Resistor, Yageo 9C08052A1001JLHFT
3	R24, R25, R26	680Ω 5% SMD0805 Resistor, Yageo 9C08052A6800JLHFT
2	R27[1], R28[1]	100Ω 1% SMD0603 Resistor, Panasonic ERJ-3EKF1000V
1	S1	Momentary Tactile Switch, Panasonic EVQPAD04M
1	S2	12-position dipswitch, CTS 206-12ST
1	U1	ispClock5520 (ispPAC-CLK5520V-01T100I)
1	U2	3.3V fixed regulator SOIC8, Texas Instruments TPS77733D
1	U3	Adjustable regulator SOIC8, Texas Instruments TPS77701D
1	X1[2]	100MHz LVCMOS Oscillator, ECS-3953M-1000-B
4	n/a	Rubber Feet, 3M SJ-5003

1. Install only for use with differential PECL oscillator – see note 2.
2. Lower jitter performance may be obtained by using NEL Frequency Controls type SD-A2920/100.00MHz Differential PECL oscillator. If this device is installed, R27, R28 must be populated.

Technical Support Assistance

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