Power Decoupling and Bypass Filtering for Programmable Devices

Technical Note

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1. Introduction

Designers often overlook the effects of transient currents when designing high-speed systems. This is particularly an important concern when using volatile programmable devices in a system. Due to the nature of the varying requirements of device power-up, programming, and operation, the large varying current supply needs are seen by the more sensitive input stages through the common power supply rail, which serves all stages. This occurrence often happens if the power rail (be it wire, PCB trace, device packaging, or a combination of these) is of sufficiently high impedance. Even if the power supply rail impedance is *ideal* (zero Ω), this can still happen: as the frequencies go higher, the inductive reactance of the leads or PCB traces increases. PCB designs need to be properly decoupled to ensure these power supply noise issues do not affect the system operation and performance.

This technical note discusses aspects of power stabilization as it relates to two PCB board requirements – decoupling and filtering. Although many use these terms interchangeably, they are distinct and sometimes contradictory conditions. Decoupling is a means of insuring energy transfer capabilities at or to a specific point. Filtering relates to the conditioning of a signal along a path – with separate start and finish locations. Although good decoupling may preclude the requirement for filtering, filtering is not the primary consideration. Likewise, good filtering may include some decoupling, but it is not optimized for this task. This technical note highlights the need to plan and design for adequate power distribution. Use of the listed PCB design practices assures first time system success using Lattice Semiconductor programmable devices.

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2. General Power and Ground Recommendations

The electrical connections between the Lattice Semiconductor programmable devices and other devices on the board must provide a solid pathway to the power system to guarantee a high degree of signal integrity. The primary function of the power plane is to provide a low impedance path between the power-source and the device. The power plane must have low resistance to ensure minimum voltage drop to the device. This can be aided by keeping via connections to a minimum. When vias cannot be avoided, use large vias for power and ground connections. The power and ground vias should connect to all of the layers associated with a particular plane.

To summarize:

- Keep via usage to minimum
- Use large power and ground vias
- Connect power and ground vias to all power and ground layers

The power traces and vias should also be thoughtfully designed. The noise generated by the device can be minimized by having the power trace pass from a via to a decoupling capacitor pad and then to the device. Using this connection sequence, the resistance and inductance of the trace and via help isolate the component noise. Keep the trace between device and the bypass capacitor as short as possible. A short, wide trace produces a lower inductance and resistance.

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3. Decoupling Recommendations

Inadequate sizing and improper placement of power supply decoupling capacitors can result in numerous board problems. The most common problem associated with inadequate decoupling capacitance is power supply noise (that is, high frequency noise and/or droop). If the decoupling capacitor does not support the switching charge requirements of the device, the power supply must deliver the additional charge (or current). These additional charging and subsequent discharge can cause undesirable fluctuations. In all cases, it is the function of the decoupling. capacitor to deliver the quick burst of energy, within a specified time element, without generating a noise pulse or an apparent voltage droop.

It is always a good design philosophy to provide RF bypassing of power and DC control lines to the device. This is indeed the case when the device is located some distance away from the power supply. RF chokes and good bypassing capacitors of approximately 1000 pf to 100 µF are recommended at the DC supply lines. If the device is powered from a regulated power supply, the regulator noise increases depending upon the external load current drawn from the regulator.

The noise performance of the device may degrade depending upon the type of regulator used, and also upon the load current drawn from the regulator. To improve the noise performance of the device under external load conditions, place a low ESR (Equivalent Series Resistance) electrolytic capacitor of about 10 µF on the voltage line. Decoupling or bypass capacitors play a large role in device performance. The main role of bypass capacitors is to act as a local DC power supply to meet the demands of fluctuating power rails and block unwanted noise going into or coming from the power plane, as well as the device generated switching noise and capacitive and inductive coupling from adjacent board level planes and traces. Decoupling must consider many frequency bands. Below is a list of guidelines for proper decoupling when using the Lattice Semiconductor programmable devices:

- Bypass capacitor usage must take into account both a low ESR as well as the self-resonant frequency.
- Vary the use of 0.1 uF and 0.01 µF capacitors per device power pin is a good rule of thumb.
- Locate decoupling capacitors as close as possible to the device power pins and run short, wide traces to vias when they are required.
- Distribute some bulk capacitance (1 uF and 10 uF) throughout the layout to help eliminate low frequency coupling and maintain a low impedance power system.
- Use a large electrolytic capacitor (100 uF) at power source.

The additional switching current flowing from the power supply to the device on a printed circuit board (PCB) trace creates a voltage drop between the supply and device. A suggested common practice of using a minimum of one capacitor per power pin, placed as physically close to the power pins. SMT (Surface Mount Technology) or chip capacitors made of ceramic are best such as EIA (Electronic Industries Alliance) sizes 0603 or 0805. It is recommended that use of several size caps in parallel are appropriate, (that is, .1ufd, .01ufd, .001ufd). The reason for this is as the capacitors become smaller in value, they also become physically smaller. This results to less inductance, which may not be the most optimal for the design. However, this is less the case with SMT capacitors. Consult your capacitor data sheets for the impedance versus frequency plots.

3.1. High Frequency Isolation

There are instances wherein the power distribution between stages cannot be sufficiently bypassed. An inductive choke offers a high impedance path to any errant signals or noise between stages, while offering a very low resistance pathway to the supply. With device interfaces that have several independent device supplies that have common voltage values, these supplies often can share the common voltage rail if the board design can guarantee that the supplies are isolated.

This can be accomplished with simple LC filtering schemes to prohibit device supplies from being influenced by power supply fluctuations. An inductor or Ferrite Bead of about 4 uH to10 uH, with good current carrying characteristics and low resistance should be placed in series with the voltage source to choke off the high frequency noise that may be caused by other shared supplies.

Ferrite Bead Inductors such as Murata BLM31B601S, BLM11B601SPB, or their equivalent, offer good inductive supply isolation.

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These techniques should be considered especially with common-rails for input voltage references and termination. Designers use a *choke and capacitor network* to provide isolation between common supply rails and voltage references.

AC ripple should be < 50 mVp-p on input DC voltage reference supplies to insure proper input switching characteristics. Manufactures have made available discrete passive digital filter devices that provide filtering of AC ripple. These devices such as Panasonic ELK100 or equivalent provide substantial noise filtering across many bands.

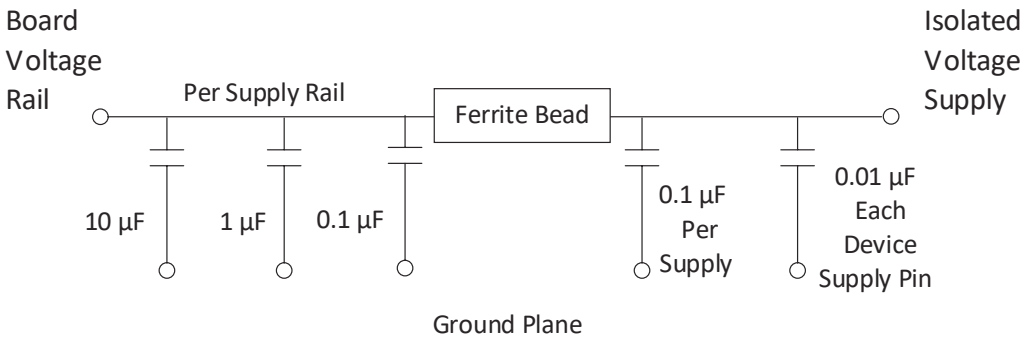

Figure 3.1. Suggested Isolation and Decoupling Scheme

3.2. Using Transient Suppression

It may become impossible to adequately reduce a board's exposure to voltage and current spikes. In this case, it is possible to momentarily clamp the spikes to the power supply protecting the devices on the board. For this, Transient Voltage Suppressors (TVS) can be used. These devices are similar to zener diodes, but offer a much faster turn-on time. There are several types of transient suppressor diodes available.

The TVS device should be selected to allow a device that will turn on at a specific voltage, clamping a voltage spike to the supply. The device turn-on voltage should be above the board (or design) V_{CC}, but below the level of potentially damaging noise.

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4. Conclusion

Proper device decoupling is critical in all board designs. This facet of PCB design is often marginalized or overlooked. Selection of the right decoupling capacitors, proper layout of power and ground planes, and thoughtful power distribution will provide a robust system by minimizing the noise floor of the board. Power supply decoupling is one of the most important aspects of board design and it is critical to use proper decoupling.

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Revision History

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Section	Change Summary
All	• Changed document number from TN1068 to FPGA-TN-02115. • Updated document template.
Disclaimers	Added this section.

Revision 1.0, May 2004

Section	Change Summary
All	Initial release.

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