Controlling and Monitoring Power-One Bricks and SIPs with Lattice Power Manager Devices

Introduction

As the semiconductor industry continues to improve both the speed and density of integrated circuits, the need for lower voltage and higher current power supplies has also increased. Along with the need for more power, many processors, ASICs, FPGAs, and modules require separate power supply voltages for different functions, such as core, I/O, and PLL. Many of these devices require that certain supplies turn on before others (sequencing) or in conjunction with others (tracking). In addition, many devices also require the supplies to turn on with a monotonically increasing ramp.

The ispPAC®-POWR1208 from Lattice is an In-system-Programmable mixed-signal stand-alone Power Manager IC that can monitor and sequence multiple supplies. This device is the preeminent choice for power supply sequencing and monitoring because of its versatile charge-pumps, open-drain outputs, and programmable logic core. The open-drain outputs can be interfaced to enable DC-to-DC power supplies for sequencing, while the programmable charge pump outputs can be used to ramp the gate of power MOSFETs to control the rate at which power is applied to the load.

Power-One Corporation is a leading supplier in the industry of DC-to-DC converters that offers a wide variety of both modular DC-to-DC converters (bricks), single-in-line pin DC-to-DC converters (SIPs) and point-of-load (POL) power supplies. These converters range in input voltages from 5V to 48V DC and output currents from 10A to over 50A in a variety of standard packages.

This application note describes how to successfully interface Power-One's SIPs and bricks with Lattice's ispPAC-POWR1208. The combination of DC-to-DC converters from Power-One and the Lattice's ispPAC Power Manager family provides an overall solution to the many challenges of power supply control. The first half of this application note focuses on SIP designs, while the latter half deals with the higher powered brick solutions.

## Enabling the SIS12VA SIP with the ispPAC-POWR1208

The SIS series of SIPs from Power-One are 12A single output power supplies that have a 5V input. They utilize negative enable logic and are turned off when the "ON/OFF" pin is pulled up and turn on when this pin is grounded or left floating. Because Lattice recommends that the open-drain outputs of the ispPAC-POWR1208 be programmed to reset high at power-up, a single pull-up resistor is all that is required to interface to the SIS12VA, as shown in Figure 7-1. If the point of load converter to be used is not the SIS series and has positive enable logic, a single transistor can invert the logic output of the ispPAC-POWR1208. Using an inverter will keep the converter off through the system power-up and only turn the supply on when the open-drain of the ispPAC-POWR1208 goes low. As a side note, the input and output of the supply were bypassed with low ESR capacitors using short traces (50 mils and wider) from the pins to caps.

Figure 7-1. SIS12VA Enabled by ispPAC-POWR1208
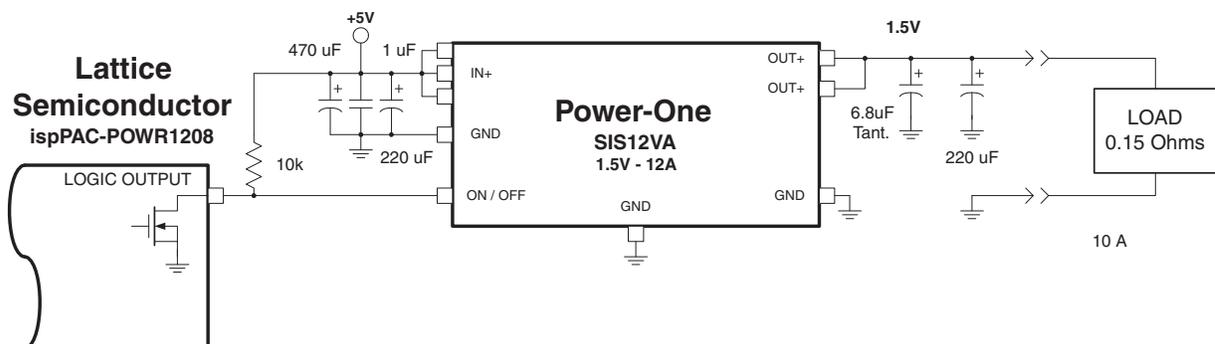
The oscilloscope plot in Figure 7-2 shows the output of the 1.5V SIS supply under load in relation to the open-drain output of the ispPAC-POWR1208 that enables the supply. The supply starts to turn on about 10µs after the open-drain goes low and has a bend in the slope 35µs later around 1.0V. The output voltage of the supply reaches its final level 120µs after the open-drain of the ispPAC-POWR1208 goes low.

Figure 7-2. Scope Shot of SIS12VA Output Under Load
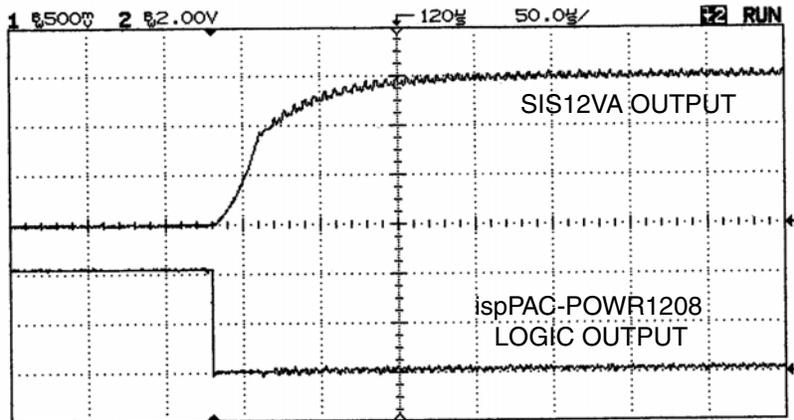
Ramping the SIP Output with a Power MOSFET

In some cases it is desirable to either have the voltage ramp up monotonically from zero to 1.5V or to slow the ramp down. By adding a series N-channel MOSFET between the output of the supply and the load, the ispPAC-POWR1208 can both enable the supply and control the rate at which voltage is applied to the load. Figure 7-3 shows the modified circuit using an International Rectifier IRL8103 MOSFET. The 100Ω resistor is placed physically near the gate lead to dampen the tendency of the MOSFET to self oscillate when used as a pass transistor. Because of the low gate charging current used, this added resistor does not significantly affect how the MOSFET turns on.

The saturated MOSFET does, however, add a series resistance of 0.01Ω to the existing path of traces and connectors from the supply output to the load. In our test circuit, the reduced voltage at the load is 1.367V, which is out of tolerance for a 1.5V supply. To bring the voltage at the load into tolerance, the SIS12VA has a trim pin that can be used to adjust the output voltage. For this series of supplies, the trim function is inverted, so a resistor from the trim pin to the output will cause the output voltage to go down. Likewise, a resistor from the trim pin to ground will cause the output voltage to go up. Data sheets for individual converters contain equations that can be used to estimate the value of the trim resistance. In this case, a 20kΩ resistor was placed between the trim pin and ground to bump the output voltage, at the load, up to the 1.5V level.

Figure 7-3. Adding a Series MOSFET to the SIS12VA Output to Control the Turn on Ramp to the Load
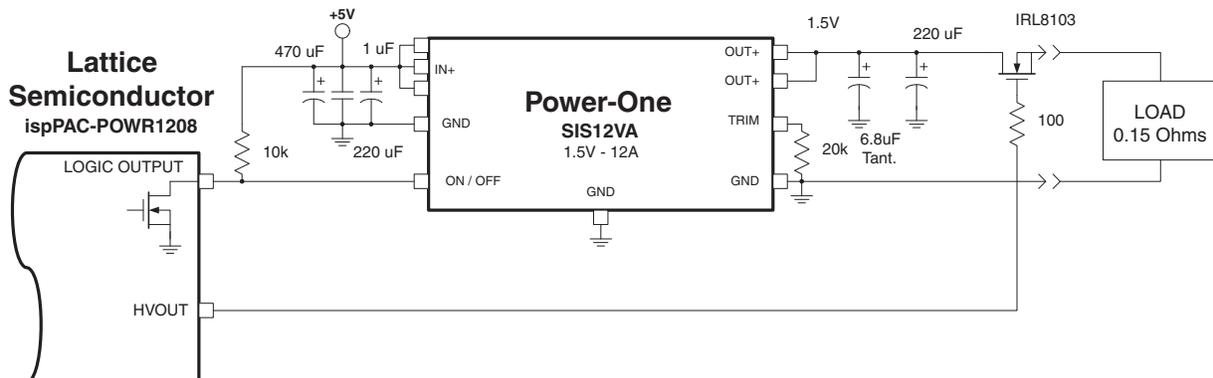
Figure 7-4 is an oscilloscope shot of the load voltage in relation to the open-drain output of the power-manager. Note the time scale is now 5ms instead of 50µs, a factor of 100 slower. This is because there is a longer delay from the open-drain transition to the start of the ramp and the ramp itself takes more time. Note that the voltage measured at the load rises from zero to 1.5V along one smooth ramp. The additional delay from the open-drain transition to the start of the ramp is the result of both a 4ms delay instruction in the Power Manager sequence and the ramping of the MOSFET gate with a constant current. The 4ms delay is added to the sequence to make sure the output of the supply is stable before engaging the MOSFET. An additional delay results from the MOSFET itself. This is because it does not turn on as soon as the HVOUT pin is activated. Rather, the MOSFET turns on when the gate-to-source voltage reaches the threshold for the device. With the HVOUT charge pump configured to source 1µA, it takes 11ms to charge the gate capacitance to the threshold voltage.

Figure 7-4. Scope Shot of Load Powering Up Using a Series MOSFET
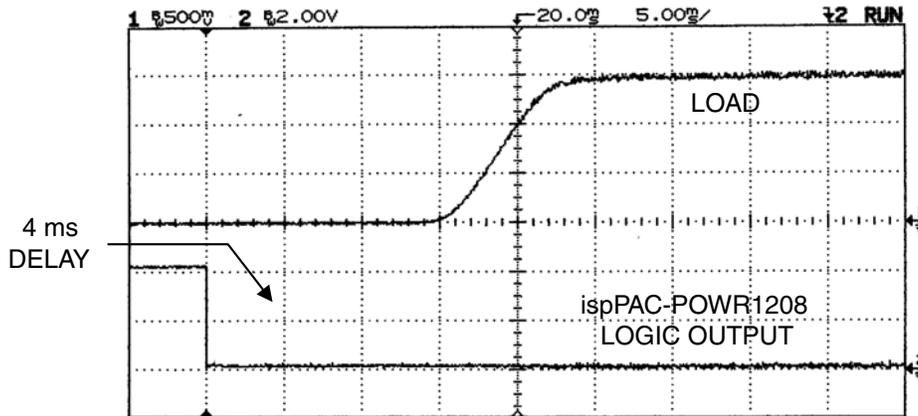
## Enabling the QLS25ZE Isolated Quarter Brick with the ispPAC-POWR1208

If the load requires more power or current than is available from a SIP package, Power-One provides several models of full-featured bricks. The QLS25 series of quarter-bricks operate on 48V input and are rated for an output of 25A without heat sinks. They are also available with either positive or inverted remote-enable logic. When the 48V supply is isolated or has a different ground than that of the ispPAC-POWR1208, which is typical of most telecommunication circuits, an optical-coupler is a cost effective and reliable solution to enable and sequence power bricks. Figure 7-5 is an example of how the QLS25ZE can be interfaced with the ispPAC-POWR1208 using an optical-coupler. When the open-drain output goes low, the LED in the optical-coupler is biased on, which turns on the output transistor. When the output transistor of the optical-isolator is saturated, the brick is turned on.

Figure 7-5. Optical isolator is used to enable Power-One QLS25ZE quarter brick
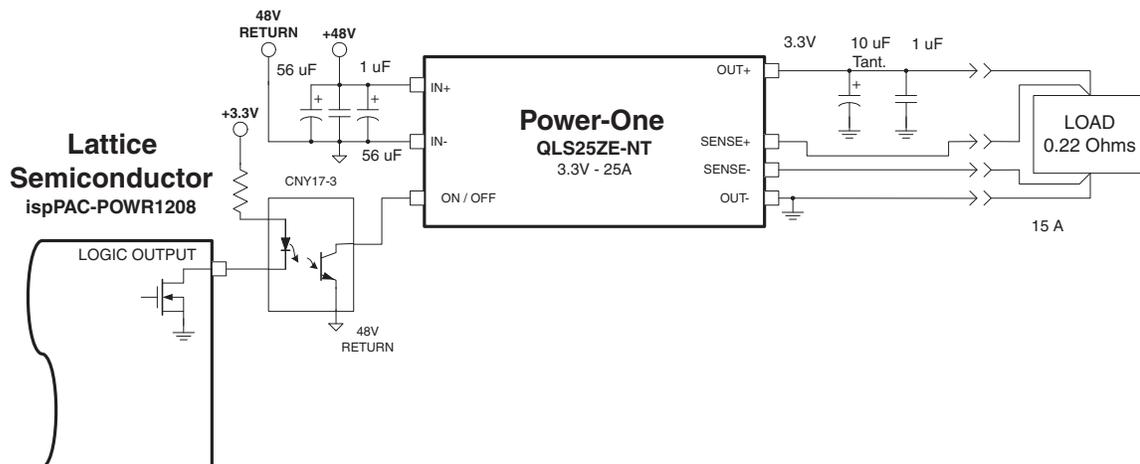
For low current loads, remote sensing is not required because the combined trace and connector resistance is typically less than 1Ω, and the brick's internal feedback (from the output to the sense pins – typically 5Ω to 1kΩ or more) maintains the desired voltage at the output pin. However, as the load current increases, a voltage drop will appear in both the supply and return lines, which will result in an under-voltage situation at the load. To compensate for this voltage drop, bricks provide remote sense pins that can be wired to the load (as shown in Figure 7-5) to override the internal feedback. This configuration will actively maintain the desired voltage at the load.

*Figure 7-6. Initial Power Up of QLS25ZE Quarter Brick Under Load*
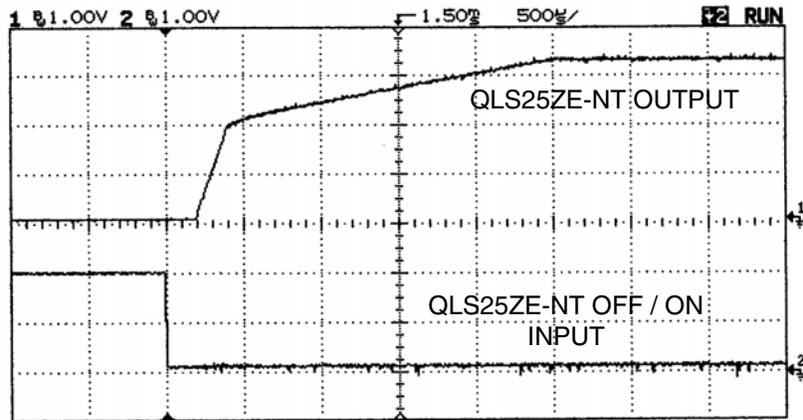
The significant features in the waveforms shown in Figure 7-6 are the start-up delay and the change in slope. The delay from when the enable pin is active to when the output is stable is about 2.5ms. Also note that a sharp change in the power-up ramp occurs near the 2.0V level.

## Ramping the Quarter Brick Output with Multiple MOSFETs

Some loads may require a slower or a more controlled power-up ramp than what is shown in Figure 7-6. Once again, the HVOUT pins of the ispPAC-POWR1208 can be used to smoothly ramp the voltage to the load at the desired rate. However, due to the higher current available from the brick output, multiple MOSFETs are used in parallel as shown in Figure 7-7.

Figure 7-7. Multiple MOSFETs are used to reduce the line drop from brick to load
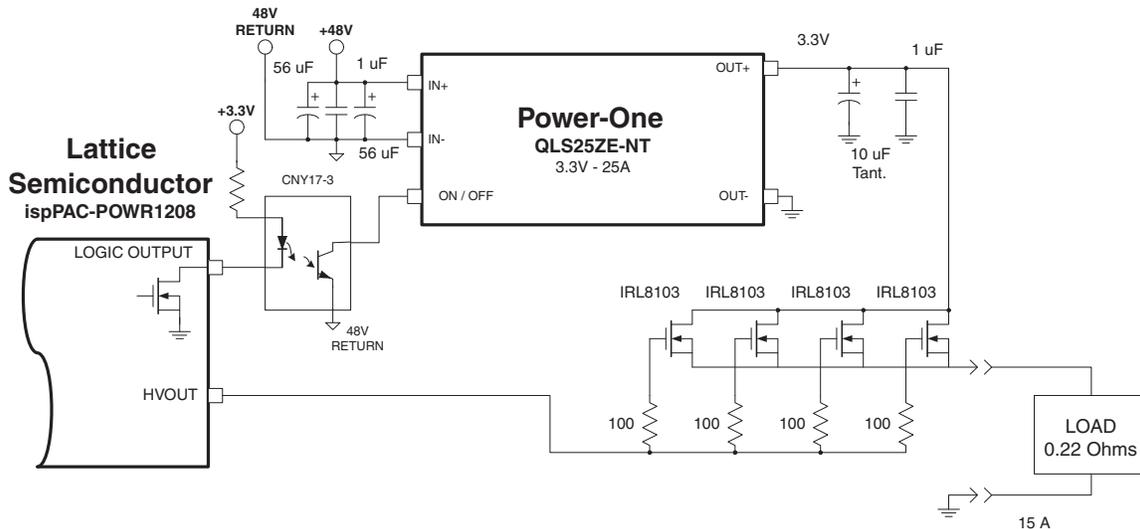
While the rated output current of the brick is only a fraction of the rated maximum drain current for a single MOS-FET, they are paralleled to reduce the voltage drop. For the circuit shown, the capacitive loading seen by the isp-PAC-POWR1208 HVOUT pin is quadrupled from what is was in the previous example. To adjust for this higher loading, the HVOUT is programmed to source 5uA instead of 1uA. This results in a turn-on-time of 15ms, as seen in Figure 7-8.

Figure 7-8. Load Voltage After Passing through Four MOSFETs
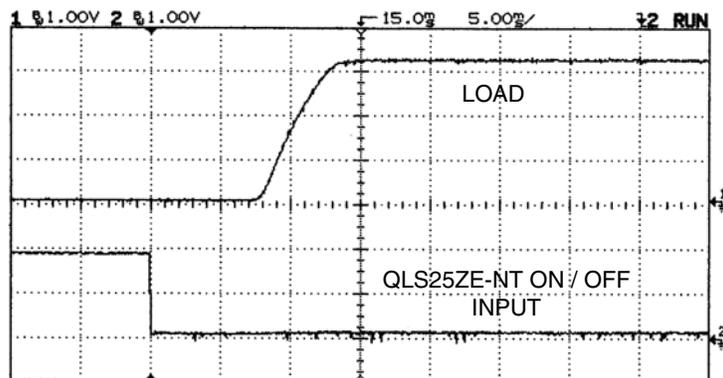
Summary

In this application note, we have seen how to enable the "ON/OFF" pin of the SIS12 series of DC-to-DC converters and how to use a trim resistor to adjust the voltage at the load. It was also shown how to use a series MOSFET to control the slope of the voltage ramp supplied to the load for both the SIP and brick converters. With regard to isolated supplies, it was shown how to use an optical-isolator to drive the "ON/OFF" pin to enable the output. Remote sensing is needed in cases where excessive line dropping occurs. For high current applications, it was shown how to parallel multiple MOSFETs to minimize the line drop and how to select the trim resistor. Thus, when Power-One DC-to-DC converters are used in conjunction with a few MOSFETS and the Lattice's ispPAC-POWR1208, a wide variety of complex power-sequencing requirements are easily addressed.

Related Literature

• ispPAC-POWR1208 Data Sheet

• AN6043 Using the ispPAC-POWR1208 MOSFET Driver Outputs.

• AN6046 Interfacing the ispPACPOWR1208 with Modular DC-to-DC Converters.

• AN6047 Powering Up and Programming the ispPAC-POWR1208

• AN6048 Using Power MOSFETs with the ispPAC-POWR1208.

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Revision History

Date	Version	Change Summary
October 2003	01.0	Initial release.
April 2008	01.1	Title changed from "Controlling and Monitoring Power-One Bricks and SIPs with the Lattice ispPAC-POWR1208" to "Controlling and Monitoring Power-One Bricks and SIPs with the Lattice Power Manager Devices."