DI2CSB

I²C Bus Interface Slave - Base version

ver 2.03

OVERVIEW

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data transmission over a short distance between many devices. The DI2CSB provides an interface between a passive target device e.g. memory, LCD display, pressure sensors etc. and an I2C bus. It can works as a slave receiver or transmitter depending on working mode determined by a master device. Very simple interface, composed with the read, write and data signals, allows easy connection to the target devices. The core doesn't required programming and is ready to work after power up/reset. The read, write, burst read, burst write and repeated start transmissions are automatically recognized by the core. The core incorporates all features required by I²C specification. The DI2CSB supports the following transmission modes: Standard, Fast and High Speed.

KEY FEATURES

- Conforms to v.2.1 of the I²C specification
- Slave operation
  - *Slave transmitter*
  - *Slave receiver*
- Supports 3 transmission speed modes
  - *Standard (up to 100 kb/s)*
  - *Fast (up to 400 kb/s)*
  - *High Speed (up to 3,4 Mb/s)*
- Allows operation from a wide range of input clock frequencies
- Support for reads, writes, burst reads, burst writes, and repeated start
- 7-bit addressing
- No programming required
- Simple interface allows easy connection to target device e.g. memory, LCD display, pressure sensors etc.
- Fully synthesizable
- Static synchronous design with positive edge clocking and synchronous reset
- No internal tri-states
- Scan test ready

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Cost-effective reliable automotive systems

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF netlist
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros

http://www.DigitalCoreDesign.com
http://www.dcd.pl

- ◊ Tests with reference responses
- ♦ Technical documentation
  - ◊ Installation notes
  - ◊ HDL core specification
  - ◊ Datasheet
- ♦ Synthesis scripts
- ♦ Example application
- ♦ Technical support
  - ◊ IP Core implementation support
  - ◊ 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

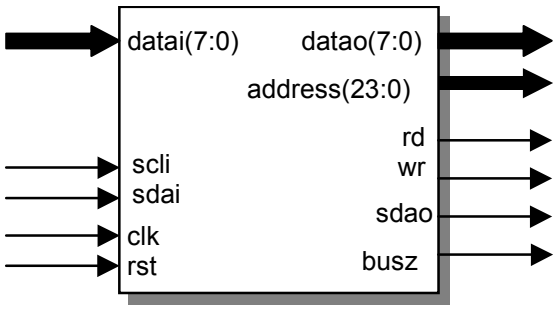
Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, *One Year* licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except *One Year* license where time of use is limited to 12 months.

- Single Design license for
  - *VHDL, Verilog source code called HDL Source*
  - *Encrypted, or plain text EDIF called Netlist*
- One Year license for
  - *Encrypted Netlist only*
- Unlimited Designs license for
  - *HDL Source*
  - *Netlist*
- Upgrade from
  - *HDL Source to Netlist*
  - *Single Design to Unlimited Designs*

SYMBOL



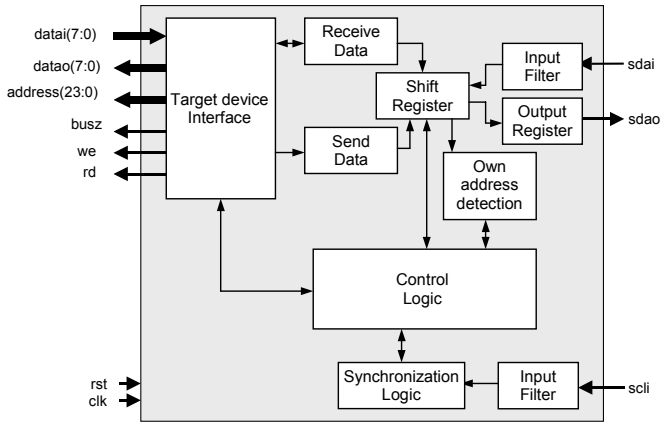
PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
rst	input	Global reset
datai(7:0)	input	Data bus from target device
scli	input	I^2C bus clock line (input)
sdai	input	I^2C bus data line (input)
datao(7:0)	output	Data bus to target device
address(23:0)	output	Address of accessed register
busz	output	Turns datao into Z state
wr	output	Write strobe for target device
rd	output	Read strobe for target device
sdao	output	I^2C bus data line (output)

BLOCK DIAGRAM

Figure below shows the DI2CSB IP Core block diagram.

Target device Interface – Performs the interface functions between DI2CSB internal blocks and target device. Allows easy connection of the core to a passive devices e.g. memory, LCD display, pressure sensors, I/O devices etc.



Control Logic – Manages execution of all commands sent via interface. Synchronizes internal data flow.

Shift Register – Controls SDA line, performs data and address shifts during the data transmission and reception.

Input Filter – Performs spike filtering.

Synchronization Logic – Synchronizes data and address shifts during the data transmission and reception. SCLI spikes are filtered by this unit.

PERFORMANCE

The following table gives a survey about the Core area and performance in the LATTICE® devices after Place & Route (all key features have been included):

Device	Speed grade	LUTs/PFUs	F_{max}
SC	-7	76 / 42	323 MHz
ECP2	-7	78 / 42	317 MHz
ECP2M	-7	70 / 27	318 MHz
XP2	-7	70 / 27	263 MHz
EC	-5	118 / 27	203 MHz
ECP	-5	118 / 27	212 MHz
XP	-5	118 / 27	180 MHz
ispXPGA	-5	79 / 21	180 MHz
ORCA 4	-3	90 / 15	129 MHz
ORCA 3	-7	73 / 17	84 MHz

Core performance in LATTICE® devices

The main features of each Digital Core Design I²C compliant cores have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application.

Design	I²C specification version	Master operation	Slave operation	CPU interface	Passive device interface	Interrupt generation	Clock synchronization	Arbitration	7-bit addressing	10-bit addressing	Standard mode	Fast mode	High-speed mode	User defined timing	Spike filtering
DI2CM	2.1	✓	-	✓	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
DI2CS	2.1	-	✓	✓	-	✓	✓	-	✓	-	✓	✓	✓	✓	✓
DI2CSB	2.1	-	✓	-	✓	-	-	-	✓	-	✓	✓	✓	-	✓

I²C cores summary table

CONTACTS

For any modification or special request please contact to Digital Core Design or local distributors.

Headquarters:

Wroclawska 94

41-902 Bytom, POLAND

e-mail: info@dcd.pl

tel. : +48 32 282 82 66

fax : +48 32 282 74 37

Distributors:

Please check http://www.dcd.pl/apartn.php