Power Estimation in ispXPGA™ Devices

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Introduction

The ispXPGA family of devices allows the creation of high-performance logic designs that are both non-volatile and infinitely reconfigurable. This family offers these capabilities within a mainstream architecture containing the features required for today's system-level designs.

Several elements must be considered when implementing a design in a programmable logic device. These issues include the device density, available I/Os, packaging, and power dissipated by the design. This technical note and the ispXPGA Power Estimation Worksheet (available on the Lattice web site at www.latticesemi.com) estimate power dissipated by ispXPGA devices based on device utilization and operating frequency. This document provides the tools needed to perform a thermal analysis of a design using ispXPGA devices. Please note that this is an estimation tool. Results may not match precisely with what is measured on the board. A thermal analysis of a design should be conducted to insure that a design will operate correctly in a particular device.

Power consumption is a function of ambient air temperature, device current, supply voltage, device loading, and output frequencies. Designers should complete a thermal analysis of their design early in the design process. This will help identify any thermal issues that should be modified to lower power consumption and thus reduce heat generation. Several thermal management options are discussed later in this document.

The architectural details of the ispXPGA device family can be found in the ispXPGA data sheet. Other factors required to estimate power, such as device resource utilization information, can be obtained from the report file generated by Lattice's ispLEVER® design tool.

A typical power estimation tool is based on the current estimation (I_{CC}) calculations for the device. The current estimation takes into consideration design parameters like resource usage, toggle rates, I/O power, HSI blocks usage, PLL usage, etc. The formulas used for calculations in the program are based on test design measurements.

Power Supply Current Calculations

The ispXPGA Power Estimation Worksheet contains all the equations and formulae that are discussed below for power estimation.

The worksheet requires users to input the following values:

Device	Select the appropriate device
V_{CC}	Power supply V_{CC} for the device, in volts
V_{CCJ}	JTAG power supply V_{CCJ} for the device, in volts
V_{CCO}	I/O power supplies V_{CCO} for the device, in volts
V_{CCP}	PLL power supply V_{CCP} for the device, in volts
Temp	Operating temperature of the device in °C
N	The number of each component used in the design (this can be obtained from the report file)
f_{MAX}	Maximum frequency at which the design is running, in MHz.
f_{MAX} PLL	Maximum Frequency at which the PLL is running, in MHz.
f_{MAX} HSI	Maximum Frequency at which the HSI is running, in MHz.
AF	Activity Factor is specified as a percentage of f_{MAX}.

The ispXPGA devices have multiple power pins: V_{CCJ}, V_{CCO}, V_{CC}, and V_{CCP}.

V_{CCJ} Supply

The JTAG power supply pin (VCCJ) current has two components: background current and I/O related current.

- Background current consumption for the VCCJ pin is minimal. The typical values are as follows:
  - 2.0 mA for a V_{CCJ} = 3.3V
  - 1.5 mA for a V_{CCJ} = 2.5V
  - 1.0 mA for a V_{CCJ} = 1.8V
- I/O related current is dependent on loads connected to the JTAG pins. The JTAG pins are normally tri-stated except during programming and test and only consume background current during normal operation when the JTAG port is inactive.

V_{CCO} Supply

The power supply pins for I/O banks current is dependent on loads connected to the I/O pins. The typical unloaded VCCO current (per I/O bank) is 2mA.

V_{CC} Supply

The power supply pin for core logic (VCC) is divided into following for current consumption (I_{CC}) calculations:

$I_{CC} = I_{DC} + I_{CORE}$

I_{DC} I_{DC} current is the device current consumption at 0MHz. For the values used for $I_{DC,}$ refer to the ispXPGA data sheet.

I_{CORE} I_{CORE} can be further split into the following components:

$I_{CORE} = I_{PFU} + I_{BLOCK\ RAM} + I_{HSI} + I_{ROUTING} + I_{PLL(D)} + I_{IO} + I_{CLOCK\ TREE} + I_{GLOBAL\ CTL\ NET}$

The various 'K' constants used in the equations that follow include:

K_{PFU}	Current per PFU unit (μA/ MHz)
$K_{BLOCK\ RAM}$	Block RAM frequency component (μA/ MHz)
K_{HSI}	Current per HSI Block unit (μA/ MHz)
$K_{ROUTING\ (GENERAL)}$	Current per general routing line (μA/ MHz)
$K_{ROUTING\ (LONG\ LINES)}$	Current per long line routing (μA/ MHz)
$K_{SRAM\ LINES}$	SRAM line component (μA/ MHz)
K_{IO}	Current per I/O from V_{CC} line (μA/ MHz)
$K_{CLOCK\ TREE}$	Current constant for the clock tree (μA/ MHz)
$K_{PLL(D)}$	Current constant for digital portion of PLL (μA/ MHz)
$K_{GLOBAL\ CTL\ NET}$	Current constant Global Control Lines (μA/ MHz)

For the values of these constants, please refer to the ispXPGA Power Estimation Worksheet.

PFU Current

PFU power is the current consumption by the PFU in a design. The I_{CC} can be calculated as:

$I_{PFU} = K_{PFU} * N_{PFU} * A_{FPFU} * f_{MAX}$

where:

K_{PFU} is the I_{CC} constant for PFU, in μA/MHz

N_{PFU} is the number of PFUs used in the design

AF is the Activity Factor or the percentage toggling

f_{MAX} is the frequency, in MHz.

BLOCK RAM Current
Similarly, we can calculate Block RAM Power as follows:

$I_{BLOCK\ RAM} = K_{BLOCK\ RAM} * N_{BLOCK\ RAM} * AF_{BLOCK\ RAM} * f_{MAX}$

HSI Block Current
For the power consumption of the HSI Block, the following calculation is used:

$I_{HSI} = K_{HSI} * N_{HSI} * f_{HSI}$

Routing Current
Routing is divided among two portions for I_{CC} value estimation, general routing and long lines. The I_{CC} calculations are as below:

$I_{ROUTING} = I_{ROUTING(GENERAL)} + I_{ROUTING(LONG\ LINES)}$

$= [K_{ROUTING\ (GENERAL)} * N_{ROUTING\ (GENERAL)} * AF_{ROUTING\ (GENERAL)} * f_{MAX}] + [K_{ROUTING\ (LONG\ LINES)} * N_{ROUTING\ (LONG\ LINES)} * AF_{ROUTING\ (LONG\ LINES)} * f_{MAX}]$

I/O Current
The I/O current calculation can be made as shown below:

$I_{IO} = K_{IO} * N_{IO} * AF_{IO} * f_{MAX}$

The number of I/Os can be divided into inputs and outputs. In the of case of bi-directional I/Os, add them to the number of outputs and use these values in the ispXPGA Power Estimation Worksheet.

Clock Tree Current
Clock Tree current consumption can be calculated as follows:

$I_{CLOCK\ TREE} = K_{CLOCK\ TREE} * N_{CLOCK\ TREE} * f_{MAX}$

PLL Current (Digital)
$I_{PLL(D)}$ is the PLL current consumption of digital V_{CC} power pin in mA as per the equation below:

$I_{PLL(D)} = K_{PLL(D)} * N_{PLL} * f_{PLL}$

Global Control Lines Current
$I_{GLOBAL\ CTL\ NET}$ is the Global Control Nets Current consumption of the V_{CC} power pin in mA is as per the equation below:

$I_{GLOBAL\ CTL\ NET} = K_{GLOBAL\ CTL\ NET} * N_{GLOCBAL\ CTL\ NET} * f_{MAX}$

Once all the above values are obtained, total current can be calculated as follows:

$I_{CORE\ =\ IPFU} + I_{BLOCK\ RAM} + I_{HSI} + I_{ROUTING} + I_{PLL(D)} + I_{IO} + I_{CLOCK\ TREE}$

Power consumption for V_{CC} will be:

$P = I_{CC} * V_{CC}$

V_{CCP} Supply

The VCCP pin is the power supply for the analog part of the PLL. There are eight PLLs available in the ispXPGA 1200. The ispXPGA Power Estimation Worksheet allows users to plug in the values for estimating power dissipation through $V_{CCP.}$

These values, once placed in the worksheet, will automatically calculate the total power consumption by the device.

Power Supply Design for ispXPGA Devices

The above power estimation pertains to the power consumption of a device while running. When designing the power supply, factors such as peak power-up current must be considered.

The maximum peak power-up currents measured for the ispXPGA devices are as per the table below. These are the peak current during a power-up cycle of approximately 200µs.

ispXPGA Device	Peak Power-up Current (mA)
ispXPGA 125	132
ispXPGA 200	200
ispXPGA 500	320
ispXPGA 1200	1500

Technical Support Assistance

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