



Avant Versa Board – Customizable HSB Sensor Interfaces

Reference Design

FPGA-RD-02329-1.0

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviations	Definition
APB	Advanced Peripheral Bus
AXI	Advanced eXtensible Interface
BOOTP	Bootstrap Protocol
CDC	Clock Domain Crossing
CRC	Cyclic Redundancy Check
DPHY	Digital Physical Layer
EBR	Embedded Block RAM
ECB	Ethernet Control Bus
FPGA	Field-Programmable Gate Array
FW	Firmware
GUI	Graphical User Interface
HDL	Hardware Description Language
HIF	Host Interface
HSB	Holoscan Sensor Bridge
I2C	Inter-Integrated Circuit
ICMP	Internet Control Message Protocol
IP	Intellectual Property (Core)
MAC	Media Access Control
MIPI	Mobile Industry Processor Interface
MPCS	Multi-Protocol Communication Stack
NGC	NVIDIA GPU Cloud
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PDC	Platform Design Constraint
PFU	Programmable Function Unit
PLL	Phase-Locked Loop
PTP	Precision Time Protocol
SDK	Software Development Kit
SERDES	Serializer/Deserializer
SFP	Small Form-factor Pluggable
SPI	Serial Peripheral Interface
STA	Static Timing Analysis
UDP	User Datagram Protocol
YAML	YAML Ain't Markup Language

1. Introduction

This user guide describes the reference design for customizable HSB sensor interfaces, implemented using the Lattice Semiconductor Avant™-X Versa Evaluation Board. The customizable interfaces in this reference design are divided into two categories.

Note: Only a single Ethernet port is used for the Avant-X Versa Evaluation board for current support.

- **Sensor Interface**

This reference design targets a MIPI CSI-2 camera sensor. The sensor interface is designed to be flexible and scalable, allowing you to integrate multiple camera sensors based on your requirements. The system supports various configurations to meet diverse imaging needs.

- **Host Interface**

The host interface focuses on Ethernet connectivity and supports multiple link speeds to accommodate varying data throughput requirements. This enables seamless communication between the sensor bridge and host systems.

In this reference design, the primary objective is to establish a robust and reliable bridge between the HSB interface and the NVIDIA host. Image tuning is not included and involves defining image quality parameters, configuring processing pipelines, and optimizing the Image Signal Processing (ISP). These tasks are highly specific to the camera sensor and require dedicated resources to achieve optimal results.

The reference design leverages NVIDIA's Holoscan Sensor Bridge solution and integrates smoothly within the broader NVIDIA ecosystem, enabling high-performance sensor data processing and transmission. An overview of the key components of the NVIDIA Holoscan Sensor Bridge solution and ecosystem is as follows:

1. **Sensors**
Targets the MIPI CSI-2 camera sensor.
2. **Holoscan Sensor Bridge (Lattice Avant-X Versa Evaluation Board)**
 - Lattice Avant-X Versa Evaluation Board functions as the Holoscan Sensor Bridge solution.
 - Performs sensor data pre-processing to reduce computational load on the host system.
 - The reference design is implemented in the Lattice FPGA targeting LAV-AT-X70 speed grade 3 device.
The key components of the reference design include:
 - **Sensor Interface**
 - Supports MIPI CSI-2 camera sensors.
 - Highly configurable to accommodate various camera sensors with different MIPI lanes and lane rates.
 - **Hololink IP**
 - Acts as a bridge between the sensor interface and the host system.
 - Handles data encapsulation, synchronization, and buffering to ensure smooth transmission of high-throughput sensor data.
 - **Host Interface (Ethernet link)**
 - Provides a high-speed Ethernet link to the host, supporting 10G or 25G speeds.
 - Enables low-latency, and high-bandwidth communication.
3. **Host (NVIDIA Jetson AGX ORIN Platform)**
 - Runs the Holoscan SDK to process incoming data.
 - Performs real-time AI inference, visualization, and decision-making.
 - Streams processed data to the cloud or other edge devices.

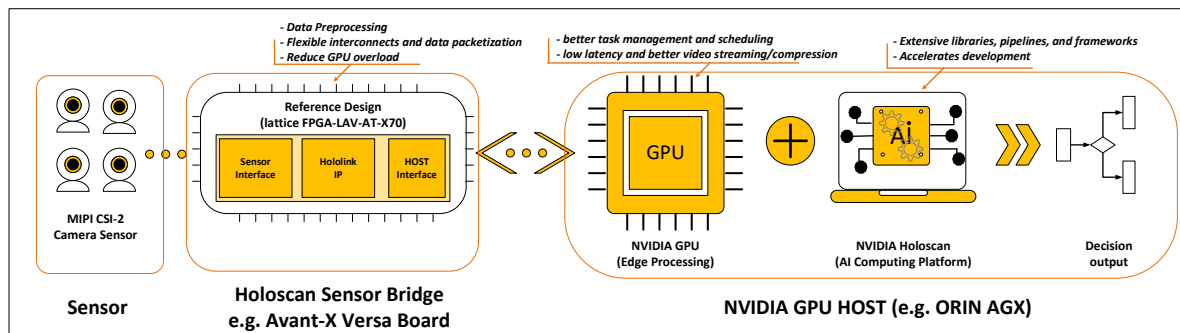


Figure 1.1. Overview of Customizable HSB Sensor Interface RD with NVIDIA ecosystem

1.1. Quick Facts

Table 1.1. Summary of the Reference Design

General	Target Devices	Avant-X FPGA (LAV-AT-X70-3LFG1156C)
	Source code format	Verilog and SystemVerilog
Simulation	Functional simulation	N/A
	Timing simulation	N/A
	Testbench	N/A
	Testbench format	N/A
Software Requirements	Software tool and version	Lattice Radiant™ software, version 2025.1.0.39.0
	IP version (if applicable)	<ul style="list-style-type: none"> CSI-2/DSI D-PHY Rx IP v2.0.0 OSC IP v2.1.0 PLL IP v2.6.1 10G Ethernet IP Core v3.3.1 25G Ethernet MAC+PHY IP Core v2.2.1 Hololink IP v2507
	Host Software	<ul style="list-style-type: none"> JetPack 6.2.1 NVIDIA Holoscan SDK 3.3.0 NVIDIA Jetson Linux 36.4.4 HSB SDK 2.2.0
Hardware Requirements	Board	<ul style="list-style-type: none"> Avant-X Versa Evaluation Board IMX258 camera module Ethernet 10GBase-T (Cat 6 RJ-45) SFP+ module (10G Ethernet) Ethernet 25G (Fiber) SFP28 module (25G Ethernet) Ethernet Switch (used to downscale 25G to 10G for Jetson AGX Orin) Display Monitor
	Host	<ul style="list-style-type: none"> NVIDIA Jetson AGX Orin Platform
	Cable	<ul style="list-style-type: none"> DisplayPort cable Ethernet Cat 6 cable Ethernet Fiber cable

1.1.1. Quick Start Guide

Refer to [Implementing the Reference Design on Avant-X Versa Board](#) for instructions on setting up and streaming video from the IMX258 camera module to the NVIDIA Jetson AGX Orin developer kit over a 10G or 25G Ethernet connection.

1.2. Features

Key features of the reference design include:

- Sensor Interface
 - Supports one or more camera sensors.
 - Designed to be customizable, allowing flexible configuration of the MIPI CSI-2 RX DPHY interface.
 - Enables integration of various camera types.
 - In testing, the Avant-X Versa Evaluation Board was used with a single MIPI CSI-2 camera.
- Hololink IP
 - Acts as a bridge between the sensor interface and the host system.
 - Implements Ethernet packetization and supports streaming DMA, control interfaces, and transport abstraction.
 - Enables low-latency, high-throughput data transfer from sensors to compute platforms.
 - Supports Precision Time Protocol (PTP) per IEEE 1588-2019 specification. PTP synchronizes the Hololink IP's internal time with the host time, enabling the host to act as the Time Transmitter and send PTP packets.
- Host Interface (Ethernet link)
 - Supports Ethernet channels with a link speed of 10G or 25G.
 - Uses UDP over Ethernet to stream sensor data directly to GPU memory.
 - Enables real-time AI inference and visualization with minimal latency.
 - In testing, the Avant-X Versa Evaluation Board was used with a single Ethernet port configured for either 10G or 25G.

1.3. Naming Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

- `_n` are active low (asserted when value is logic 0)
- `_i` are input signals
- `_o` are output signals

2. Directory Structure and Files

The following figure illustrates the directory structure of the reference design.

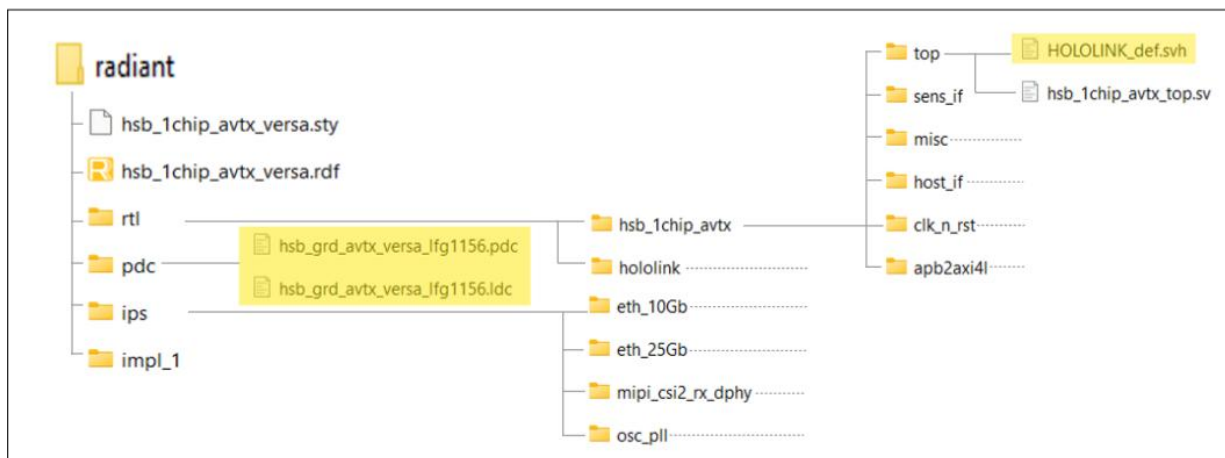


Figure 2.1. Directory Structure

Table 2.1. Folder Structure Description

Folder/File	Description
hsb_1chip_avtx_versa.rdf	This file is the Lattice Radiant software project file for the Avant-X reference design.
hsb_1chip_avtx_versa.sty	This file is the strategy file used for the project. Custom settings were applied to improve place-and-route results.
rtl/hsb_1chip_avtx	This folder contains HDL code for the sensor interface, host interface, top level design and other components.
rtl/hololink	This folder contains the encrypted Hololink IP. The current version is 2507.
pdc	This folder contains the LDC and PDC files.
ips	This folder contains IP cores used in the reference design, such as the oscillator, PLLs, MIPI CSI-2 RX DPHY IP, Ethernet 10G IP and Ethernet 25G MAC+PHY IP.
imp_1	This folder contains reports and logs generated during FPGA bitstream compilation.

Note: The highlighted files in [Figure 2.1](#) (HOLOLINK_def.svh, hsd_grd_avtx_versa_lfg1156.ldc and hsb_grd_avtx_versa_lfg1156.pdc) are important. The user is required to modify these files to create the intended reference design.

3. Functional Description

This section describes the architecture of the reference design. The system architecture includes several key subsystems working together seamlessly. The reference design includes three main components: the MIPI CSI-2 sensor interface, Hololink IP, and the Ethernet link as host interface. The reference design is implemented on the Avant-X Versa Evaluation Board. Figure 3.1 shows the overview of the reference design block diagram.

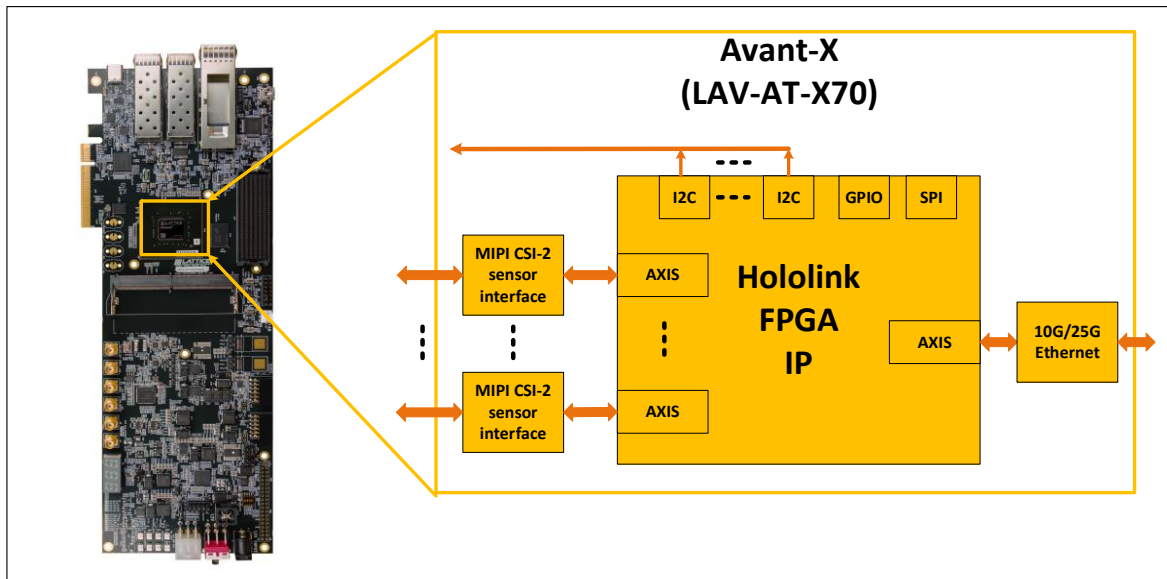


Figure 3.1. Overview of Reference Design Block Diagram

The MIPI CSI-2 sensor interface is highly customizable, supporting a variety of camera configurations based on user platform requirements. Its primary function is to receive raw image data from camera sensors and convert it into AXI-Stream (AXIS) payloads, which are then transmitted to the Hololink IP for further processing. This modularity ensures flexibility in adapting to different camera sensor types and resolutions.

The Hololink IP, provided by NVIDIA, serves as a critical bridge between the sensor interface and the host interface. It offers extensive configurability, including reconfigurable AXIS ports on both the sensor and host sides, and supports control peripherals such as I2C, GPIO, and SPI. This flexibility allows for seamless integration and communication between the sensor subsystem and the host processing platform.

The Ethernet block functions as the host interface. It supports both 10G and 25G link speeds with MAC+PHY IP cores. The Ethernet block connects to the Hololink IP via AXI-Stream ports and uses UDP over Ethernet to stream sensor data directly to GPU memory.

3.1. Customizable MIPI CSI-2 Sensor Interface

The customizable MIPI CSI-2 camera sensor interface has two capabilities:

- **Scalability**
Refers to the ability of the MIPI CSI-2 sensor interface to increase or decrease the number of the sensor interfaces based on user platform requirements.
- **Configurability**
Refers to the ability to configure each camera sensor interface individually, such as setting different MIPI CSI-2 lane counts and lane rates.

Figure 3.2 shows the block diagram of MIPI CSI-2 interface. It consists of two main components: the MIPI CSI-2 RX DPHY IP and the MIPI CSI-2 to AXIS payload converter.

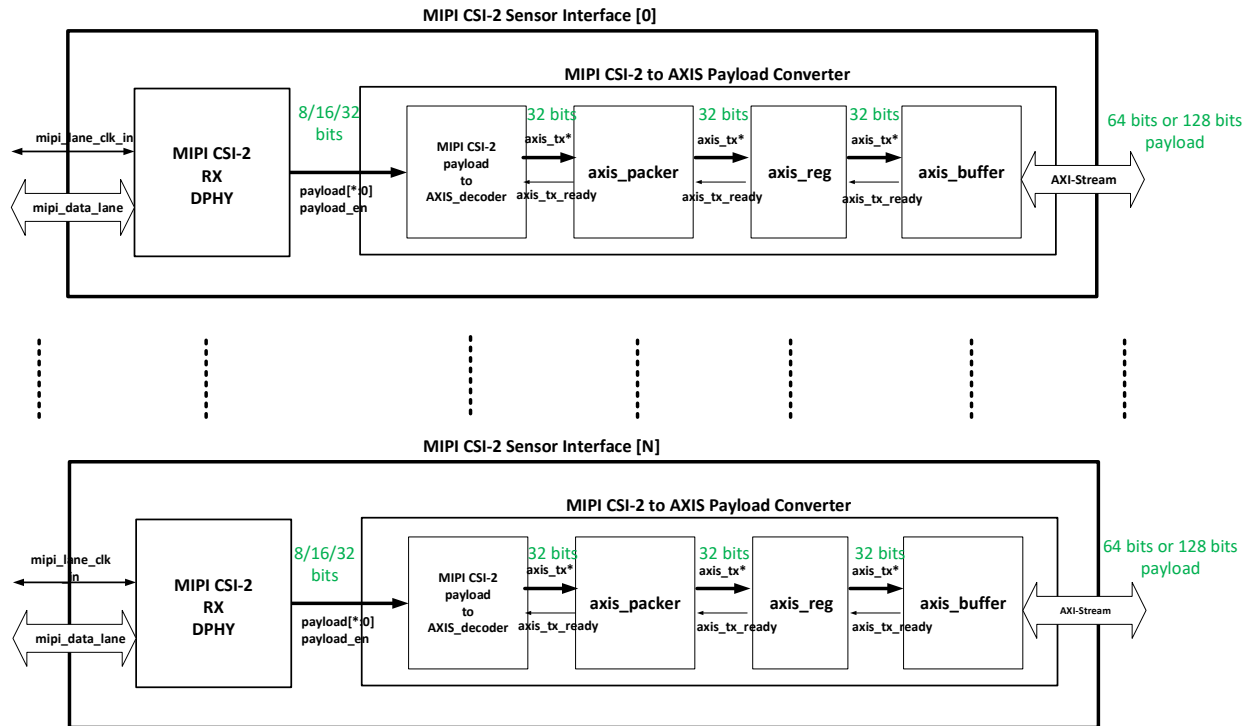


Figure 3.2. Overview block diagram of MIPI CSI-2 interface

3.1.1. MIPI CSI-2 RX DPHY IP

As the reference design targets the Avant-X device (package type), only the soft MIPI CSI-2/DSI RX DPHY IP is available. The soft MIPI CSI-2 RX DPHY IP is a configurable block. It receives MIPI CSI-2 data streams and converts them into parallel data formats such as 8-bit, 16-bit or 32-bit, based on the number of lanes configured during the IP generation. The IP provides flexibility to configure the MIPI CSI-2 lane rate as according to the camera sensor's requirement. Additionally, it generates an output byte clock based on the data type, which is passed to the AXIS blocks. When the sensor outputs a continuous D-PHY clock, it is recommended to disable RX_FIFO in the settings and drive the `clk_byte_fr_i` input clock directly using the `clk_byte_hs_o` output clock. However, the soft MIPI CSI-2 RX DPHY IP has limitations compared to the hardened version, particularly in performance. These limitations may vary depending on the FPGA device family and package type used. For more detailed specifications and configuration guidelines, refer to the [CSI-2/DSI D-PHY Receiver IP Core - User Guide \(FPGA-IPUG-02081\)](#).

3.1.2. MIPI CSI-2 to AXIS Payload Converter

The MIPI CSI-2 to AXIS Payload Converter module bridges the MIPI CSI-2 protocol and the AXI4-Stream (AXIS) interface. It extracts image data packets from the CSI-2 stream and reformats them into AXIS-compatible payloads for downstream processing.

This converter handles:

- Parsing of CSI-2 protocols elements (such as, long packets, short packets).
- Extracting payload from CSI-2 long packets.
- AXIS framing, including valid signals and handshake logic.
- Detecting errors in packet integrity and protocol compliance.

It enables seamless integration of camera sensor data into FPGA-based image processing pipelines using standard AXI4-Stream interfaces.

Note: Depending on the Hololink IP version, some features listed above may not be used. For example, in Hololink IP version 2507, *parsing of CSI-2 protocols elements (such as, long packets, short packets)* and *detecting errors in packet integrity and protocol compliance* are not supported.

3.1.2.1. MIPI CSI-2 Payload to AXIS Decoder Module

This module extracts image data packets from the CSI-2 stream and converts them into AXIS-compatible payloads. It supports CSI-2 stream output in parallel RAW10 formats of 8-bit, 16-bit, or 32-bit, as provided by the MIPI CSI-2 RX D-PHY IP. AXIS-compatible payloads are data packets formatted according to the AXI4-Stream (AXIS) protocol.

1. Structured data words: Payloads are aligned into fixed-width data words.
 - TDATA[31:0]: Carries the payload of the MIPI CSI-2 RAW10
2. Control signals: Each payload includes AXIS control signals:
 - TVALID: Indicates valid data.
 - TREADY: Handshake signal from the receiver.
 - TLAST: Marks the end of a frame or packet.
 - TKEEP[3:0]: Specifies which bytes in the data word are valid.
 - TUSER[1:0] Typically used for user-defined metadata.
 - tuser[0] is asserted during cycles containing embedded data (MIPI Data Type = 0x12)
 - tuser[1] is asserted on the final clock cycle of a long packet, indicating the line end signal.

3.1.2.2. AXIS Packer Module

A key feature of this module is its handling of the TKEEP signal, which indicates the validity of individual bytes within each data word. The AXIS Packer filters out invalid TKEEP bits, ensuring that only valid image data is included in the output stream. This maintains data integrity and prevents downstream modules from processing corrupt or incomplete payloads.

3.1.2.3. AXIS REG Module

The AXIS REG module acts as a simple register stage within the AXIS data path. Its primary function is to shift and hold one cycle of AXIS data, helping to manage timing, pipeline depth, and synchronization between modules.

3.1.2.4. AXIS Buffer Module

The AXIS Buffer Module receives AXIS data from the AXIS REG module and passes it through a dual-clock FIFO (DC_FIFO) to facilitate clock domain crossing (CDC). This ensures reliable data transfer between modules operating in different clock domains.

Key functions include:

- Data buffering: Temporarily stores AXIS data and control signals to manage timing differences.
- Clock domain crossing: Uses DC_FIFO to safely transfer data between asynchronous clock domains.
- Flow control: Maintains AXIS protocol integrity using TVALID, TREADY, and TLAST signals across domains.

This module is essential in systems where the CSI-2 receiver and downstream AXIS processing blocks operate on separate clocks, ensuring smooth and error-free data streaming.

3.2. Hololink IP

3.2.1. Overview

A detail explanation on the Nvidia Hololink IP is provided in the NVIDIA documentation webpage, [Holoscan Sensor Bridge v2.2.0](#) - NVIDIA Docs. You are encouraged to review the document for further understanding. This section provides only an overview of the IP.

The NVIDIA Holoscan Sensor Bridge FPGA IP works with the Holoscan software to provide a sensor-agnostic platform that transfers data from various sensors to an Ethernet-connected host.

The Holoscan Sensor Bridge FPGA IP, comprises three main components: the Sensor Interface IP, the Hololink IP, and the Host Interface IP. [Figure 3.3](#) illustrates the block diagram of the Holoscan Sensor Bridge FPGA IP. The Sensor Interface and Host (Ethernet) Interface blocks are implemented using FPGA vendor-specific logic. In this reference design, Lattice Semiconductor is responsible for the integration and maintaining the IP for both the Sensor Interface and Host Interface components.

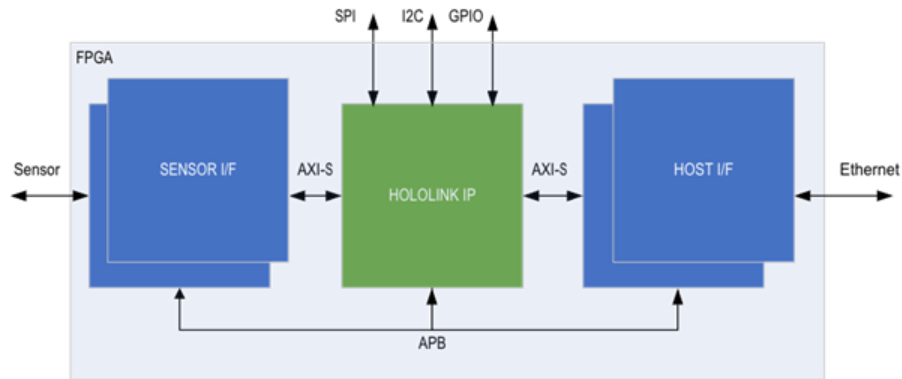


Figure 3.3. Holoscan Sensor Bridge IP in FPGA

The Holoscan Sensor Bridge FPGA IP streamlines FPGA development, offering scalability and configurability to support a wide range of sensor-to-host applications.

Key functions of the Holoscan Sensor Bridge IP include:

- Encapsulation of sensor data: Converts AXI-Stream sensor data into Ethernet UDP AXI-Stream format for host-side processing.
- Network protocol support: Implements BOOTP, ICMP, and NVIDIA-defined Ethernet Control Bus (ECB) protocols.
- Event and control packet transmission: Sends enumeration and control event packets based on predefined conditions.
- Peripheral interface control: Manages SPI, I2C, and GPIO interfaces to configure sensors and other onboard components.

3.3. Ethernet 10G/25G Support in Avant-X Device

The Avant-X device supports high-speed Ethernet connectivity via integrated IP cores and external transceiver modules. This section outlines the supported configurations for both 10G and 25G Ethernet, including key components, integration details, and functional descriptions.

3.3.1. Ethernet 10G Support with 10GBase-T SFP+ Transceiver

The Avant-X device supports 10G Ethernet using SFP+ transceivers, enabling high-speed data communication for bandwidth-intensive applications. The solution combines multiple IP cores and hardware components.

Key Components:

- **MAC IP Core**
Manages Ethernet frame-level operations, including encapsulation, CRC generation, and flow control. Interfaces with system logic via AXI or Avalon, depending on the FPGA architecture.
- **PCS IP Core (Physical Coding Sublayer)**
Handles low-level physical-layer functions and interfaces directly with the SFP+ module.
Features:
 - Encoding and Decoding: Supports 8b/10b or 64b/66b schemes.
 - Scrambling and Descrambling: Maintains signal integrity.
 - Clock Data Recovery (CDR): Aligns incoming data with system clock.
 - Link synchronization: Establishes and maintains stable link.
 - Error handling: Includes optional Forward Error Correction (FEC) for enhanced reliability.
- **SFP+ Transceiver Module**
A compact, hot-swappable module used for 10G connections.
Features:
 - Hot-swappable: Enables module replacement without shutting down the system.
 - Media support: Compatible with copper and fiber (such as SR for short range, LR for long range).

- Diagnostics: supports real-time monitoring of temperature, power, and signal quality.
- Transmission range: Varies from a few meters (copper) to tens of kilometers (fiber).

The MAC and PCS IP cores work together to prepare and transmit Ethernet frames through the SFP+ module. This setup ensures high-speed, low-latency communication for advanced networking applications.

3.3.2. Ethernet 25G Support with 25GBase-SR SFP28 Transceiver

The Avant-X device supports 25G Ethernet using 25GBASE-SR SFP28 transceivers. This setup uses the Lattice 25G Ethernet MAC+PHY IP core, providing high-speed 25Gbps connectivity. The integrated MAC and PHY communicate through a 25-Gigabit Media-Independent Interface (25GMII), enabling seamless data transmission and reception between the host system and Ethernet networks in 25GBASE-R applications.

Key Components

- **MAC IP Core**
Manages Ethernet frame processing, enforces media-access rules, supports flow control (pause frames, PFC), CRC/FCS checks, and collects statistics. Operates on a 128-bit data path at 195.3125 MHz with AXI4-Stream TX/RX interfaces.
- **PHY IP Core**
Handles PCS (64b/66b encoding) and PMA for the serial interface, with lane merging, loopback modes, and AXI4-Lite management.
- **25GBase-SR SFP28 Transceiver Module**
A compact, hot-swappable module used for 25GbE connections.

Features:

- Hot-swappable: Enables module replacement without shutting down the system.
- Media support: Compatible with fiber (such as SR for short range, LR for long range).
- Diagnostics: Supports real-time monitoring of temperature, power, and signal quality.

The 25G Ethernet MAC+PHY IP core integrates with the SFP28 module to process and transmit Ethernet frames, providing high-speed, low-latency 25Gbps communication for advanced networking applications.

3.4. Clocking and Reset Scheme

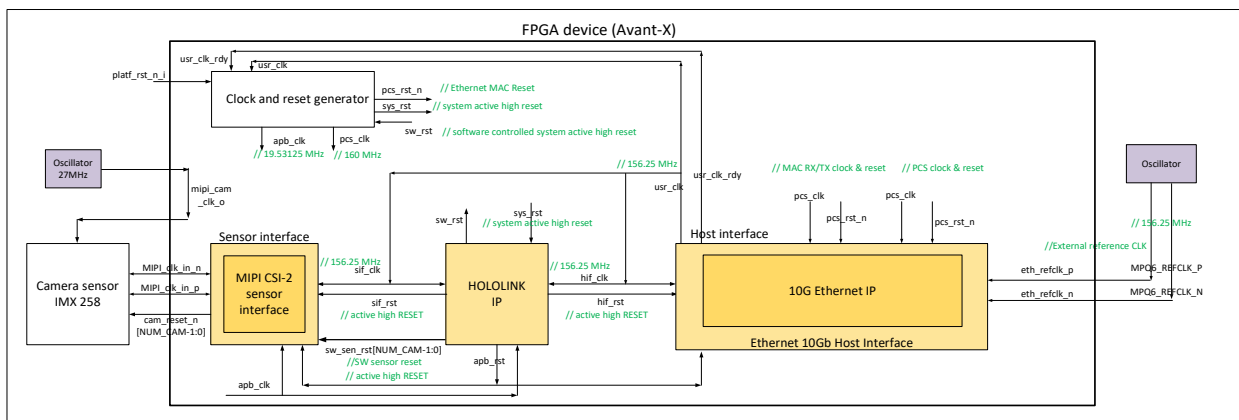


Figure 3.4. Reset and Clock Domain Block Diagram for Ethernet 10G

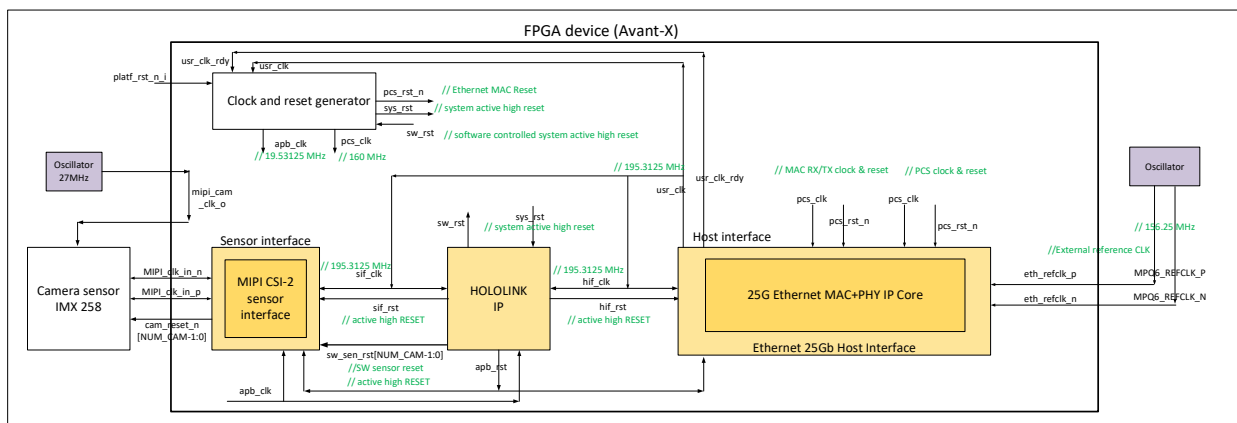


Figure 3.5. Reset and Clock Domain Block Diagram for Ethernet 25G

The following table lists the clock frequencies and their distribution.

Table 3.1. Clock Domain Distribution for Reference design with Ethernet 10G

Clocks	Frequency (MHz)	Description
usr_clk	156.25	Ethernet IP TX output clock used as a reference clock for the PLL to generate system clocks (such as apb_clk).
pcs_clk	160	PCS calibration clock.
hif_clk	156.25	Directly assigned from usr_clk and is used for host AXIS interface.
sif_clk	156.25	Directly assigned from hif_clk and is used as the AXIS clock for the sensor interface.
apb_clk	19.5313	APB bus clock.

Table 3.2. Clock Domain Distribution for Reference design with Ethernet 25G

Clocks	Frequency (MHz)	Description
usr_clk	195.3125	Ethernet IP TX output clock used as a reference clock for the PLL to generate system clocks (such as apb_clk).
pcs_clk	160	PCS calibration clock.
hif_clk	195.3125	Directly assigned from usr_clk and is used for host AXIS interface.
sif_clk	195.3125	Directly assigned from hif_clk and is used as the AXIS clock for sensor interface.
apb_clk	19.5313	APB bus clock.

Table 3.3. Reset Distribution applicable for both Ethernet 10G and 25G

Clocks	Description
sw_sen_rst[NUM_CAM-1:0]	Register-controlled sensor reset. The reset signal width increases based on the number of assigned cameras. Details are discussed in the Customizing the Reference Design section.
sw_sys_rst	Register-controlled system reset. Used to reset system-level logic. Also triggers reset for hif_rst, apb_rst, and sif_rst.
apb_rst	Reset APB logic
hif_rst	Reset Host logic
sif_rst	Reset Sensor logic

4. Customizing the Reference Design

4.1. Steps for Customizing Reference Design

This section provides a detailed walkthrough of the steps required to configure the reference design and to verify the customized reference design. [Figure 4.1](#) illustrates the steps involved to enable customization and support for various customer-specific configurations. Detailed explanation is provided in this section. However, details on reference design compilation and implementation are covered separately in [Compiling the Reference Design](#) section and [Implementing the Reference Design on Avant-X Versa Board](#) section.

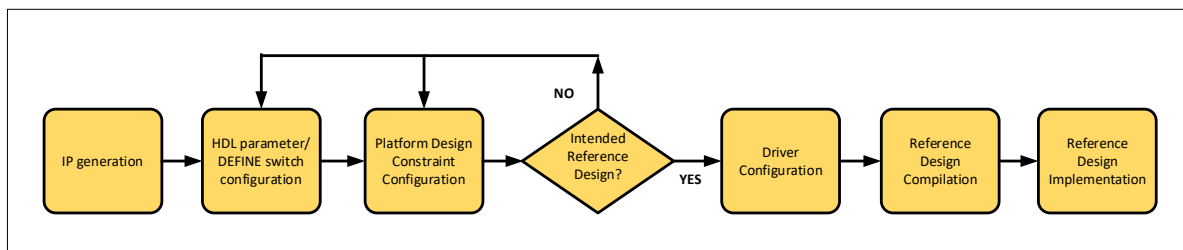


Figure 4.1. Steps Flow to Customize and Verify the Reference Design

4.1.1. IP Generation

4.1.1.1. MIPI CSI-2 RX DPHY IP generation

Each MIPI CSI-2 camera sensor interface requires a corresponding MIPI CSI-2 RX DPHY IP block. This IP must be generated based on the specifications of the camera sensor being used. The key parameters to configure includes:

- Number of data lanes
- MIPI lane rate
- Gear Ratio
- MIPI synchronizer clock frequency

These parameters must be correctly set before generating the IP to ensure compatibility with the camera sensor. The gear ratio for the Avant-X family device is fixed at 8, and the MIPI synchronizer clock frequency in the reference design is set to 160 MHz. The reference design also provides preconfigured MIPI CSI-2 RX DPHY IPs for users to choose from. The table shows the available IP configuration option that the user can select. The IP is selected based on user settings, which will be explained in the [HDL Parameter and Define Switch Configuration](#) section.

Table 4.1. Reference design's MIPI CSI-2 RX DPHY IP configuration options

MIPI Lane Rate (Mbps)	MIPI Lane Number	MIPI RX DPHY IP name
720	1 lane	mipi_csi2_rx_DPHY_720Mbps_1L.ipx
	2 lanes	mipi_csi2_rx_DPHY_720Mbps_2L.ipx
	4 lanes	mipi_csi2_rx_DPHY_720Mbps_4L.ipx
960	2 lanes	mipi_csi2_rx_DPHY_960Mbps_2L.ipx
	4 lanes	mipi_csi2_rx_DPHY_960Mbps_4L.ipx
1440	4 lanes	mipi_csi2_rx_DPHY_1440Mbps_4L.ipx
1500	4 lanes	mipi_csi2_rx_DPHY_1500Mbps_4L.ipx

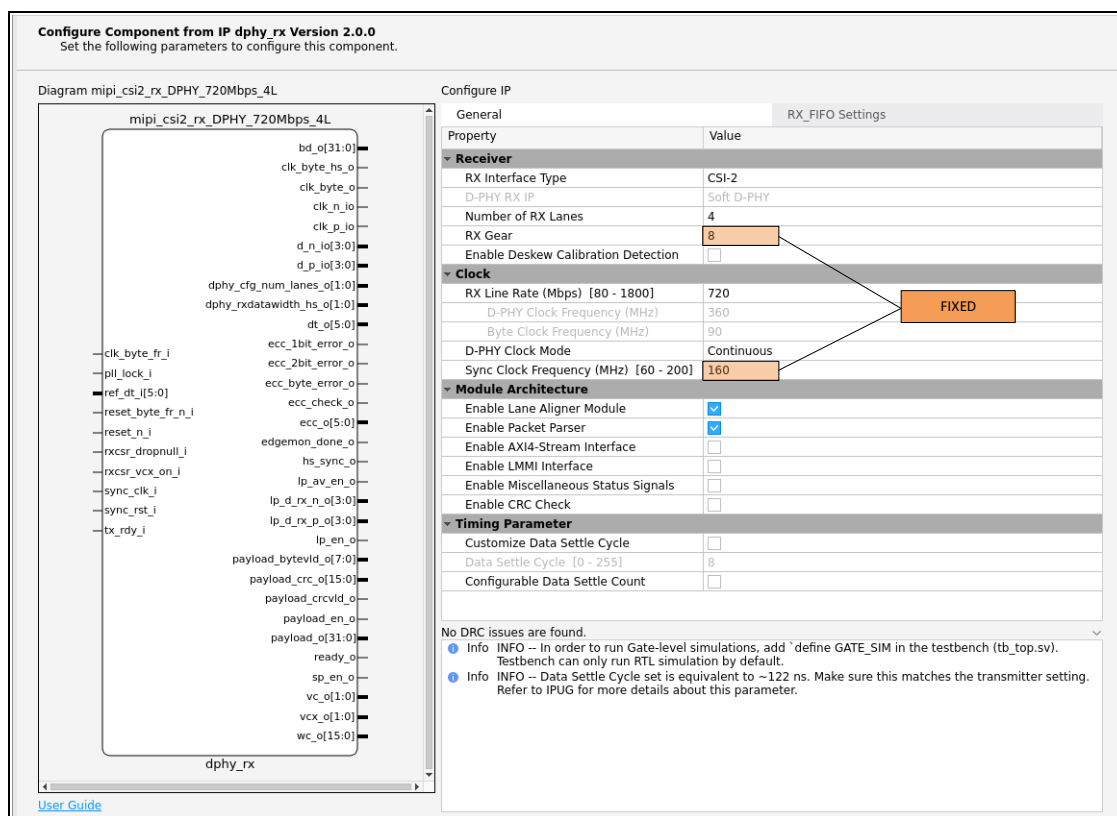


Figure 4.2. MIPI CSI-2 RX DPHY IP Generation Module

4.1.1.2. Hololink IP

Hololink IP is owned by NVIDIA, and NVIDIA updates the latest Hololink IP source code on GitHub at the following link, [GitHub - nvidia-holoscan/holoscan-sensor-bridge](https://github.com/nvidia-holoscan/holoscan-sensor-bridge) at 2.2.0-branch. The IP is encrypted. Currently, the reference design integrates the latest available Hololink IP, which is version 2507.

4.1.1.3. Ethernet IP Generation

Specific Ethernet IPs are required to support 10G or 25G link speeds in the Avant-X FPGA device. To support Ethernet 10G link speed, the 10Gb Ethernet IP Core v3.3.1 is used. To support Ethernet 25G link speed, the 25Gb Ethernet MAC+PHY IP Core v2.2.1 is used. The 10G and 25G Ethernet Lane ID is set to AUTO for the Avant-X Versa Evaluation Board before generating the IP. Figure 4.3 shows the 10Gb Ethernet IP generation, while Figure 4.4 shows the Ethernet 25Gb MAC+PHY IP generation.

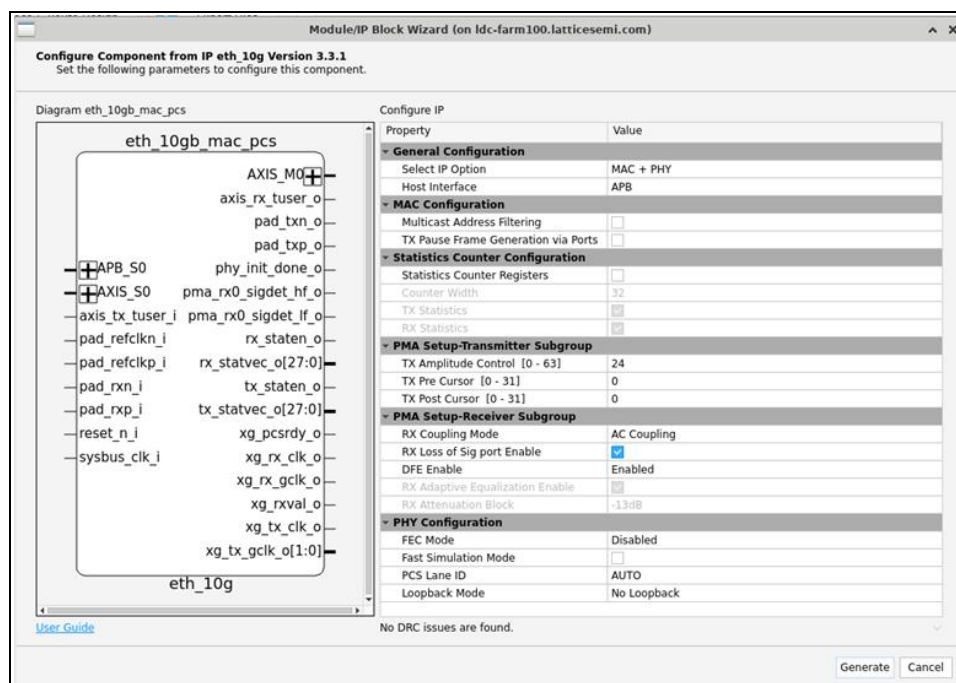


Figure 4.3. Ethernet 10Gb (MAC + PHY) IP Generation

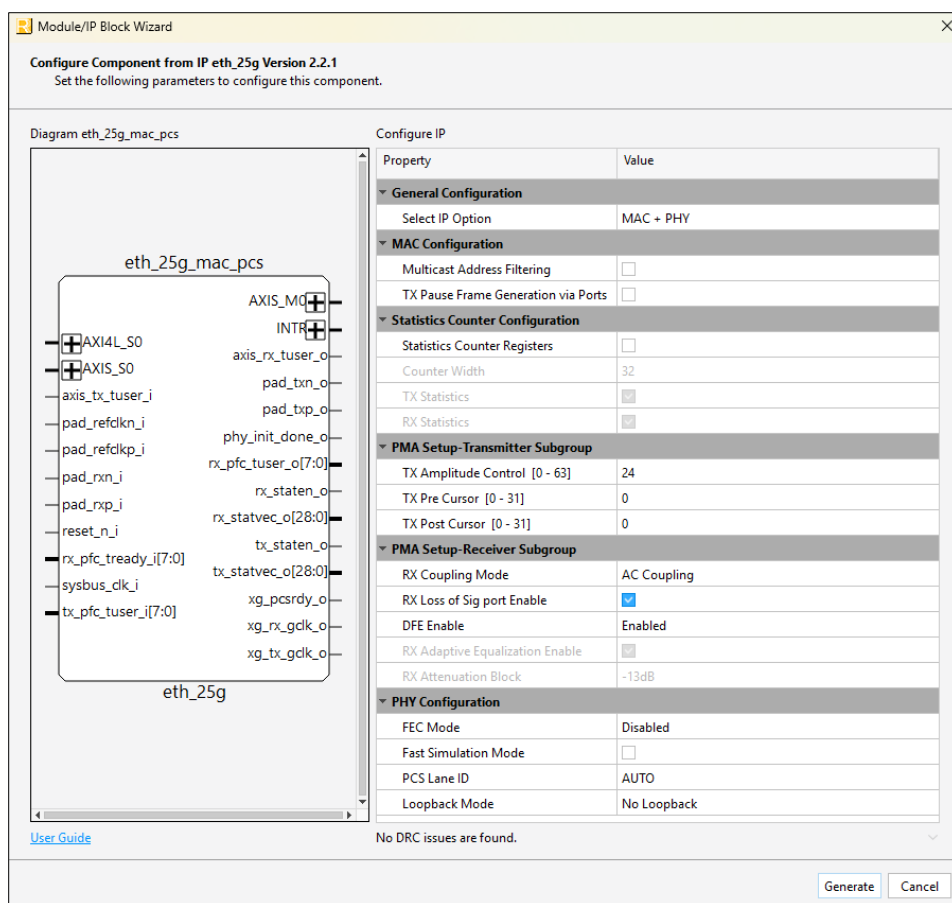


Figure 4.4. Ethernet 25Gb (MAC + PHY) IP Generation

4.1.2. HDL Parameter and Define Switch Configuration

Configure the HDL parameters and Define switches to reflect the desired hardware setup. These configurations modify the HDL design prior to compilation and affect the following aspects:

- Number of camera sensor interfaces
- Number of lanes per camera sensor
- Number of camera reset outputs
- I2C control peripherals for each camera sensor
- AXI-Stream ports connecting the sensor interface to the Hololink IP
- AXI-Stream ports connecting the Hololink IP to the host interface (Ethernet link)
- Ethernet link speed: 10G or 25G
- Number of Ethernet links used as host interface
- Ethernet MAC IP address

These changes should be made in the DEFINE file to ensure proper integration. The DEFINE file is located at:

<project_name>/radiant/rtl/hsb_1chip_avtx/top/HOLOLINK_def.svh

Configurations such as cameras reset outputs, I2C camera controls, and AXI-Stream ports for the sensor/host interface are automatically configured based on the number of camera sensors and assigned Ethernet 10G or 25G links.

Figure 4.5 shows the DEFINE switches that need to be changed in HOLOLINK_def.svh file. These settings must be carefully configured to ensure the HDL design reflects the intended hardware setup and supports the required camera sensor interfaces.



Figure 4.5. Define Switch Setting in HOLOLINK_def.svh File

Note: Figure 4.5 screenshot shows an example setting of four camera sensors. If more or less cameras are required for the intended reference design, the array size for `USR_NUM_RX_LANE[\"NUM_CAM-1:0\"]` and `USR_MIPI_RATE_Mbps[\"NUM_CAM-1:0\"]` will change. Therefore, the data assigned to it are trimmed or added based on the intended camera number usage.

4.1.3. Platform Design Constraint Configuration

Once the HDL design configuration is finalized, platform design constraints in both the LDC and PDC files are updated. An LDC and PDC template files are provided with this reference design and are located at:

```
<project_name>/radiant/pdc/hsb_grd_avtx_versa_lfg1156.ldc
<project_name>/radiant/pdc/hsb_grd_avtx_versa_lfg1156.pdc
```

```

1
2  set ETH_NUM 1
3
4  ldc_set_location -site {MPQ6_REFCLKP} [get_ports eth_refclk_p]
5  ldc_set_location -site {MPQ6_REFCLKN} [get_ports eth_refclk_n]
6  ldc_set_location -site {MPQ6_RX0N} [get_ports {eth_rxd_n[0]}]
7  ldc_set_location -site {MPQ6_RX0P} [get_ports {eth_rxd_p[0]}]
8  ldc_set_location -site {MPQ6_TX0N} [get_ports {eth_txd_n[0]}]
9  ldc_set_location -site {MPQ6_TX0P} [get_ports {eth_txd_p[0]}]
10 if {($ETH_NUM == 2) } {
11  ldc_set_location -site {MPQ6_RX1N} [get_ports {eth_rxd_n[1]}]
12  ldc_set_location -site {MPQ6_RX1P} [get_ports {eth_rxd_p[1]}]
13  ldc_set_location -site {MPQ6_TX1N} [get_ports {eth_txd_n[1]}]
14  ldc_set_location -site {MPQ6_TX1P} [get_ports {eth_txd_p[1]}]
15 }
16
```

Figure 4.6. LDC File Setting for Ethernet Ports and Pin Allocation

Figure 4.6 shows the LDC file settings for the Ethernet port configuration and pin allocation. Please note that the Avant-X Versa board supports a maximum of two SFP+ connectors.

```

1 #####
2 # BEGIN: USR CONFIG SETUP
3 #####
4 #-----
5 # 1) SENSOR IF SETTING: CAM MIPI
6 #-----
7 #
8 # 1.1) available number of CAM
9 #
10 set CAM_NUM 2
11 #
12 #-----
13 # 1.2) cam0 config setup
14 #-----
15 set CAM0_LANE0 4
16 set MIPI_lanerate0_inMbps 720
17 set mipigear0 8
18 #-----
19 # 1.3) cam1 config setup
20 #-----
21 set CAM1_LANE0 4
22 set MIPI_lanerate1_inMbps 720
23 set mipigear1 8
24 #-----
25 # 1.4) cam2 config setup
26 #-----
27 set CAM2_LANE0 4
28 set MIPI_lanerate2_inMbps 720
29 set mipigear2 8
30 #-----
31 # 1.5) cam3 config setup
32 #-----
33 set CAM3_LANE0 4
34 set MIPI_lanerate3_inMbps 720
35 set mipigear3 8
36 #
37 #-----
38 # 2) HOST IF SETTING: ETHERNET
39 #   ETH_SPD at 10G/25G etc.
40 #-----
41 set ETH_NUM 1
42 set ETH_SPD 25 #ETH_SPD_10
43 #
44 #
```

Figure 4.7. PDC File Setting for 10G or 25G

Figure 4.7 shows the PDC file settings for the number of camera sensors, data lane, and lane rates used for each camera sensor, as well as the number of Ethernet ports and link speed, configurable to 10G or 25G. If fewer cameras are used, the lane numbers for undefined cameras will be ignored. For example, if the number of cameras is 1, the lane number values set for cameras 2, 3, and 4 will be ignored.

The steps to update the platform design constraints include:

- Pin assignment at the top level of the HDL design
- Defining timing constraints

Proper configuration of these constraints is essential to produce intended reference design. However, the PDC file template provided with the reference design allows users to choose 1, 2, or 4 camera sensors. If more camera sensors are required, users must manually add the desired settings.

4.1.3.1. Pin Assignment for MIPI CSI-2 Camera Sensor Interface

In this section, the focus is solely on the MIPI CSI-2 camera sensor interface. The pins that need to be updated at the HDL top level are the camera MIPI clock lane, camera MIPI data lane, camera sensor reset, and camera I2C control. Special attention is required for the MIPI data lane assignment due to the use of two-dimensional array coding method at the HDL top-level design.

MIPI clock and data lanes are differential signals, and the pins assigned to them must be high-speed differential I/O types. For Avant-X FPGAs, the typical I/O type used for MIPI clock and data lanes is LVDS (Low Voltage Differential Signaling) I/O pairs. Special handling is required when setting pin assignments for MIPI data lanes, as the reference design's top level uses a two-dimensional array coding method. This affects how the assignments are defined and mapped in PDC file. Table 4.2 illustrates the correct pin assignment approach under these conditions in the PDC file.

Table 4.2. PDC Pin Assignment for 2-Dimension Array for MIPI Data Lane

Camera	System Verilog pin name	PDC mapped pin name
Camera 0	mipi_cam_data_p[0][0]	mipi_cam_data_p[0]
	mipi_cam_data_n[0][0]	mipi_cam_data_n[0]
	mipi_cam_data_p[0][1]	mipi_cam_data_p[1]
	mipi_cam_data_n[0][1]	mipi_cam_data_n[1]
	mipi_cam_data_p[0][2]	mipi_cam_data_p[2]
	mipi_cam_data_n[0][2]	mipi_cam_data_n[2]
	mipi_cam_data_p[0][3]	mipi_cam_data_p[3]
	mipi_cam_data_n[0][3]	mipi_cam_data_n[3]
Camera 1	mipi_cam_data_p[1][0]	mipi_cam_data_p[4]
	mipi_cam_data_n[1][0]	mipi_cam_data_n[4]
	mipi_cam_data_p[1][1]	mipi_cam_data_p[5]
	mipi_cam_data_n[1][1]	mipi_cam_data_n[5]
	mipi_cam_data_p[1][2]	mipi_cam_data_p[6]
	mipi_cam_data_n[1][2]	mipi_cam_data_n[6]
	mipi_cam_data_p[1][3]	mipi_cam_data_p[7]
	mipi_cam_data_n[1][3]	mipi_cam_data_n[7]
Camera 2	mipi_cam_data_p[2][0]	mipi_cam_data_p[8]
	mipi_cam_data_n[2][0]	mipi_cam_data_n[8]
	mipi_cam_data_p[2][1]	mipi_cam_data_p[9]
	mipi_cam_data_n[2][1]	mipi_cam_data_n[9]
	mipi_cam_data_p[2][2]	mipi_cam_data_p[10]
	mipi_cam_data_n[2][2]	mipi_cam_data_n[10]
	mipi_cam_data_p[2][3]	mipi_cam_data_p[11]
	mipi_cam_data_n[2][3]	mipi_cam_data_n[11]

Camera	System Verilog pin name	PDC mapped pin name
Camera 3	mipi_cam_data_p[3][0]	mipi_cam_data_p[12]
	mipi_cam_data_n[3][0]	mipi_cam_data_n[12]
	mipi_cam_data_p[3][1]	mipi_cam_data_p[13]
	mipi_cam_data_n[3][1]	mipi_cam_data_n[13]
	mipi_cam_data_p[3][2]	mipi_cam_data_p[14]
	mipi_cam_data_n[3][2]	mipi_cam_data_n[14]
	mipi_cam_data_p[3][3]	mipi_cam_data_p[15]
	mipi_cam_data_n[3][3]	mipi_cam_data_n[15]

4.1.3.2. Timing constraint for MIPI CSI-2 Camera Sensor Interface

Using the PDC template from reference design, you can configure the timing constraint for the MIPI CSI-2 camera sensor interface by assigning the MIPI lane rate, as shown in [Figure 4.7](#). In the PDC file, this value will be used to assign the timing constraint required for the MIPI clock input.

4.1.4. Driver Configuration/patches

Driver configuration is modified based on the target reference design. For example, each camera sensor has its own I2C control signals, so the driver must be modified to correctly identify and communicate with the target sensor. This ensures successful initialization and operation of the camera.

Driver configuration support for IMX258 is specifically covered in the [Applying Patch to Support the IMX258 Camera Module](#) section. To enable the driver configuration support, follow the steps from the [Configuring the AGX Orin Developer Host Kit](#) section through the [Applying Patch to Support the IMX258 Camera Module](#) section.

4.1.5. Verifying Reference Design Configuration

You are expected to verify whether the configured setting delivers the target reference design. There are two steps required for you to verify: first, check the Lattice Radiant software's hierarchy list to confirm the selected camera number and camera configuration. Secondly, you need to check the clock summary details in the timing analysis report to ensure the assigned timing constraint matches the target configuration. [Figure 4.8](#) shows a screenshot of the reference design implemented on the Avant-X Versa Evaluation Board. If the verified design is not the target reference design, then you are required to review the HDL parameters, DEFINE switch configuration, and PDC configuration, following the configuration flow shown in [Figure 4.1](#).

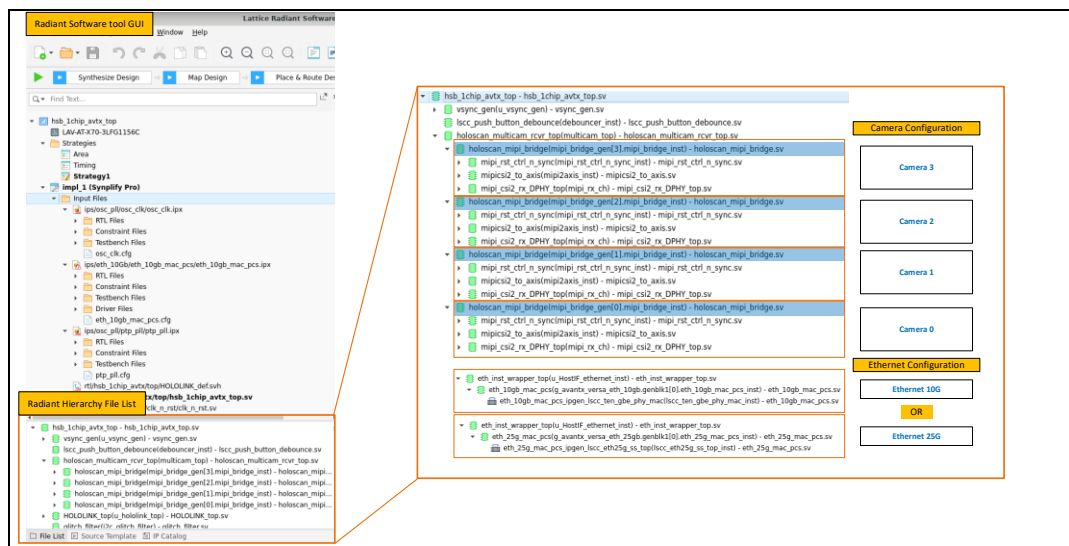


Figure 4.8. Screenshot of Lattice Radiant Software Hierarchy File List

4.2. Customizing Reference Design to Fit into Avant-X Versa Evaluation Board

Figure 4.9 shows an overview of the configured Avant-X Versa Evaluation board block diagram.

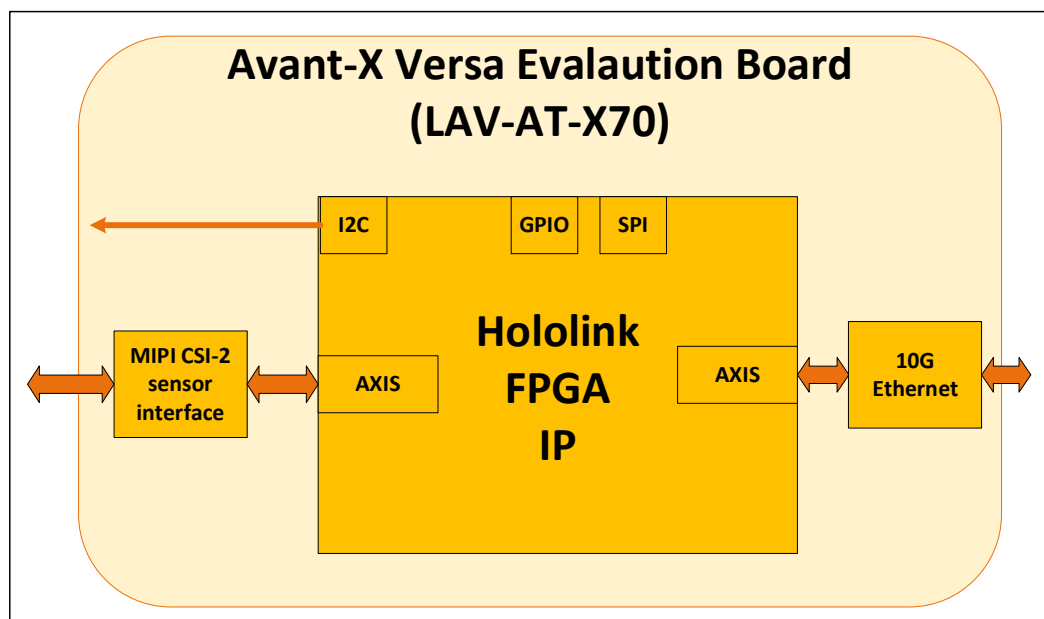


Figure 4.9. Avant-X Versa Evaluation Board Block Diagram

Table 4.3 shows the configuration required for the reference design to fit onto the Avant-X Versa Evaluation Board.

Table 4.3. Configuration required for reference design to fit into Avant-X Versa Evaluation Board

	Features	Configuration
Camera sensor interface	Number of camera sensors	1
	Camera 0: MIPI lane number	4
	Camera 0: MIPI lane rate	720 Mbps
Ethernet Link	Number of Ethernet port	1
	Ethernet link speed	10G

To customize the reference design, follow the steps below.

Note: This reference design is already integrated with a preset MIPI RX DPHY IP configuration, latest Hololink IP version 2507 and Ethernet IPs.

1. Configure HDL Parameter and DEFINE Switch.

The reference design need to be configured by changing the settings of the HDL parameter and DEFINE switch to meet the Avant-X Versa board requirement using this file.

```
<project_name>/radiant/rtl/hsb_1chip_antx/top/HOLOLINK_def.svh
```



Figure 4.10. Required HDL Parameter and DEFINE Switch Configuration

- Review the PDC configuration file.

Figure 4.11 shows the screenshot of the required LDC configuration. Figure 4.12 shows a screenshot of the required PDC configuration.

<project_name>/radiant/pdc/hsb_grd_avtx_versa_lfg1156.ldc
<project_name>/radiant/pdc/hsb_grd_avtx_versa_lfg1156.pdc

```

1
2 set ETH_NUM 1
3
4 ldc_set_location -site {MPQ6_REFCLKP} [get_ports eth_refclk_p]
5 ldc_set_location -site {MPQ6_REFCLKN} [get_ports eth_refclk_n]
6 ldc_set_location -site {MPQ6_RX0N} [get_ports {eth_rxd_n[0]}]
7 ldc_set_location -site {MPQ6_RX0P} [get_ports {eth_rxd_p[0]}]
8 ldc_set_location -site {MPQ6_TX0N} [get_ports {eth_txd_n[0]}]
9 ldc_set_location -site {MPQ6_TX0P} [get_ports {eth_txd_p[0]}]
10 if ({ETH_NUM == 2}) {
11 ldc_set_location -site {MPQ6_RX1N} [get_ports {eth_rxd_n[1]}]
12 ldc_set_location -site {MPQ6_RX1P} [get_ports {eth_rxd_p[1]}]
13 ldc_set_location -site {MPQ6_TX1N} [get_ports {eth_txd_n[1]}]
14 ldc_set_location -site {MPQ6_TX1P} [get_ports {eth_txd_p[1]}]
15 }
16

```

Number of Ethernet = 1

Figure 4.11. Required LDC Configuration

Figure 4.12. Required PDC Configuration

3. Configure the driver: For details on how to configure the driver, refer to the [Applying Patch to Support the IMX258 Camera Module](#) section. To enable driver configuration support, follow the steps from the [Configuring the AGX Orin Developer Host Kit](#) section through the [Applying Patch to Support the IMX258 Camera Module](#) section.
4. Verify the reference design configuration: Review the Lattice Radiant software hierarchy file list and the clock summary from the place-and-route timing report. [Figure 4.13](#) shows the reference design in the Lattice Radiant software hierarchy file list. The reference design is now ready for compilation and implementation.



5. Compiling Reference Design

This section describes how to compile the reference design using Lattice Radiant software. For more details on the Lattice Radiant software, please refer to the [Lattice Radiant Software User Guide](#).

5.1. Configuring the Reference Design Parameters

To configure the reference design parameters, refer to the details in the [Customizing the Reference Design](#) section.

5.2. Assigning a Revision for each Bitstream

To assign a revision ID for each bitstream modify the reference design HDL top-level file, *hsb_1chip_avtx_top.sv* as shown in [Figure 5.1](#).

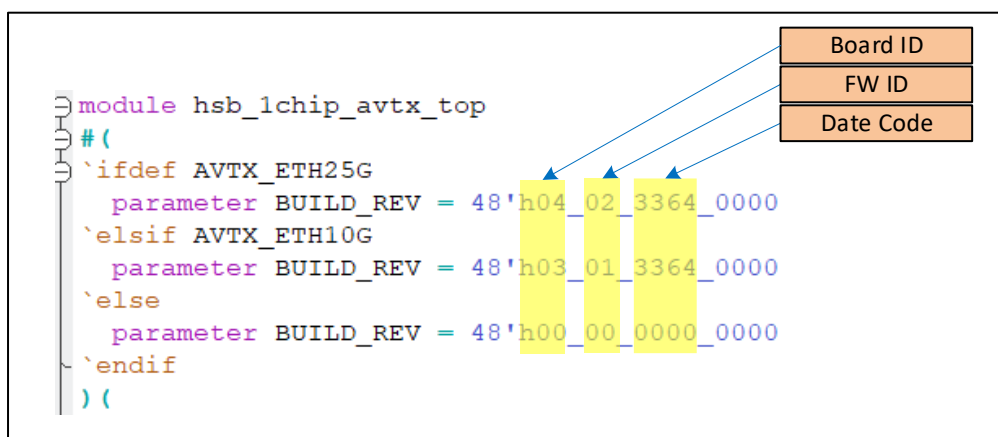


Figure 5.1. Revision ID assignment in *hsb_1chip_avtx_top.sv*

[Table 5.1](#) shows the board ID and firmware ID in hexadecimal format.

Table 5.1. Revision ID's Board ID and FW ID Representation

Reference design with Avant-X Device	Reference Design with 10G Ethernet	Reference Design with 25G Ethernet	Remarks
Board ID (in Hexadecimal)	03	04	Board ID used for Avant-X device with ethernet link 10G or 25G
FW ID (in Hexadecimal)	01	02	FW ID used for FW upgrade that has code change (design integration, bug fix or new feature)

The date code refers to the date used to generate the release bitstream. The date code is represented differently, as shown in [Figure 5.2](#). The example in the figure illustrates the conversion of the date 4th November 2025 from decimal to binary to hexadecimal formats.

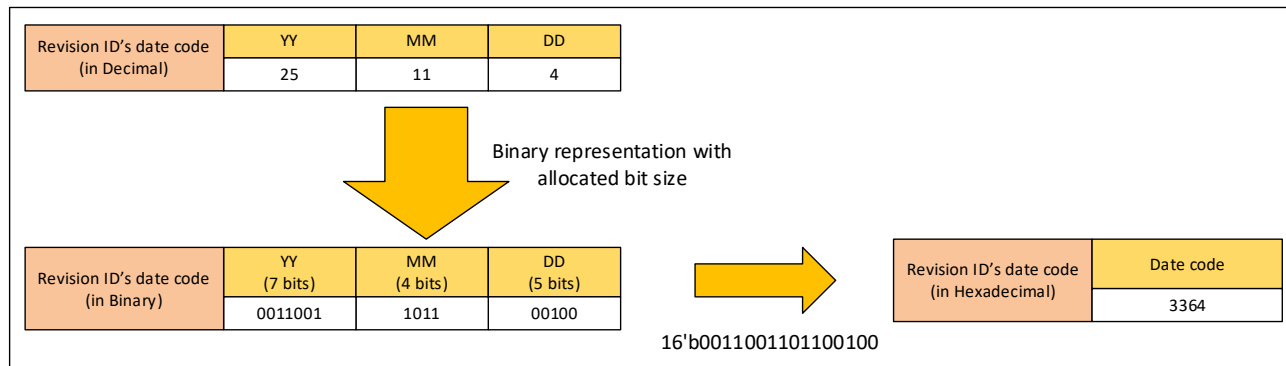


Figure 5.2. Revision ID Date Code Representation

5.3. Configuring the Lattice Radiant Software to Compile the Reference Design

1. Launch the Lattice Radiant software, as shown in Figure 5.3. Note that the project is compiled using the Lattice Radiant software version 2025.1.0.39.0

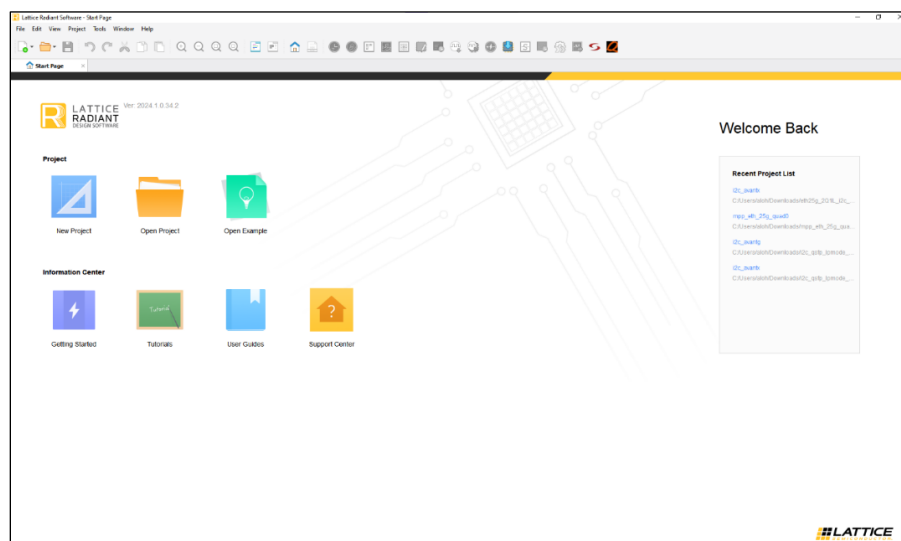


Figure 5.3. Lattice Radiant Software

2. Click **File > Open Project**. From the project database, open the Lattice Radiant software project file (*hsb_1chip_avtx_versa.rdf*), as shown in Figure 5.4.

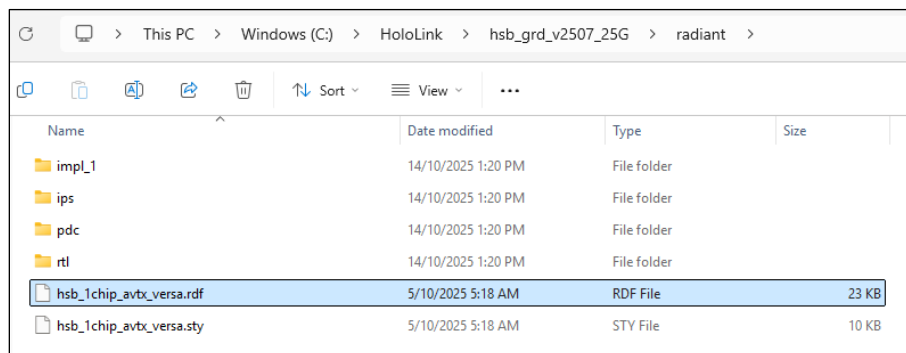


Figure 5.4. Open Project File

3. Modify the Synplify Pro strategy details under **Synthesis Design > Synplify Pro**. Refer to [Figure 5.5](#).

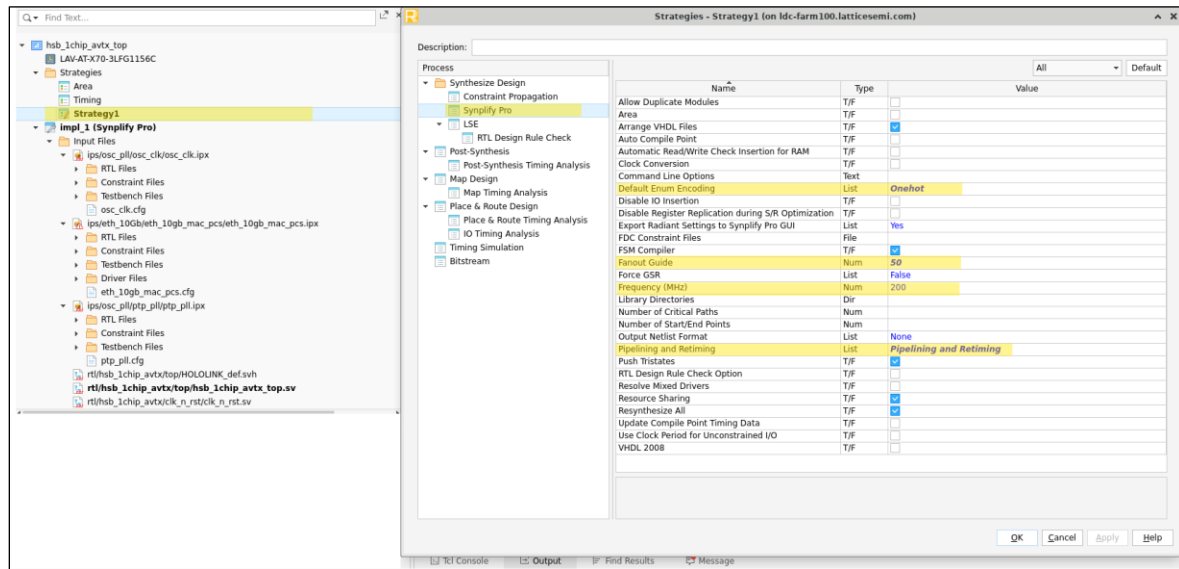


Figure 5.5. Synthesis Design's Strategy

4. Modify the Place and Route design strategy details under **Strategy1 > Place & Route Design**. Refer to [Figure 5.6](#). The seed run count has been increased to 10 for this reference design, allowing you to select the reference design with the best place-and-route result and the best STA report. Specify multiple seeds for placement and routing during implementation.

Note: This is controlled by the Placement Iteration setting under the Place and Route Design strategy in the Lattice Radiant software, which determines how many placement and routing iterations are performed. Each iteration uses a different cost table, resulting in a unique placement strategy and generating a distinct Uniform Database (.udb) file. By exploring multiple placement options, you increase the likelihood of achieving better timing closure and overall design performance. Using multiple seeds is beneficial for complex designs as it provides alternative implementations that may meet timing more effectively.

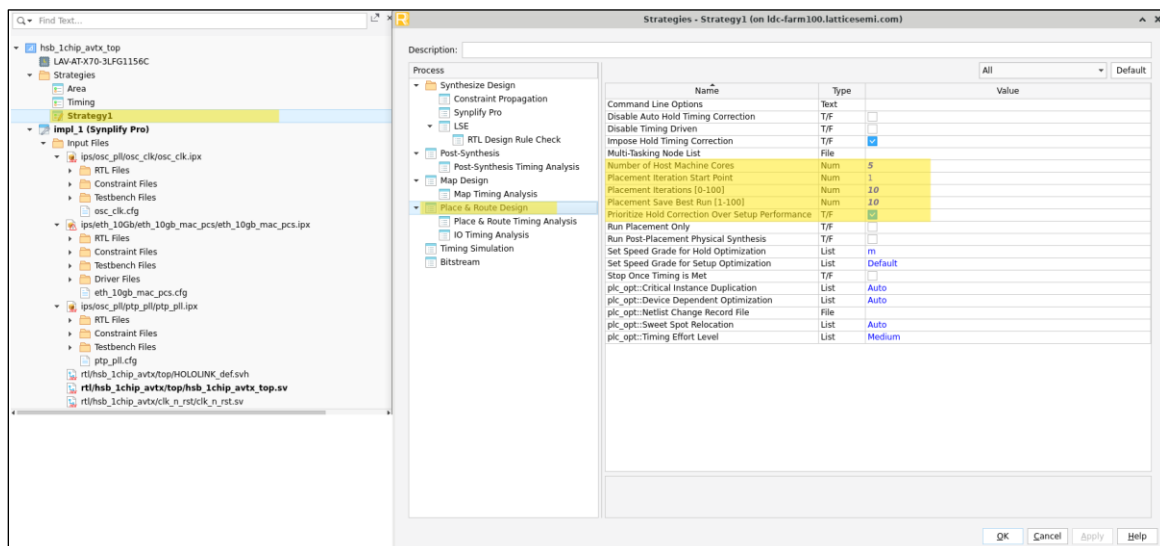


Figure 5.6. Place and Route Design's Strategy

For further details on configuring Lattice Radiant Software, refer to the [Lattice Radiant User Guide 2025.1](#).

5.4. Generating the Bitstream File

To create the FPGA bitstream file, click **Export Files** to generate the bit file. View the log message in the Export Reports folder for the generated bitstream.

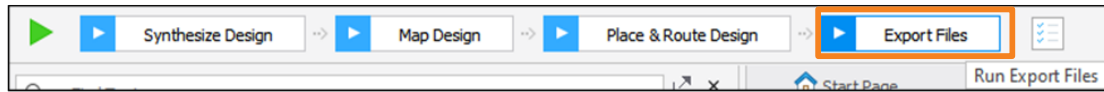


Figure 5.7. Generate and Export Bitstream File

6. Implementing the Reference Design on the Avant-X Versa Board

6.1. Requirements

6.1.1. Hardware

- [NVIDIA](#) Jetson AGX Orin Developer Kit
- [Lattice Avant-X Versa Board](#)
- IMX258 Camera Sensor Module – contact [Lattice Sales](#) for more information
- Ethernet 10GBase-T (Cat 6 RJ-45) SFP+ Module (tested with [6COM](#) 6C-SFP+-T Compatible 10GBASE-T SFP+ Copper RJ-45 30m Optical Transceiver Module)
- 25G SFP28 Optical Transceiver Module (tested with [FS](#) 25GBASE-SR SFP28 850nm 100m DOM Duplex LC/UPC MMF Optical Transceiver Module for FS Switches)
- CAT6 Ethernet cable (support 10G)
- Fiber Optic cable (support 25G)
- Type-C USB Cable
- DisplayPort Cable
- Monitor with DisplayPort support (for AGX Orin)
- Keyboard (for AGX Orin)
- Mouse (for AGX Orin)
- Mini USB Type-A cable for programming
- 12 V Power Supply
- Host Orin AGX power adapter
- Gigabit Ethernet Switch (tested with [MikroTik](#) CRS510-8XS-2XQ-IN)

The additional camera power jumper connector (J22) should be set to the 1.2 V option, as illustrated in [Figure 6.1](#). This configuration is intended for the IMX258 camera, which supports switching between 1.0 V and 1.2 V, depending on the specific camera model connected.

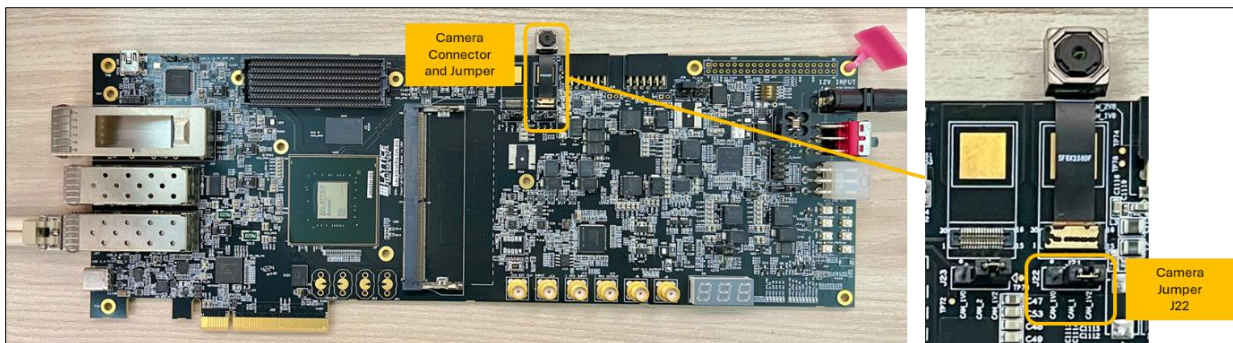


Figure 6.1. Avant-X Versa Board Camera Connector and Jumper

Figure 6.2 shows the hardware setup for the Jetson AGX Orin host and the Lattice Avant-X Versa Board used in the 10G Ethernet Reference Design implementation.

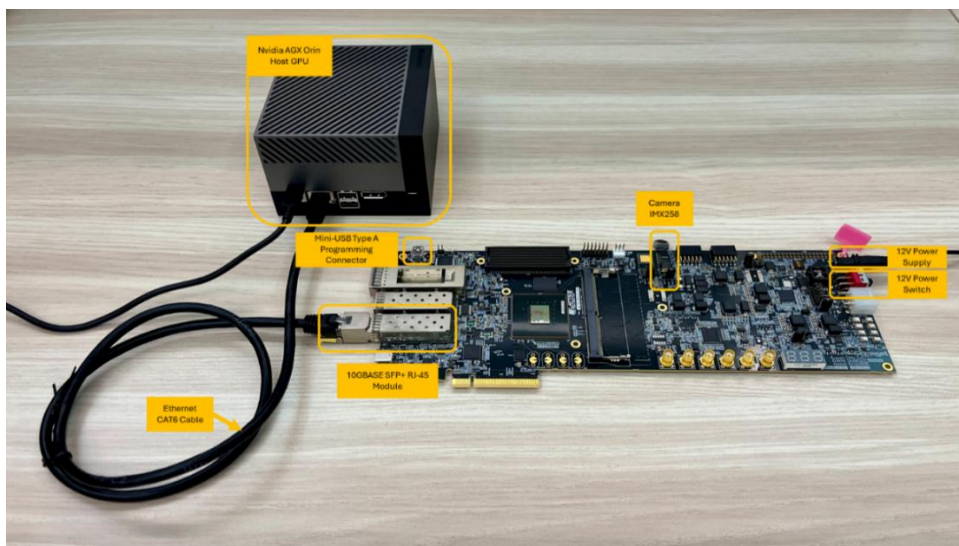


Figure 6.2. Hardware Setup to support 10G Ethernet

Figure 6.3 shows the hardware setup for the Jetson AGX Orin host and the Lattice Avant-X Versa Board used in the 25G Ethernet Reference Design implementation.

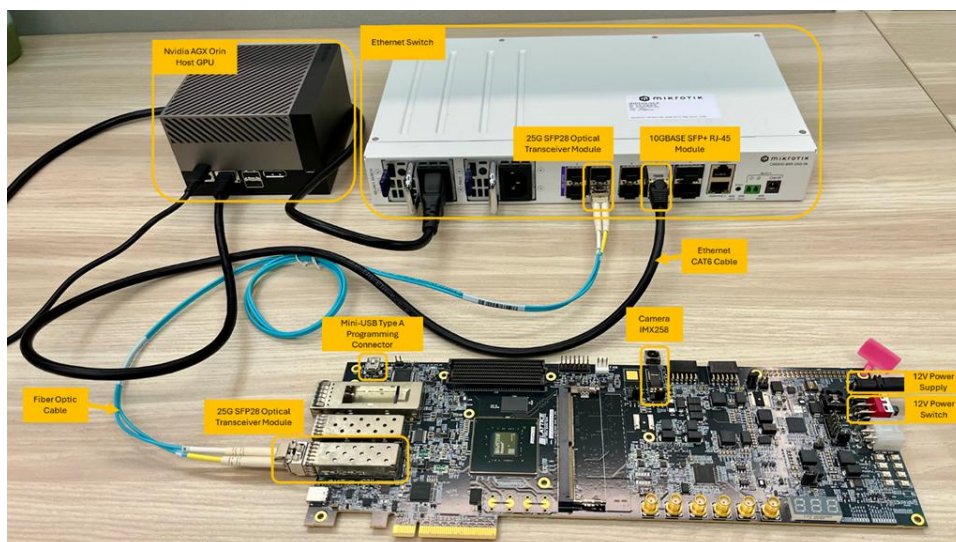


Figure 6.3. Hardware Setup to support 25G Ethernet

Note: An additional Ethernet switch is required to reduce 25 Gb traffic to 10 Gb to match the Jetson AGX Orin maximum supported bandwidth of 10 Gb. A fiber-optic cable connects the 25 Gb output from the Avant-X Versa Board's SFP cage to the Ethernet switch, while a CAT6 Ethernet cable links the switch to the Jetson AGX Orin's Ethernet port.

Be aware that additional configuration may be necessary on the Ethernet switch to ensure compatibility with both 10 Gb and 25 Gb protocols, depending on the expected input speed. A MikroTik Gigabit Ethernet switch was used in this demonstration, as shown in Figure 6.3. Users may opt for any equivalent switch that supports 25 Gb connectivity.

6.1.2. Software

- Jetpack 6.2.1
- NVIDIA Jetson Linux 36.4.4
- NVIDIA Holoscan SDK 3.3.0
- Holoscan Sensor Bridge (HSB) SDK 2.2.0

6.2. Jetson AGX ORIN Host Setup

6.2.1. Setting Up the Jetson AGX ORIN Developer Kit

To set up the Jetson AGX Orin Developer Kit, follow the steps below. These steps are to be executed on the Ubuntu host PC terminal.

1. Set up an Ubuntu 22.04 host PC with at least 8 GB of RAM and an internet connection. Connect the Ubuntu host to the Jetson AGX Orin using a USB cable as shown in Figure 6.4.

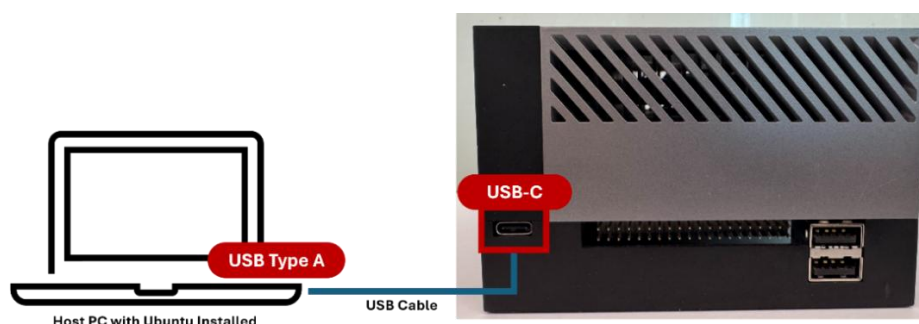


Figure 6.4. Ubuntu Host PC and Jetson AGX Orin Developer Kit Setup

2. Download and install the NVIDIA SDK Manager:

```
wget https://developer.download.nvidia.com/compute/cuda/repos/ubuntu2204/x86_64/cuda-keyring_1.1-1_all.deb
sudo dpkg -i cuda-keyring_1.1-1_all.deb
sudo apt-get update
sudo apt-get -y install sdkmanager
```

3. Place the AGX Orin into recovery mode by pressing and holding the recovery button as shown in Figure 6.5. While holding the recovery button, press the reset button and release it. Wait for about three seconds or more, then release the recovery button.

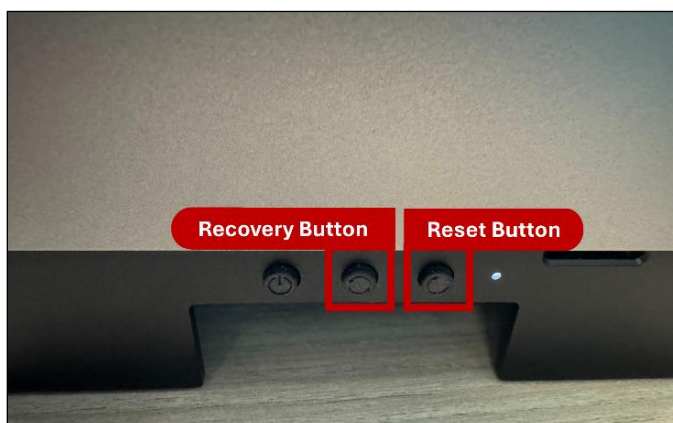


Figure 6.5. Recovery and Reset Button

- Launch SDK Manager from the terminal, type:
`sdkmanager`
- Log in using your NVIDIA developer credentials if using the SDK Manager for the first time. Select the checkbox, **Stay logged in**, then click the **LOGIN** button.
- Select **Jetson AGX Orin [64 GB Developer Kit version]** as the target hardware after the SDK Manager window appears. Then click **OK**.

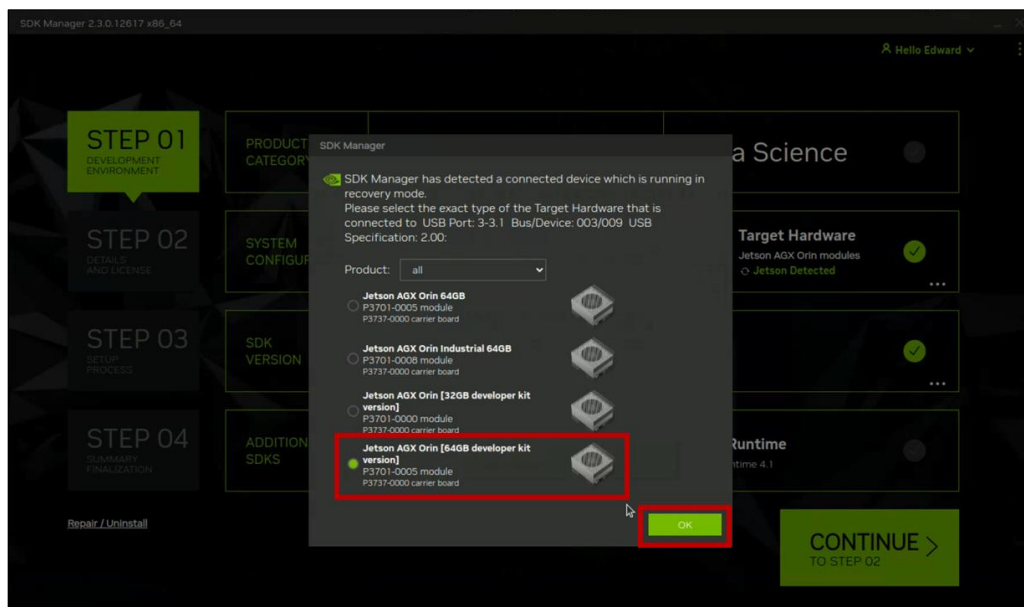


Figure 6.6. Jetson AGX Orin [64GB developer kit version]

- Click the ... icon at (A) as shown in Figure 6.7, and select **JetPack 6.2.1 (Rev. 1)**. Then, click **CONTINUE** to proceed.

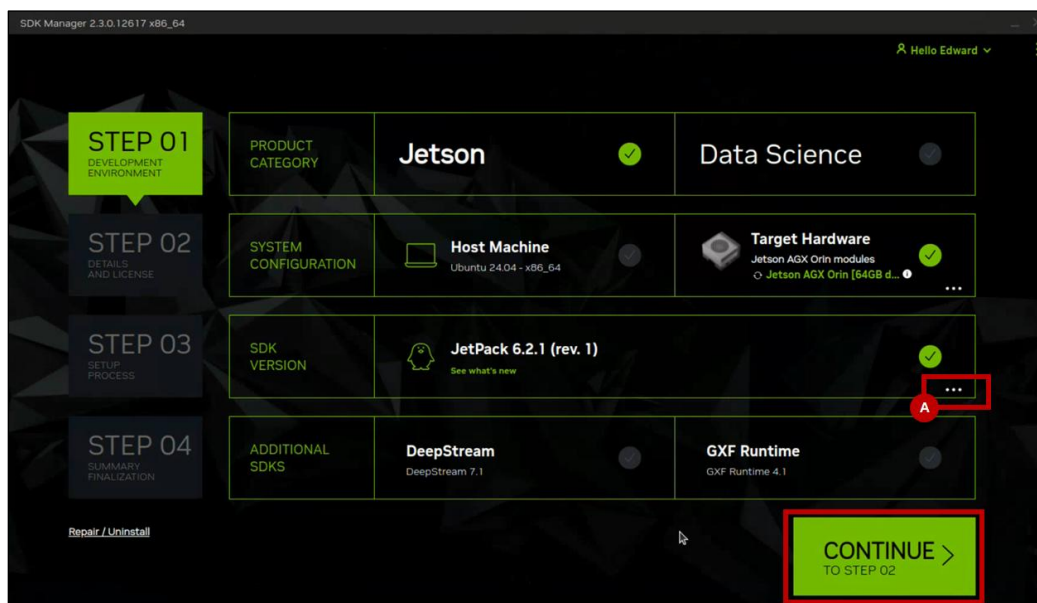


Figure 6.7. JetPack 6.2.1 (Rev.1)

8. Leave all settings as default, and select **I accept the terms and conditions of the license agreements**. Then, click **CONTINUE** to proceed with the installation process.

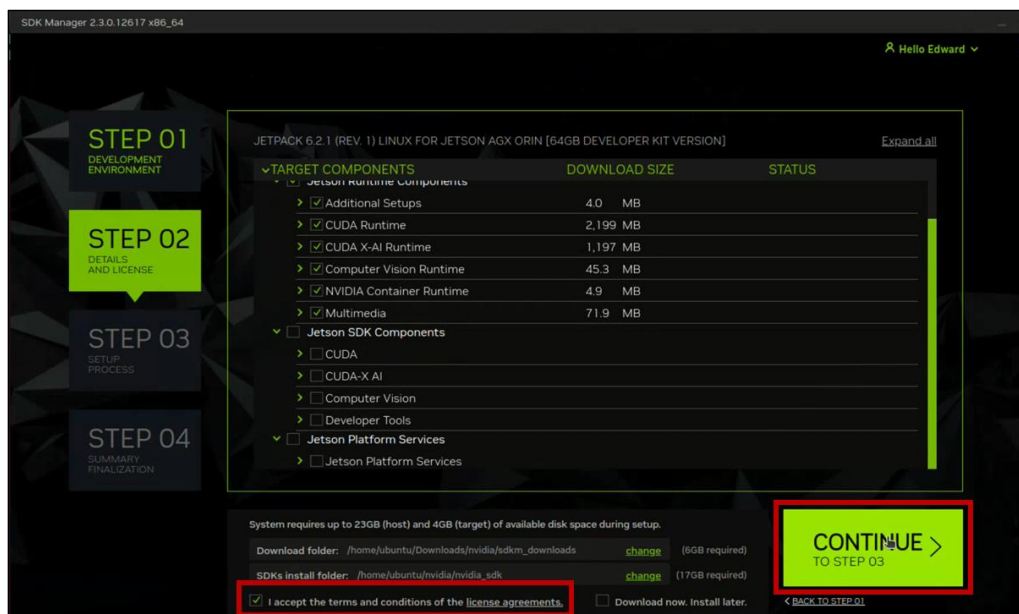


Figure 6.8. Terms and Conditions – License Agreement

9. In **STEP 03 – SETUP IN PROCESS**, as shown in Figure 6.9, wait for the download operation and OS image creation process to complete.



Figure 6.9. Download Operation and OS Image Creation

10. When prompted for the flash setup, enter the desired username to access the AGX Orin system, see letter **(A)** in [Figure 6.10](#), along with the password at **(B)**. Select **Pre-Config** from the dropdown at **(C)** and **EMMC** as the storage device at **(D)**. Then, click **Flash** to proceed.

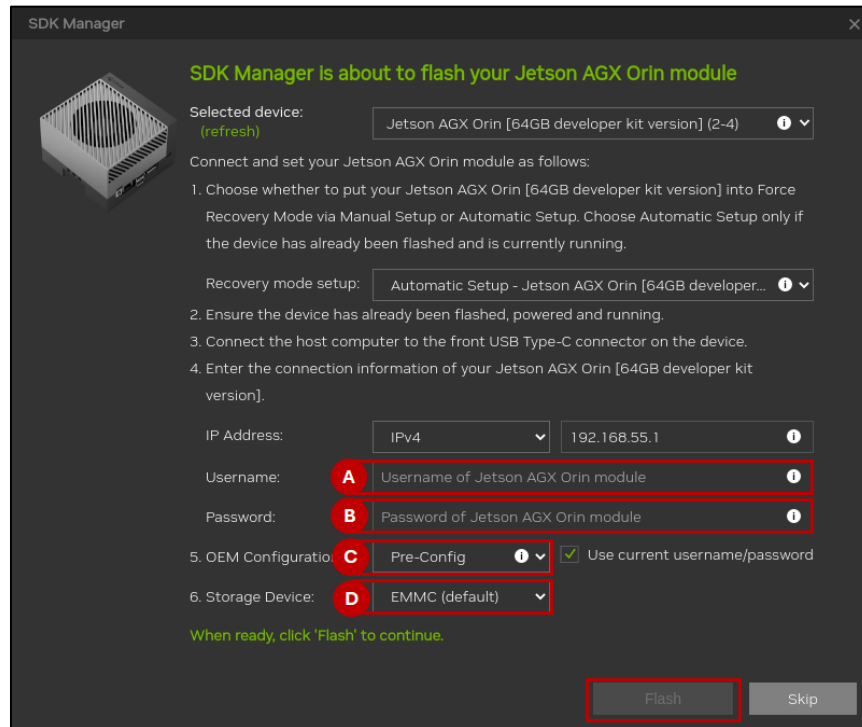


Figure 6.10. SDK Manager

11. Complete **STEP 04 – SUMMARY FINALIZATION** to finish the setup. Reset the Jetson AGX Orin system by pressing the reset button as shown in [Figure 6.4](#). Then proceed to the next section to configure the Jetson AGX Orin itself.

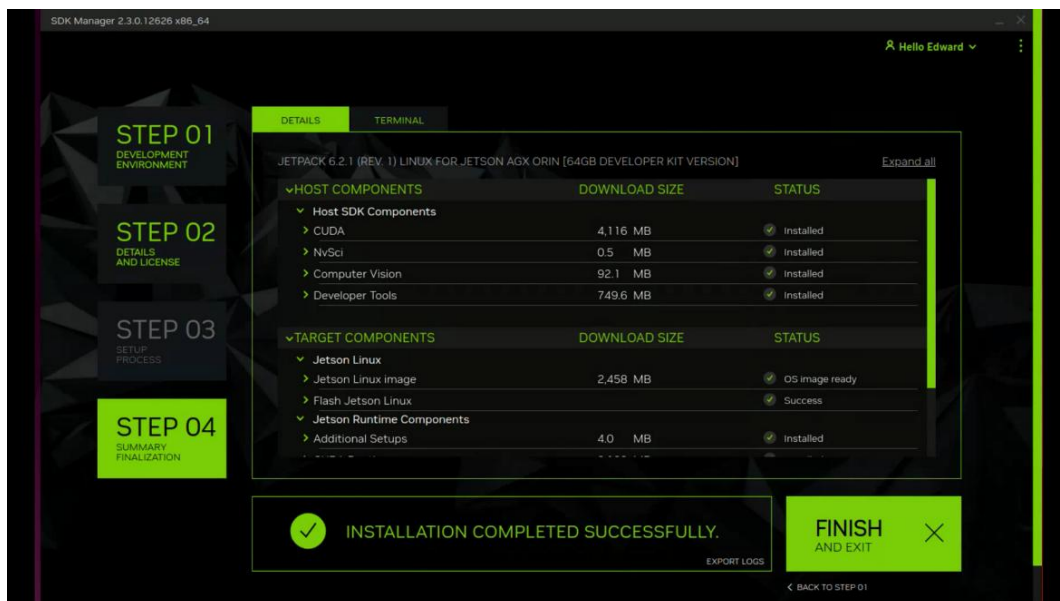


Figure 6.11. Summary Finalization

6.2.2. Configure the AGX Orin Developer Host Kit

The customizable HSB sensor interface reference design is supported by the Jetson AGX Orin system running at JetPack 6.2.1. The following steps are one-time setup procedures and should be executed directly on the AGX Orin terminal, outside the Holoscan Sensor Bridge (HSB) docker container. All commands assume the HSB is connected via eno1 (the Ethernet interface on the Jetson AGX Orin).

1. Install git-lfs (some data files in the HSB source repository use it).

```
sudo apt-get update
sudo apt-get install -y git-lfs
```

2. Grant the user permission to the docker subsystem.

```
sudo usermod -aG docker $USER
```

3. Reboot the AGX Orin to apply the changes.

```
sudo reboot
```

4. Increase the network receive buffer size to support Linux sockets.

```
echo 'net.core.rmem_max = 31326208' | sudo tee /etc/sysctl.d/52-hololink-
rmem_max.conf
sudo sysctl -p /etc/sysctl.d/52-hololink-rmem_max.conf
```

5. Assign a static IP address (192.168.0.101) to the onboard network port.

```
EN0=eno1
sudo nmcli con add con-name hololink-$EN0 ifname $EN0 type ethernet ip4
192.168.0.101/24
sudo nmcli connection up hololink-$EN0
```

6. Power on the Avant-X Versa board and ensure it is properly connected. Then, ping to check connectivity .

```
ping 192.168.0.101
```

7. Isolate a processor core from the Linux kernel when running Linux socket-based examples¹.

To isolate that core, edit the /boot/extlinux/extlinux.conf file.

```
sudo nano /boot/extlinux/extlinux.conf
```

8. Add the setting isolcpus=2 to the end of the line that begins with **APPEND**.

Your file should resemble the following:

```
TIMEOUT 30
DEFAULT primary

MENU TITLE L4T boot options

LABEL primary
    MENU LABEL primary kernel
    LINUX /boot/Image
    ...
    APPEND ${cbootargs} ...<other-settings>... isolcpus=2
```

9. Save and exit by pressing **Ctrl+O**, then **Enter**, followed by **Ctrl+X**.

The sensor bridge applications can run the network receiver process on a different core by setting the environment variable **HOLOLINK_AFFINITY** to the desired core.

For example, to run on the first processor core, type:

```
HOLOLINK_AFFINITY=0 python3 examples/linux_imx258_player.py
```

10. Run the **jetson_clocks** tool at startup to set the core clocks to their maximum.

```
JETSON_CLOCKS_SERVICE=/etc/systemd/system/jetson_clocks.service
cat <<EOF | sudo tee $JETSON_CLOCKS_SERVICE >/dev/null
[Unit]
Description=Jetson Clocks Startup
After=nvpmode1.service

[Service]
Type=oneshot
ExecStart=/usr/bin/jetson_clocks

[Install]
WantedBy=multi-user.target
EOF
sudo chmod u+x $JETSON_CLOCKS_SERVICE
sudo systemctl enable jetson_clocks.service
```

11. Set the Jetson AGX Orin power mode to **MAXN** for optimal performance. You can change this setting via the L4T power dropdown menu in the upper-right corner of the screen, as indicated by (A). Click (B) to select the **MAXN** option.

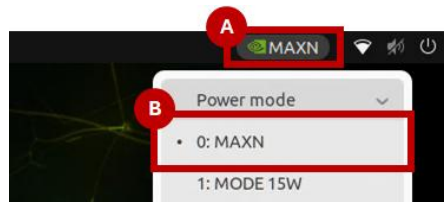


Figure 6.12. MAXN Power Mode

12. Reboot Jetson AGX Orin to apply changes.

```
sudo reboot
```

13. Enable PTP for **\$EN0** to synchronize timestamps in received data with the host system time. Install the **linuxptp** tool, then create a systemd service file to run **phc2sys** at boot time, ensuring the clock in **\$EN0** is synchronized with the system clock.

```
sudo apt update && sudo apt install -y linuxptp
EN0=en01
PHC2SYS_SERVICE=/etc/systemd/system/phc2sys-$EN0.service
cat <<EOF | sudo tee $PHC2SYS_SERVICE >/dev/null
[Unit]
Description=Copy system time to $EN0
Requires=NetworkManager.service
After=NetworkManager.service
After=timemaster.service

[Service]
Type=simple
ExecStartPre=timeout 3m bash -c "until [ \"\$(nmcli -g GENERAL.STATE device show $EN0)\"] = \"100 (connected)\" ]; do sleep 1; done"
ExecStart=/usr/sbin/phc2sys -c $EN0 -s CLOCK_REALTIME -O 0 -S 0.0001

[Install]
WantedBy=multi-user.target
EOF
```


14. Configure it for execution at startup, and start it now.

```
sudo chmod u+x $PHC2SYS_SERVICE
sudo systemctl enable phc2sys-$EN0.service
sudo systemctl start phc2sys-$EN0.service
```

15. Next, run **ptp4l** to send PTP SYNC messages to **\$EN0**.

```
cat <<EOF | sudo tee /etc/linuxptp/hsb-ntp.conf >/dev/null
# This configuration is appropriate for NVIDIA Holoscan sensor bridge
# applications, where PTP messages are sent over L2 and a 1/2 second interval.
[global]
logSyncInterval -1
logMinDelayReqInterval -1
network_transport L2
EOF
```

16. Create a systemd service to run **ptp4l**.

```
PTP4L_SERVICE=/etc/systemd/system/ptp4l-$EN0.service
cat <<EOF | sudo tee $PTP4L_SERVICE >/dev/null
[Unit]
Description=Send PTP SYNC messages to $EN0
After=phc2sys-$EN0.service

[Service]
Type=simple
ExecStart=/usr/sbin/ptp4l -i $EN0 -f /etc/linuxptp/hsb-ntp.conf

[Install]
WantedBy=multi-user.target
EOF
```

```
sudo chmod u+x $PTP4L_SERVICE
sudo systemctl enable ptp4l-$EN0.service
sudo systemctl start ptp4l-$EN0.service
```

17. Log in to NVIDIA GPU Cloud (NGC).

- Register for an NGC account at <https://catalog.ngc.nvidia.com/>
- Create an API key at <https://ngc.nvidia.com/setup/api-key>
- Use the API key to log in to **nvcr.io**

```
$ docker login nvcr.io
Username: $oauthtoken
Password: <Your token key to NGC>
WARNING! Your password will be stored unencrypted in
/home/<user>/docker/config.json.
Configure a credential helper to remove this warning. See
https://docs.docker.com/engine/reference/commandline/login/#credentials-store

Login Succeeded
```

Note:

1. For high-bandwidth applications, such as 4K video acquisition, isolate the network receiver core to ensure optimal performance. Set processor affinity for the example program to the isolated core to improve performance and reduce latency. By default, the sensor bridge software runs the time-critical background network receiver process on core 3. Ensure core 3 is isolated from Linux scheduling so that no other processes run on it without explicit user assignment, thereby improving reliability and performance.

6.2.3. Building the Holoscan Sensor Bridge Demo Container

The MIPI IMX258 camera reference design is based on the HSB release version 2.2.0-GA.

1. Fetch the HSB source code version 2.2.0 from Github:

```
git clone https://github.com/nvidia-holoscan/holoscan-sensor-bridge -b 2.2.0
```

2. Build the HSB demo container for iGPU (default for AGX Orin).

```
cd holoscan-sensor-bridge  
sh docker/build.sh --igpu
```

6.2.4. Applying Patch to Support the IMX258 Camera Module

1. Place the patch file **lattice_sensor_bridge_2.2.0.patch** in the same directory level as the **holoscan-sensor-bridge** directory.

2. Apply the patch using the following command:

```
patch -p0 < lattice_sensor_bridge_2.2.0.patch
```

3. Verify that **linux_imx258_player.py** exists after applying **lattice_sensor_bridge_2.2.0.patch** to confirm the patch was applied correctly:

```
ls holoscan-sensor-bridge/examples/linux_imx258_player.py
```

4. Rebuild the HSB demo container using the following command:

```
cd holoscan-sensor-bridge  
sh docker/build.sh --igpu
```

6.3. Testing the System

This section provides details of the reference design testing on the Avant-X Versa Evaluation Board with NVIDIA AGX ORIN GPU Host connected.

6.3.1. Programming the Bit File

This section outlines the steps for uploading the *.bit* file. Currently, the Avant-X Versa Evaluation board supports only one method for updating the reference design firmware: a local update via USB interface. This method allows you to flash the firmware directly to the board using a USB connection, independent of the Holoscan ecosystem. It is ideal for initial setup, debugging, and hands-on development. The following section provides detailed steps for uploading the *.bit* file with this USB update method.

6.3.1.1. Local Firmware Update via USB Interface

1. Connect the board to the PC using a mini-USB Type-A cable, as shown in [Figure 6.13](#). Ensure jumper **JP1** is properly connected. Connect the power adapter to the board power port and turn the switch **ON**. The board is now ready to be programmed.

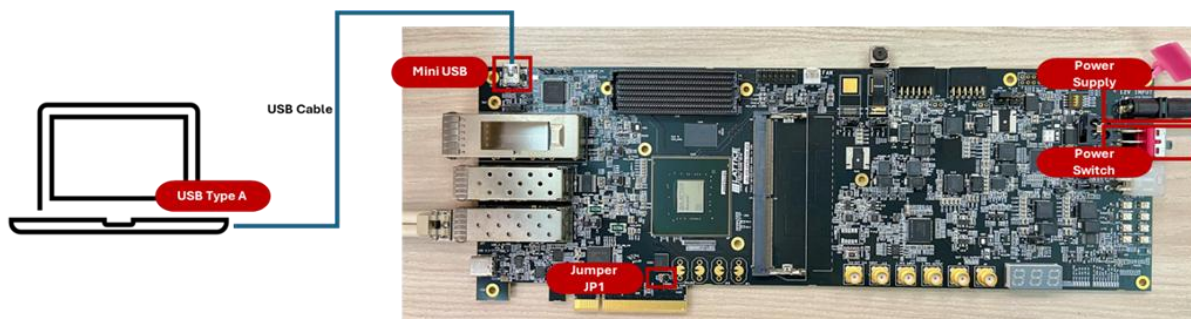



Figure 6.13. Hardware Setup for Bit File Programming

2. Click the Radiant Programmer icon () if the project is already open in the Lattice Radiant software, otherwise, launch the standalone Radiant Programmer. Enter the **Project Location**, **Project Name**, then click **OK**.

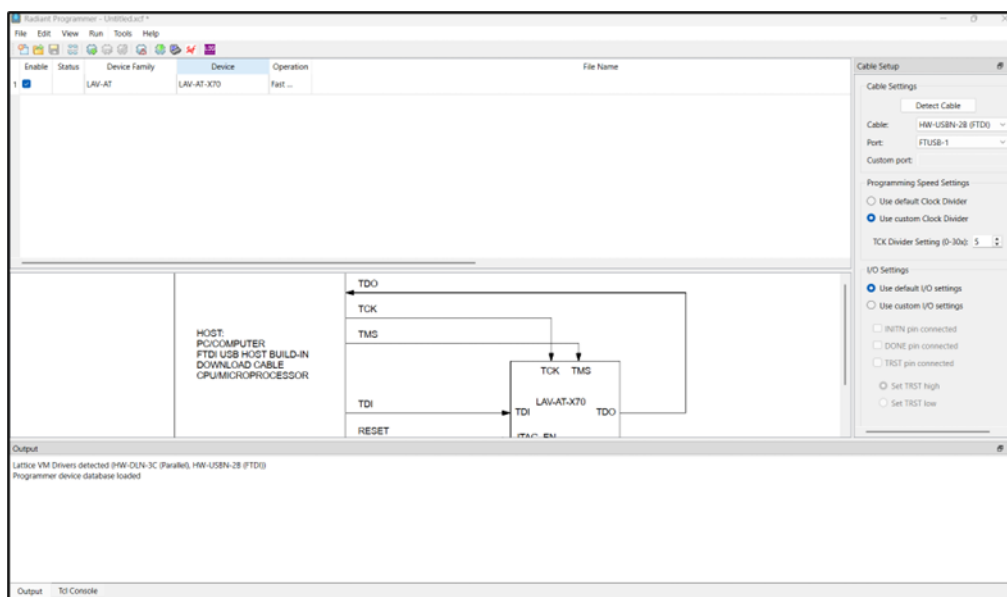


Figure 6.14. Radiant Programmer Window

- Click **Detect Cable** in the cable setup section, select **FTUSB-1**. Then click **OK** to proceed.

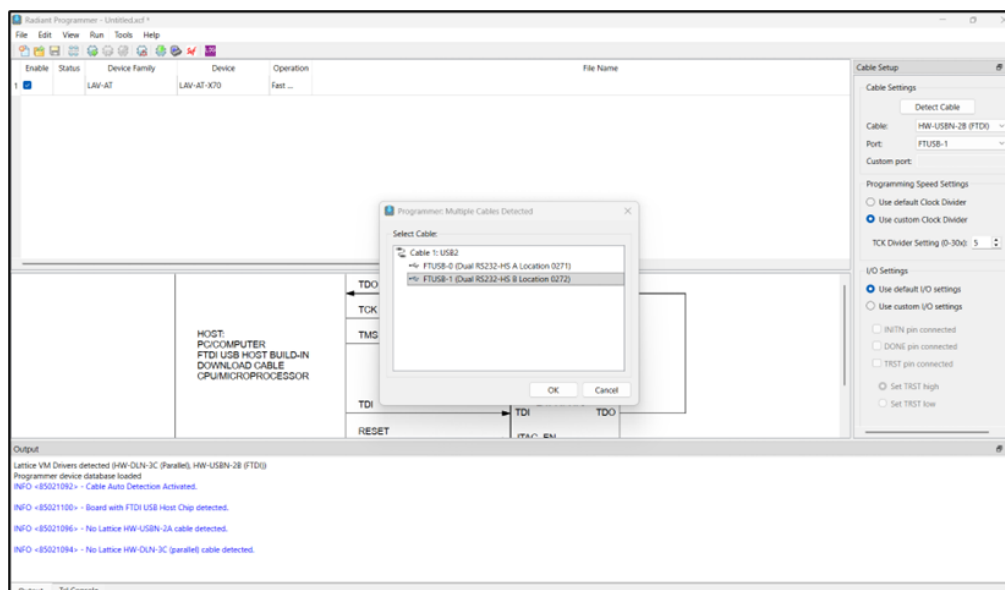


Figure 6.15. Select Cable Settings

- Select the appropriate SPI flash configuration to flash directly to external SPI flash. Refer to Figure 6.16 for the expected settings. Click the ... button under the file name bar and choose the bitstream file to program.

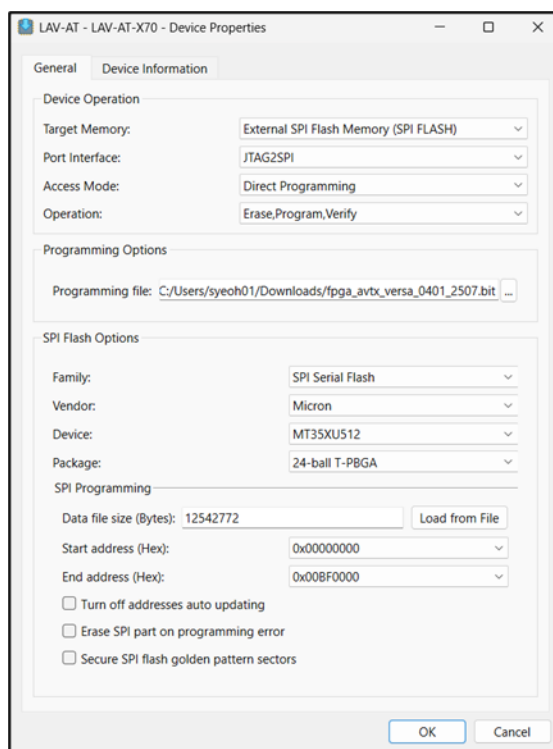


Figure 6.16. Load Bitstream File

- Click the **Program Device** toolbar icon to load the bitstream into the board, as shown in Figure 6.17.



Figure 6.17. Program Device Toolbar Icon

- Verify that the programming status is **Operation: successful** in the output window, as shown in Figure 6.18.
To activate the flashed bitstream, power OFF the Avant-X Versa Evaluation board, then disconnect **JP1** before power ON the Avant-X Versa Evaluation board.

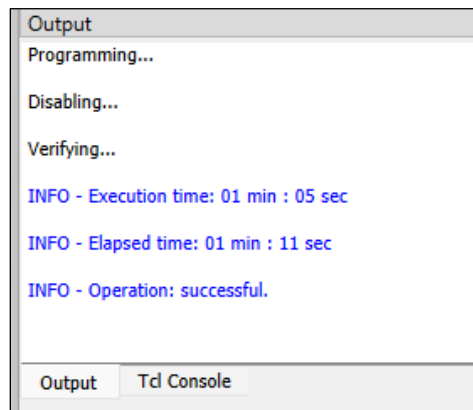


Figure 6.18. Message on Successful Programming

6.3.2. Camera Video Streaming Test

- Run the Holoscan Sensor Bridge demo container.

```
cd /<path>/<to>/<holoscan-sensor-bridge>  
xhost +  
sh docker/demo.sh
```

- Run the camera video streaming example.

This example will be streaming from the camera and display the video on AGX Orin.

Note: Once Step 1 is executed in the AGX Orin terminal, the demo container starts, the command prompt will switch to the environment inside the container.

- Run the video streaming demo for IMX258 camera using the following command.

- When using 10G or 25G Ethernet:

```
python examples/linux_imx258_player.py
```

7. Resource Utilization

This section shows the resource utilization of the reference design for the Avant-X FPGA (LAV-AT-X70-3LFG1156C) device using the Synplify Pro tool in the Lattice Radiant software version 2025.1.0.39.0. Refer to the [Compiling the Reference Design](#) section for configuration details. Note that changes in the design attributes may affect resource utilization, and values may vary over time due to feature updates, bug fixes, and other modifications.

Note: Resource utilization may change over time due to reference design feature updates, bug fixes, and other factors.

7.1. Resource Utilization with Ethernet 10G

[Table 7.1](#) shows one camera interface configured with four MIPI lanes at 720 Mbps, paired with a single-port 10G Ethernet host interface.

Table 7.1. Logic Consumption for each instance Available in the Reference Design

Instance name	LUT4 Logic	LUT4 Distributed RAM	LUT4 Ripple Logic	PFU Registers	DSP MULT	EBR
multicam_top (1x camera sensor interface)	1900	0	290	1541	0	8
Hololink_top (Hololink IP)	17984	2028	2766	24623	2	19
Ethernet_inst (Ethernet 10G- host interface)	4614	0	190	3913	0	2
Clk_rst	75	0	28	115	0	0
Miscellaneous	273	48	142	752	0	0
Total	24846	2076	3416	30944	2	29

Note: Other submodules are categorized as miscellaneous in this table.

[Table 7.2](#) compares the reference design logic consumption with available resources of Avant-X (LAV-AT-X70-3LFG1156C) device, based on the configuration described in [Table 7.1](#).

Table 7.2. Comparison between Reference Design Utilization and LAV-AT-X70 Resources Available

	LUT	PFU registers	DSP Mult	EBR
Avant LAV-AT-X70 device logic resource	397,440	397,440	1,800	990
Reference design logic resource consumed	30338	30944	2	29
Reference design logic resource consumed (%)	7.63	7.79	0.11	2.93

7.2. Resource Utilization with Ethernet 25G

Table 7.3 shows one camera sensor interface configured with four MIPI lanes at a lane rate of 720 Mbps, and a single-port 25G Ethernet host interface.

Table 7.3. Logic Consumption for each Instance Available in the Reference Design

Instance name	LUT4 Logic	LUT4 Distributed RAM	LUT4 Ripple Logic	PFU Registers	DSP MULT	EBR
multicam_top (1x camera sensor interface)	1891	0	290	1541	0	8
Hololink_top (Hololink IP)	21,413	2028	2722	27870	2	21
Ethernet_inst (Ethernet 25G- host interface)	10,311	0	264	7,619	0	4
Clk_rst	79	0	28	114	0	0
Miscellaneous	273	48	142	704	0	0
Total	33967	2076	3446	37848	2	33

Note: Other submodules are categorized as miscellaneous in this table.

Table 7.4 compares the reference design logic consumption with the available resources of the Avant-X (LAV-AT-X70-3LFG1156C) device, based on the configuration described in Table 7.3.

Table 7.4. Comparison between Reference Design Utilization and Avant LAV-AT-X70 Resources

	LUT	PFU registers	DSP Mult	EBR
Avant LAV-AT-X70 device logic resource	397,440	397,440	1,800	990
Reference design logic resource consumed	39,489	37848	2	33
Reference design logic resource consumed (%)	9.94	9.52	0.11	3.33

8. Debug Methodology

This section outlines the recommended steps for debugging the camera video streaming setup in the Holoscan Sensor Bridge reference design. By following this procedure, you can verify the system functionality and identify potential issues during integration and testing.

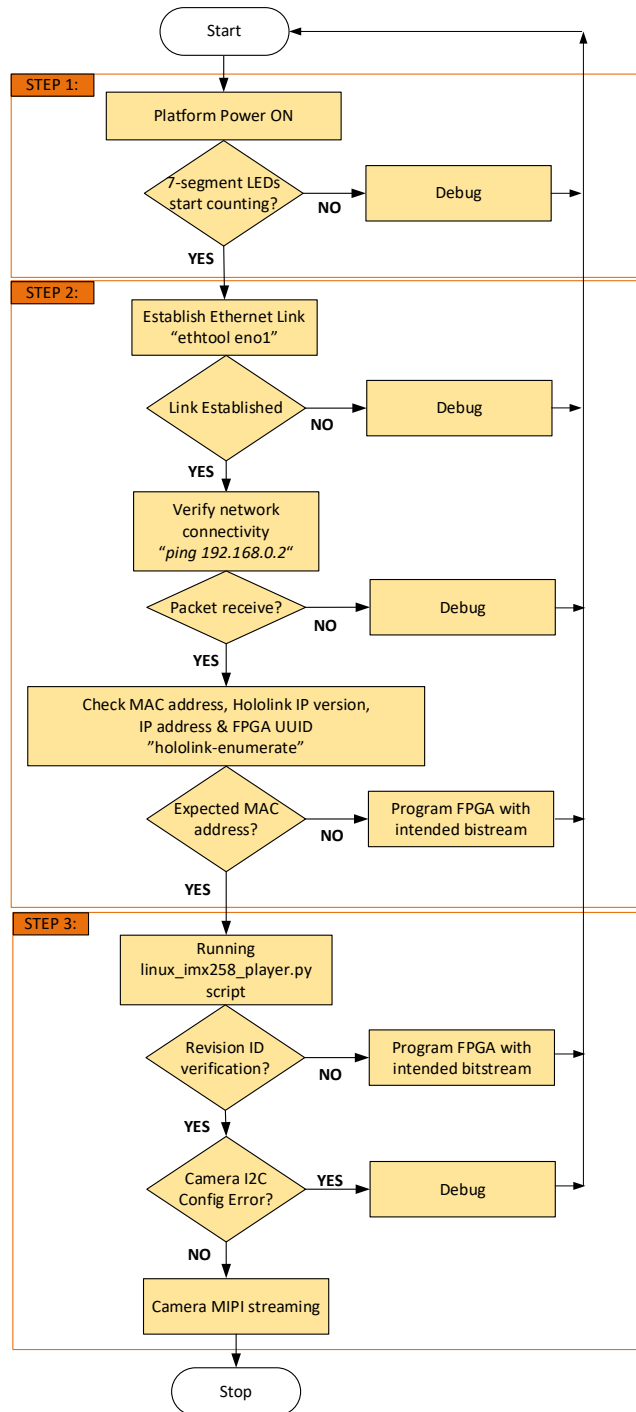


Figure 8.1. Debug Methodology Flow Chart For Reference Design

8.1. Powering Up the Evaluation Board

1. Power cycle the board after programming.

After programming the FPGA firmware into the external SPI flash, fully power down the platform, then power it back up. This power cycle ensures the FPGA correctly loads and configures the new firmware.

2. After powering up, the 7-segment display should begin counting, indicating the Ethernet link is successfully established. it also indicates that the connection is active and internal clocks are running correctly.

Note: This step assumes the HSB Docker container is already set up on the host system.

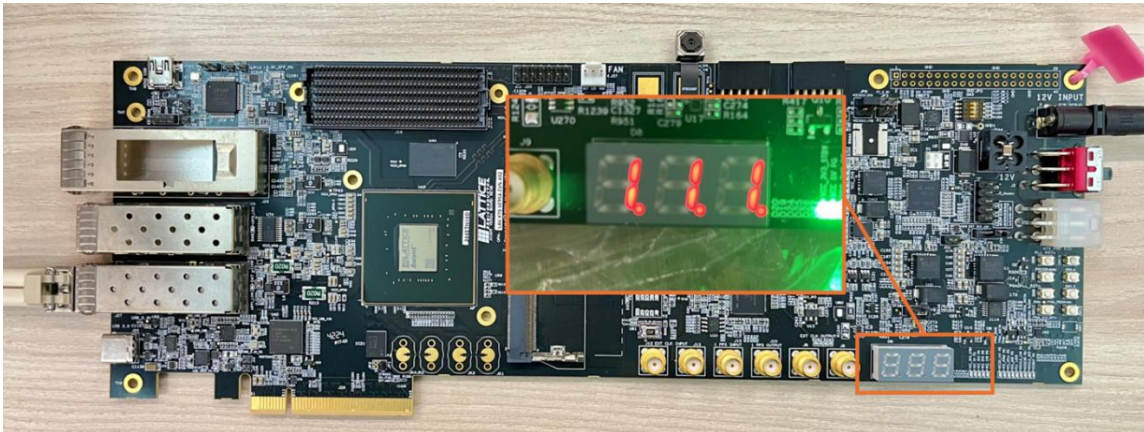


Figure 8.2. Position of the 7-segment LEDs on Avant-X Versa Evaluation Board

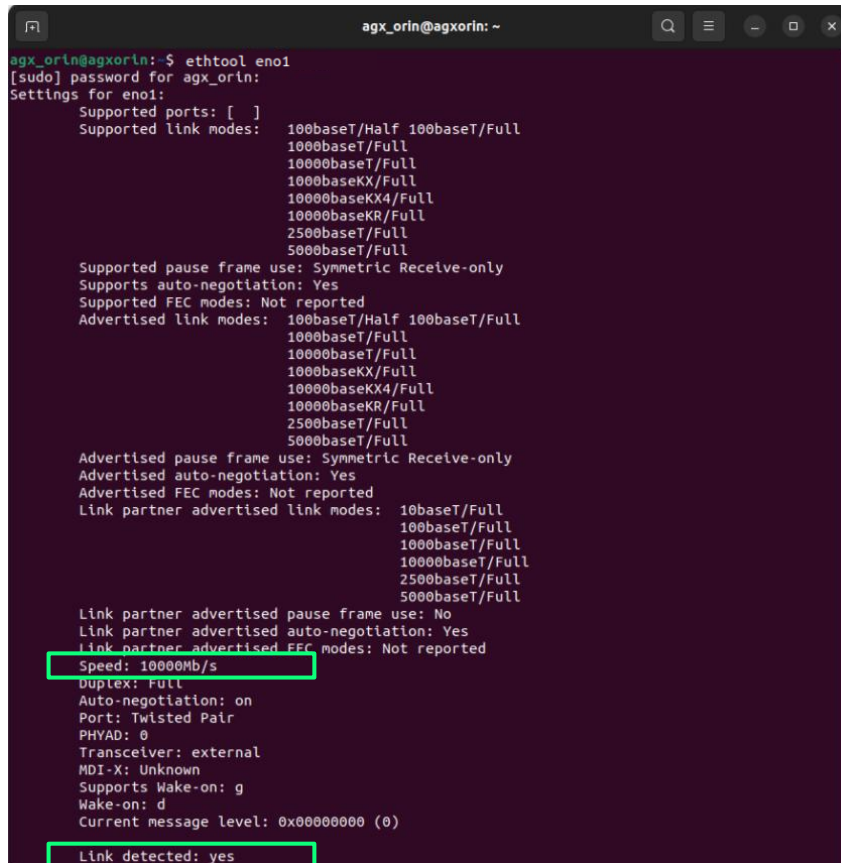
8.1.1. Troubleshooting Common Issues

- Issue A: The 7-segment LEDs are not on.
 - Workaround 1: Make sure the Avant-X Versa board's power supply is connected and the 12 V plug-in switch is turned on.
 - Workaround 2: Power the Avant-X Versa board **OFF** and **ON** using the 12 V plug-in switch.
 - Workaround 3: Reprogram the FPGA device to confirm that you are using the correct FPGA bitstream.
 - Workaround 4: If the issue persists, submit a technical support case through www.latticesemi.com/techsupport.
- Issue B: The 7-segment LEDs are not counting; the Ethernet IP may be experiencing issues.
 - Workaround 1: Regenerate the Ethernet IP with the correct configuration, then recompile and reprogram the FPGA device with the newly compiled FPGA bitstream.
 - Workaround 2: If the issue persists, submit a technical support case through www.latticesemi.com/techsupport.

8.2. Verifying the Ethernet Connection

1. Check the Ethernet link status.

On the host terminal, run `ethtool eno1` command. This verifies whether the Ethernet link is established, and confirms that the link speed is as expected. If successful, the terminal will display the link status, as shown in [Figure 8.3](#).



```
agx_orin@agx_orin: ~  
agx_orin@agx_orin:~$ ethtool eno1  
[sudo] password for agx_orin:  
Settings for eno1:  
Supported ports: [ ]  
Supported link modes: 100baseT/Half 100baseT/Full  
1000baseT/Full  
1000baseT/Full  
1000baseKX/Full  
1000baseKX4/Full  
1000baseKR/Full  
2500baseT/Full  
5000baseT/Full  
Supported pause frame use: Symmetric Receive-only  
Supports auto-negotiation: Yes  
Supported FEC modes: Not reported  
Advertised link modes: 100baseT/Half 100baseT/Full  
1000baseT/Full  
1000baseT/Full  
1000baseKX/Full  
1000baseKX4/Full  
1000baseKR/Full  
2500baseT/Full  
5000baseT/Full  
Advertised pause frame use: Symmetric Receive-only  
Advertised auto-negotiation: Yes  
Advertised FEC modes: Not reported  
Link partner advertised link modes: 10baseT/Full  
100baseT/Full  
1000baseT/Full  
1000baseT/Full  
2500baseT/Full  
5000baseT/Full  
Link partner advertised pause frame use: No  
Link partner advertised auto-negotiation: Yes  
Link partner advertised FEC modes: Not reported  
Speed: 10000Mb/s  
Duplex: Full  
Auto-negotiation: on  
Port: Twisted Pair  
PHYAD: 0  
Transceiver: external  
MDI-X: Unknown  
Supports Wake-on: g  
Wake-on: d  
Current message level: 0x00000000 (0)  
Link detected: yes
```

Figure 8.3. Ethernet Link Establishment Status

2. Test the Ethernet connectivity.

Run `ping 192.168.0.2` command on the host terminal. A successful response confirms that the platform network connection is active. You should see messages indicating that packets are being received. Refer to [Figure 8.4](#) for an example of successful ping response from the evaluation board.

Figure 8.4. Data Packet Received by Host

- On the host HSB container prompt, run `hololink-enumerate` command. This command displays the MAC address, Hololink IP version, IP address, and FPGA UUID. See [Figure 8.5](#) for a sample output.

Figure 8.5. Sample Output

- Workaround 1: Ensure the SFP module is securely locked into the SFP cage.
- Workaround 2: Confirm that the LAN cable is properly connected to both the SFP module and the host LAN port. If the connection is correct, the LAN indicator light should be **ON** as shown in [Figure 8.6](#).

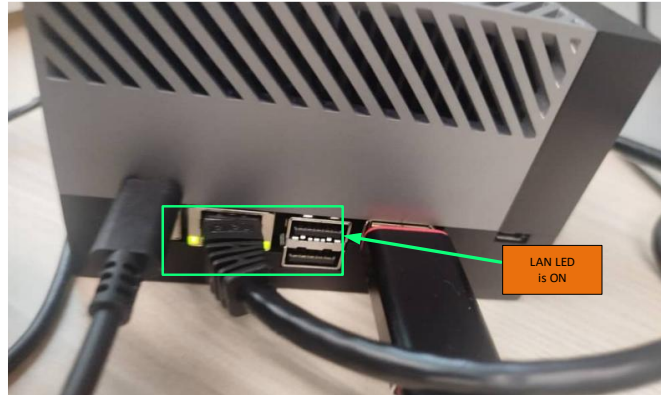


Figure 8.6. LAN Light Indication on Host

8.3. Running the Streaming Script (linux_imx258_player.py)

8.3.1. Preparing the Streaming Script

Run the script. Follow the steps in the [Camera Video Streaming Test](#) section to run *linux_imx258_player.py* on the host HSB Docker container prompt using the command *python examples/linux_imx258_player.py*.

8.3.2. Monitoring the Output of the Streaming Script

Once the script is running, observe the following:

1. Verify the Revision ID.

Check the log for the Revision ID to confirm the FPGA firmware version. [Figure 8.7](#) shows the Revision ID version from the host HSB docker container prompt, which represents the bitstream version for Avant-X with 10G Ethernet.

```

root@agxorin:/home/agx_orin/Desktop/holoscan-sensor-bridge_2.2.0_patches
root@agxorin:/home/agx_orin/Desktop/holoscan-sensor-bridge_2.2.0_patches# python examples/linux_imx258_player.py
<Frozen ImportLib._bootstrap_external:1297: FutureWarning: The cuda.cuda module is deprecated and will be removed in a future release, please switch to u
se the cuda.bindings.driver module instead.
INFO 195 main linux_imx258_player.py:185 tid=MainThread -- Initializing.
I2C Controller Address 1
Camera ID 0
INFO 898 _init_ linux_imx258_player.py:39 tid=MainThread -- _init_
INFO hololink.cpp:1496 configure_hsb tid=0xf1 -- HSB IP version=0x2507 datecode=0x3013364
[info] [fragment.cpp:765] Loading extensions from configs...
INFO 2693 compose linux_imx258_player.py:50 tid=MainThread -- compose
INFO csi_to_bayer.cpp:271 configure tid=0xf1 -- start_byte=0, bytes_per_line=2400, pixel_width=1920, pixel_height=1080, pixel_format=1, trailing_bytes=0.
INFO 2704 compose linux_imx258_player.py:83 tid=MainThread -- frame_size=2592000
INFO 3075 setup base_receiver_op.py:58 tid=MainThread -- setup
[info] [gxf_executor.cpp:326] Creating context
[info] [gxf_executor.cpp:2398] Activating Graph...
[info] [gxf_executor.cpp:2467] Running Graph...
[info] [gxf_executor.cpp:2469] Waiting for completion...
[info] [greedy_scheduler.cpp:191] Scheduling 5 entities
INFO 3182 start base_receiver_op.py:71 tid=Dummy-1 -- frame_size=2592000 frame=4386484224
INFO data_channel.cpp:368 configure_socket tid=0x102 -- (done) DataChannel configure_socket socket_fd=71 local_ip=192.168.0.121.
INFO 3185 start base_receiver_op.py:76 tid=Dummy-1 -- local_ip='192.168.0.121' local_port=46805
INFO data_channel.cpp:119 compute_payload_size tid=0x102 -- header_size=70 payload_size=1400 packets=1841
error: XDC_RUNTIME_DIR is invalid or not set in the environment.
[info] [context.cpp:52] Vulkan Version:
[info] [context.cpp:52] - available: 1.3.275
[info] [context.cpp:52] - requesting: 1.2.0
[info] [context.cpp:52] Used Instance Layers :
[info] [context.cpp:52] Used Instance Extensions :
[info] [context.cpp:52] VK_KHR_surface
[info] [context.cpp:52] VK_KHR_xcb_surface
[info] [context.cpp:52] VK_EXT_debug_utils
[info] [context.cpp:52] VK_KHR_external_memory_capabilities
[info] [context.cpp:52] Compatible Devices :
[info] [context.cpp:52] 0: NVIDIA Tegra Orin (nvgpu)
[info] [context.cpp:52] Physical devices found :
[info] [context.cpp:52] 1

```

Figure 8.7. Revision ID Version

2. Check the camera for I2C configuration errors.

Look for any I2C configuration errors in the log, when the *linux_imx258_player.py* script is executed. [Figure 8.8](#) shows an example of a failed camera I2C configuration.


```
root@agxorin: /home/agx_orin/Desktop/holoscan-sensor-bridge_2.2.0_patches
root@agxorin:/home/agx_orin/Desktop/holoscan-sensor-bridge_2.2.0_patches# python examples/linux_imx258_player.py
<frozen importlib._bootstrap_external>:1297: FutureWarning: The cuda.cuda module is deprecated and will be removed in a future release, please switch to use the cuda.bindings.driver module instead.
INFO 196 main linux_imx258_player.py:185 tid=MainThread -- Initializing.
I2C Controller Address 1
Camera ID 0
INFO 1413 __init__ linux_imx258_player.py:39 tid=MainThread -- __init__
INFO hololink.cpp:1496 configure_hsb tid=0x109 -- HSB IP version=0x2507 datecode=0x1023336
Traceback (most recent call last):
  File "/home/agx_orin/Desktop/holoscan-sensor-bridge_2.2.0_patches/examples/linux_imx258_player.py", line 238, in <module>
    main()
  File "/home/agx_orin/Desktop/holoscan-sensor-bridge_2.2.0_patches/examples/linux_imx258_player.py", line 227, in main
    camera_0.configure()
  File "/usr/local/lib/python3.12/dist-packages/hololink/sensors/imx258.py", line 164, in configure
    self.set_register(reg, val)
  File "/usr/local/lib/python3.12/dist-packages/hololink/sensors/imx258.py", line 209, in set_register
    self._i2c.i2c_transaction(
RuntimeError: I2C port indicates I2C_I2C_NAK.
root@agxorin:/home/agx_orin/Desktop/holoscan-sensor-bridge_2.2.0_patches#
```

Figure 8.8. Camera I2C configuration fail log

3. Confirm MIPI Camera Streaming
If no errors are detected, the MIPI camera streaming should be display successfully on the host monitor.

8.3.3. Troubleshooting Common Errors

- Revision ID version mismatch.
 - Workaround: Reprogram the HSB board with the correct FPGA bitstream version.
- Camera I2C Configuration Error.
 - Workaround 1: Ensure the *IMX258* camera sensor is properly connected.
 - Workaround 2: If you are using your own reference design HDL code, verify that the camera reset signal is not asserted.
 - Workaround 3: If you are using your own software patch, confirm the camera I2C configuration port is correctly targeted.
 - Workaround 4: If you are using your own software patch, ensure the camera sensor register settings are correct.

Appendix A. Known Issue

- Remote firmware update via Ethernet is not available on the current Avant Versa customizable HSB sensor interface reference design.

References

- [CSI-2/DSI D-PHY Receiver IP Core - User Guide \(FPGA-IPUG-02081\)](#)
- [CSI-2/DSI D-PHY Receiver IP Core](#) web page
- [Avant-X Versa Board](#) web page
- [Lattice Radiant](#) FPGA design software
- [Lattice Solutions IP Cores](#) web page
- [Lattice Radiant Software User Guide](#)
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans
- [NVIDIA Holoscan - NVIDIA Docs](#) NVIDIA Holoscan Docs Hub

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, December 2025

Section	Change Summary
All	Initial release.



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