MachXO5-55TD and MachXO5-55TDQ Evaluation Boards

Preliminary

User Guide

FPGA-EB-02076-0.80

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AC	Alternating Current
ADC	Analog-to-Digital Converter
ASC	Analog Sense and Control
caBGA	Chip Array Ball Grid Array
CMOS	Complementary Metal-Oxide Semiconductor
DC	Direct Current
DI	Do Install
DIP	Dual In-line Package
DNI	Do Not Install
EFUP	Environment-Friendly Use Period
ESD	Electrostatic Discharge
FTDI	Future Technology Devices International
FPC	Flexible Printed Circuit
FPGA	Field Programmable Gate Array
Gbe	Gigabit Ethernet
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit
IP	Intellectual Property
I/O	Input/Output
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
L-ASC10	Lattice Analog Sense and Control-10 Rail
LDO	Low Dropout
LED	Light Emitting Diode
LPDDR4	Low Power Double Data Rate Four
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
OPN	Ordering Part Number
OSC	Oscillator
PC	Personal Computer
PCIe	Peripheral Component Interconnect Express
PCS	Physical Coding Sublayer
PHY	Physical Layer
PLD	Programmable Logic Device
PLL	Phase-Locked Loop
PMOD	Peripheral Module
POT	Potentiometer
PSR	Production Shipment Release
RAM	Random Access Memory
RX	Receiver
UART	Universal Asynchronous Receiver/Transmitter
SGMII	Serial Gigabit Media Independent Interface
SLVS	Scalable Low Voltage Signaling
SMA	SubMiniature version A
SPI	Serial Peripheral Interface

Abbreviation	Definition
SSPI	Synchronous Serial Peripheral Interface
TX	Transmitter
USB	Universal Serial Bus

1. Introduction

The Lattice Semiconductor MachXO5™-55TD and MachXO5-55TDQ Evaluation Boards allow you to investigate and experiment with the features of the MachXO5-NX LFMXO5-55TD and LFMXO5-55TDQ devices. The features of the MachXO5-55TD and MachXO5-55TDQ Evaluation Boards can assist you with the rapid prototyping and testing of your specific designs.

The MachXO5-55TD Evaluation Board includes the following:

- MachXO5-55TD Evaluation Board pre-loaded with the demo design
  Note: The board ordering part number (OPN) is LFMXO5-55TD-EVN.
- 12 V AC/DC Power adapter
- Mini USB cable
- Quick Start Guide

The MachXO5-55TDQ Evaluation Board includes the following:

- MachXO5-55TDQ Evaluation Board pre-loaded with the demo design
  Note: The board OPN is LFMXO5-55TDQ-EVN.
- 12 V AC/DC Power adapter
- Mini USB cable
- Quick Start Guide

The contents of this user guide include top-level functional descriptions of the various portions of the boards, descriptions of the on-board headers, diodes, and switches, and a complete set of schematics. While this document applies to both the MachXO5-55TD and MachXO5-55TDQ Evaluation Boards, the board pictures, the schematics, and the bill of materials are of the MachXO5-55TD Evaluation Board, whose OPN is LFMXO5-55TD-EVN.

1.1. MachXO5-55TD and MachXO5-55TDQ Evaluation Boards

Along with the LFMXO5-55TD and LFMXO5-55TDQ devices, the MachXO5-55TD and MachXO5-55TDQ Evaluation Boards also include features to expand the LFMXO5-55TD and LFMXO5-55TDQ devices usability with Arduino, Raspberry, PCIe, RJ45, Versa, and Aardvark headers. The board pictures provided below show the MachXO5-55TD Evaluation Board featuring the LFMXO5-55TD device, with the OPN LFMXO5-55TD-EVN. For the MachXO5-55TDQ Evaluation Board with the LFMXO5-55TDQ device, the OPN is LMFXO5-55TDQ-EVN. The only difference between the two boards is the U3 component, which is either the LFMXO5-55TD or LFMXO5-55TDQ device. The rest is the same for both boards.

Figure 1.1 shows the top view of the MachXO5-55TD Evaluation Board.

Figure 1.2 shows the bottom view of this board.

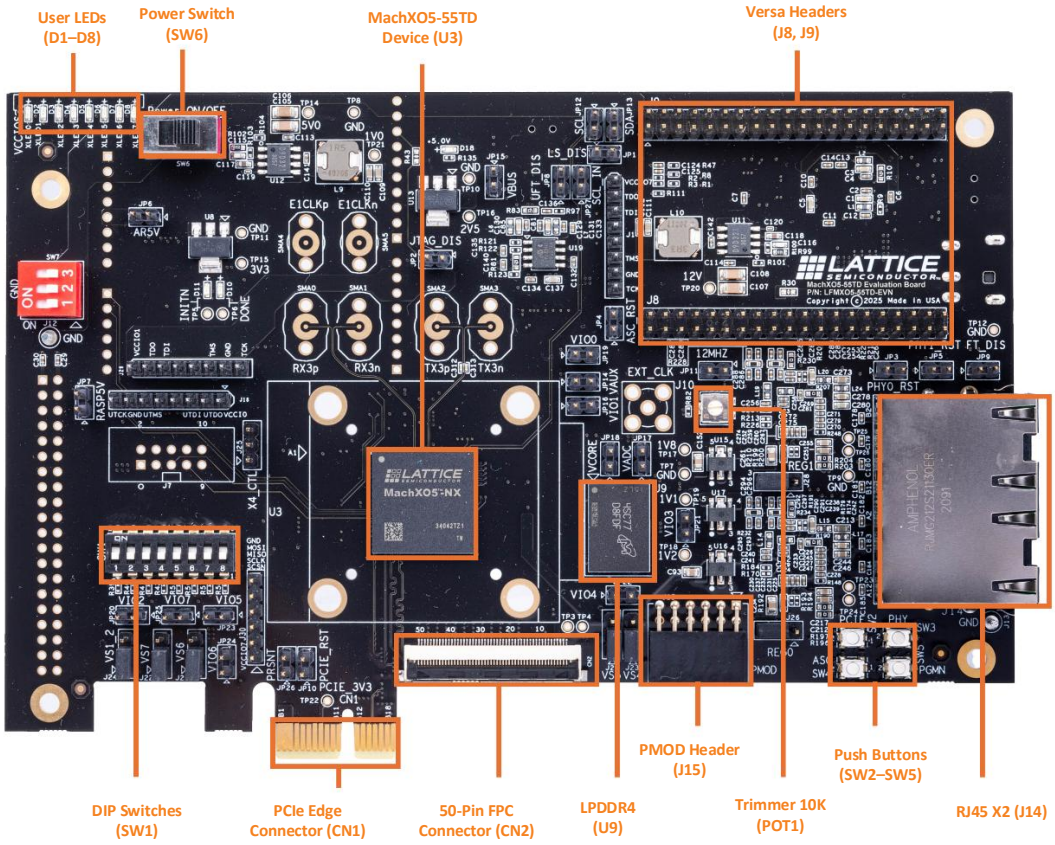

Figure 1.1. Top View of MachXO5-55TD Evaluation Board

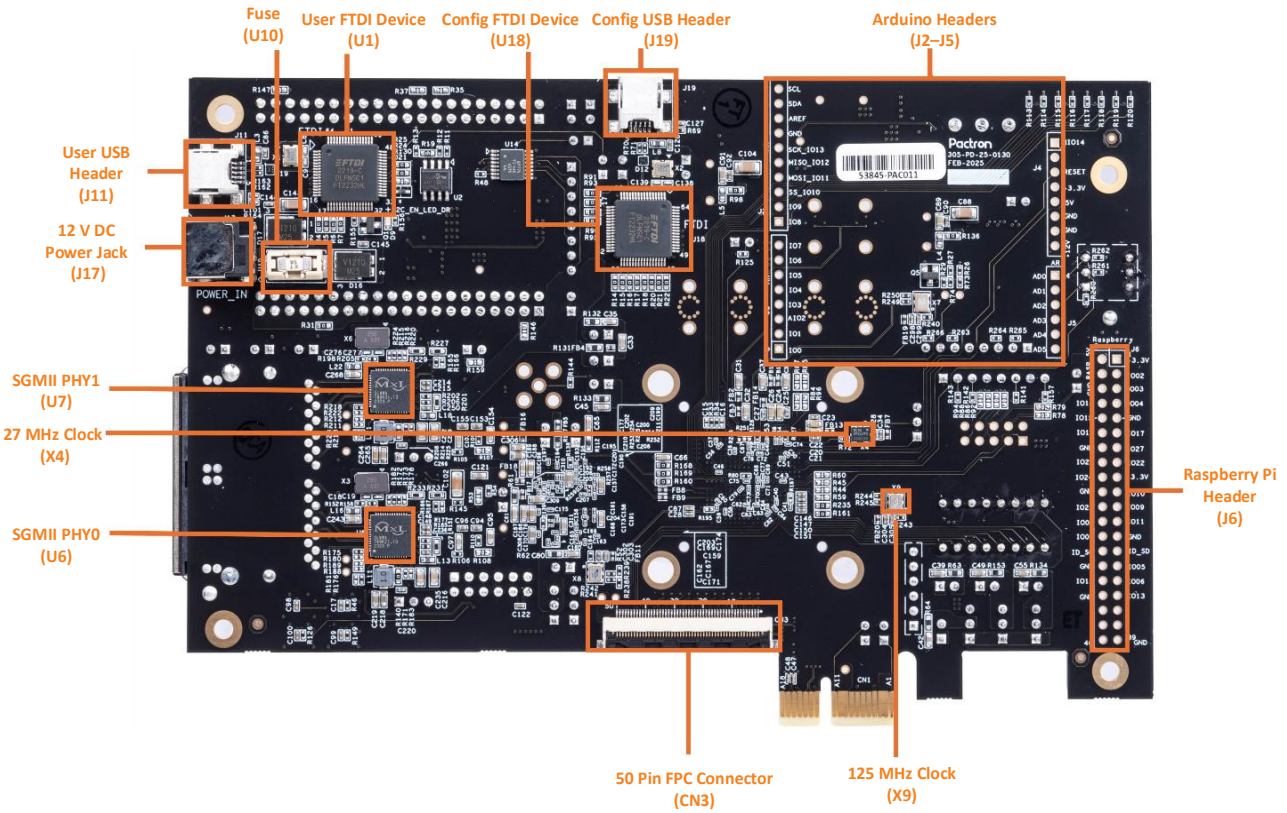

Figure 1.2. Bottom View of MachXO5-55TD Evaluation Board

1.2. Features

- On-board LFMXO5-55TD or LFMXO5-55TDQ device
- Two Gigabit Ethernet (Gbe) PHY RJ45 connectors, with Serial Gigabit Media Independent Interface (SGMII) PHY support
- Low Power Double Data Rate Four (LPDDR4) up to 1066 Mbps, ×16 bits
- Peripheral Component Interconnect Express (PCIe) Gen2 x1 Edge Connector
- Optional SubMiniature version A (SMA) to support ×1 PCIe
- Versa Headers bridge with Lattice Advanced Signal Controller (ASC) Demo Board to support L-ASC10
- General Purpose Input/Output (GPIO) interface with Peripheral Module (PMOD), Arduino and Raspberry Pi boards
- USB-B connection for device programming with Joint Test Action Group (JTAG) and Inter-Integrated Circuit (I2C) utility
- Additional USB-B connection for user with Soft JTAG and Universal Asynchronous Receiver/Transmitter (UART) utility
- Eight-position Dual In-line Package (DIP) Switches, four push buttons, and eight red LEDs for demo purposes
- Analog-to-Digital Converter (ADC) interface with 10K POT
- Two 50-pin Flexible Printed Circuit (FPC) headers
- Multiple reference clock sources
- Optional Aardvark header
- Support FPGA Power Evaluation
- Lattice Radiant™ Software programming support

Note: DNI stands for *Do Not Install* parts and DI stands for *Do Install* parts for assembly.

Caution: The MachXO5-55TD and MachXO5-55TDQ Evaluation Boards contain Electrostatic Discharge (ESD) -sensitive components. ESD safe practices should be followed while handling and using the evaluation boards.

1.3. LFMXO5-55TD and LFMXO5-55TDQ Devices

The MachXO5-55TD and MachXO5-55TDQ Evaluation Boards feature the LFMXO5-55TD and LFMXO5-55TDQ devices, respectively, each in a 400-ball caBGA package. The LFMXO5-55TD and LFMXO5-55TDQ devices both offer a variety of features and programmability that enhances Secure Control Programmable Logic Device (PLD) functionality with Multiple Boot capabilities. Its cryptographic engine supports user-mode security features. Along with the cryptographic engine, numerous system functions are included such as four Phase-Locked Loops (PLL) and 3,744 kbits of embedded RAM plus hardened implementations of I2C and Serial Peripheral Interface (SPI). The MachXO5-NX FPGAs feature one hard PCIe link layer IP block which supports PCIe Gen1, Gen2 with one or two ×1 configuration, with flexible, high performance I/O supporting numerous single-ended and differential standards including LPDDR4 controller and Scalable Low Voltage Signaling (SLVS). For more information on the capabilities of LFMXO5-55TD and LFMXO5-55TDQ devices, see MachXO5-NX Family Root of Trust Devices Data Sheet (FPGA-DS-02120).

2. Applying Power to the Boards

The MachXO5-55TD and MachXO5-55TDQ Evaluation Boards come ready to power up with on-board DC/DC switching regulators and Low Dropout (LDO) generators powered by an external 12 V DC power source. The external power supply can be connected with the DC power input jack J17 or the PCIe edge connector CN1, which is fused with a surface mounted fuse U10. The 5 A fuse prevents the crashed current from flowing into the internal circuits and causing serious damage, as shown in Figure 2.1.

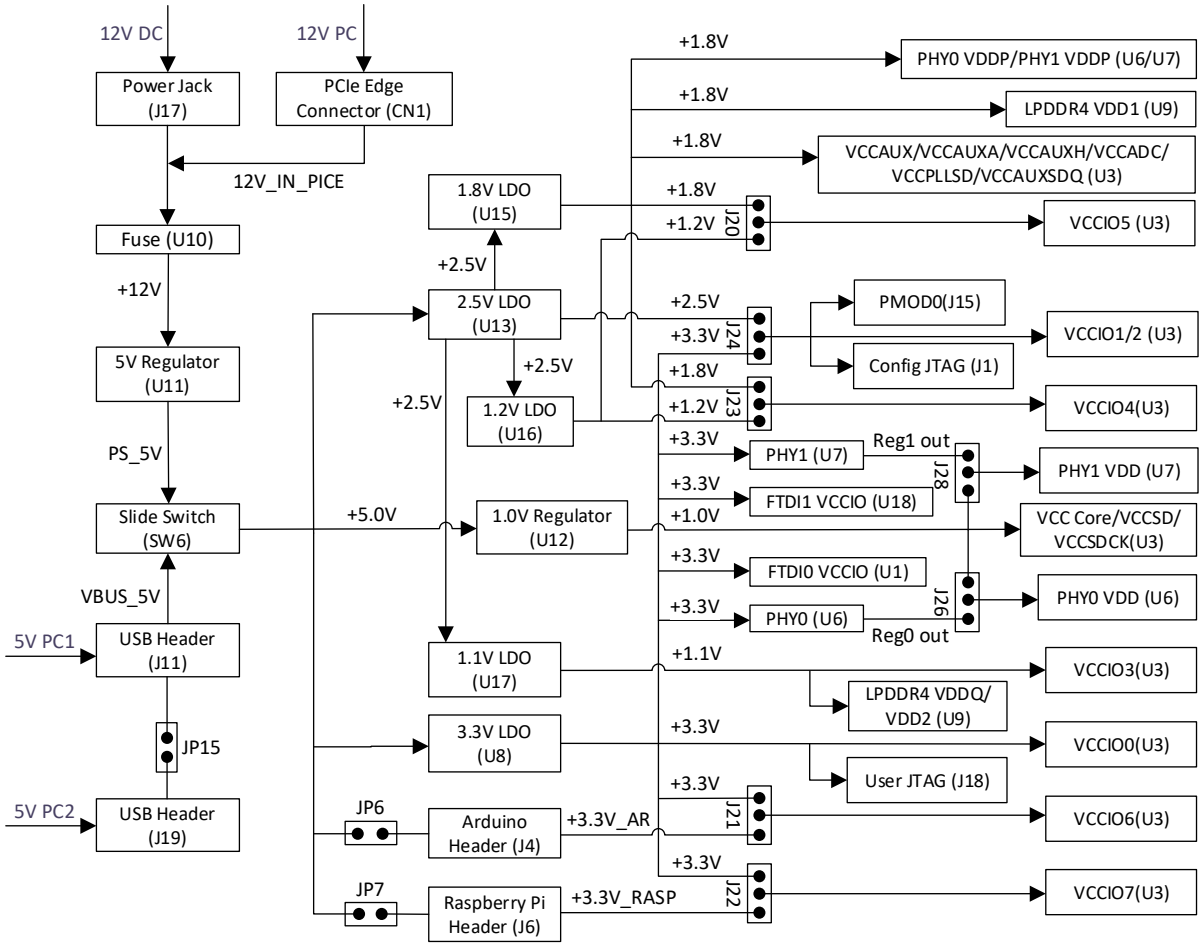

Figure 2.1. Board Power Supply

The on-board 5 V power regulator U11 provides 90% power convert efficiency from 12 V DC when the output current is between 50 mA and 3 A. It is distributed to 3.3 V, 2.5 V LDOs, and 1.0 V regulator through one side of slide switch SW6 to support on-board devices. Through another side of SW6, this board can take the 5 V DC power from USB header J11 as well to supply those LDOs. For some low power applications, JP15 can be used to double the power supplier capability, if J19 is also plugged into the same PC that is connected to J11. You need to ensure 5 V DC power consumes less than maximum capability from each USB port of PC when taking power from J11 and J19.

For the board extension, the 5 V DC power can also supply Raspberry Pi and Arduino boards through the jumpers and on-board headers, to consolidate AC/DC adapters for stack boards system. Conversely, the 5 V DC power for the MachXO5-55TD and the MachXO5-55TDQ Evaluation Boards can be supplied either from mated Raspberry Pi or Arduino Boards, if they are powered up by external AC/DC adapters already. You need to ensure the 5 V power is from a single source when adding JP6 or JP7 jumpers. However, maintaining the 5 V DC supplier is the basic requirement to power on the board, which is indicated by the power good blue LED D18.

The on-board 1.1 V, 1.2 V, and 1.8 V LDOs take the power from the 2.5 V LDO output.

Table 2.1 summarizes on-board major power rails and their test points.

Table 2.1. On-board Major Power Rails

Power Net Name	Primary Source	Test Point
+12V	DC Power Jack (J17) or PCIE Edge Connecter (CN1)	TP20
PS_5V	DC/DC Regulator (U11)	—
VBUS_5V	Mini-USB Headers (J11 or J19)	JP15
+5.0V	Selected by Slide Switch (SW6)	TP14
+3.3V	LDO (U8)	TP15
+2.5V	LDO (U13)	TP16
+1.8V	LDO (U15)	TP17
+1.2V	LDO (U16)	TP18
+1.1V	LDO (U17)	TP19
+1.0V	DC/DC Regulator (U12)	TP21
+3.3V_RASP	Raspberry Pi Header (J6)	—
+3.3V_AR	Arduino Header (J4)	—

As shown in Figure 2.1, the MachXO5-55TD and the MachXO5-55TDQ Evaluation Boards provide multiple power options for I/O bank voltage flexibility. Table 2.2 summarizes the V_{CCIO} support matrix on each board. For example, V_{CCIO1} and V_{CCIO2} share the same three-position jumper J24 and shorting its Pin 1 and Pin 2 can bring the 3.3 V LDO output to both I/O Bank 1 and Bank 2. For power consumption evaluation, each board facilitates some two-position jumpers with 1 Ω sense resistors to measure the voltage drop on each power rail. Then, the supply current can be calculated.

Table 2.2. LFMXO5-55TD and LFMXO5-55TDQ I/O Bank Power Rails Stuff

LFMXO5-55TD and LFMXO5-55TDQ Power (U3)	Jumpers	3.3 V	2.5 V	1.8 V	1.2 V	1.1 V	External 3.3 V	Power Test Point	Sense Resistor of 1 Ω
V_{CCIO0}	—	Fixed	—	—	—	—	—	JP19	R132
V_{CCIO1}	J24	Pin 1-2	Pin 2-3	—	—	—	—	JP16	R133
V_{CCIO2}	J24	Pin 1-2	Pin 2-3	—	—	—	—	JP20	R134
V_{CCIO3}	—	—	—	—	—	Fixed	—	JP21	R61
V_{CCIO4}	J23	—	—	Pin 1-2	Pin 2-3	—	—	JP22	R62
V_{CCIO5}	J20	—	—	Pin 1-2	Pin 2-3	—	—	JP23	R63
V_{CCIO6}	J21	Pin 1-2	—	—	—	—	Pin 2-3	JP24	R64
V_{CCIO7}	J22	Pin 1-2	—	—	—	—	Pin 2-3	JP25	R153

Other than the power rail for each I/O bank, the MachXO5-55TD and MachXO5-55TDQ Evaluation Boards also provide some test points to evaluate the major power consumptions for the LFMXO5-55TD and the LFMXO5-TDQ devices respectively, as listed in Table 2.3.

Table 2.3. LFMXO5-55TD and LFMXO5TDQ Devices Major Power Rails Stuff

LFMXO5-55TD and LFMXO5-55TDQ Power (U3)	Power Test Point	Voltage Drop Resistor	Resistance
V_{CC_CORE}	JP18	R112	0.01 Ω
V_{CC_AUX}/V_{CC_AUXH}/V_{CCAUXA}	JP14	R131	1 Ω
V_{CC_ADC}	JP17	R137	1 Ω

3. JTAG & SSPI Provisioning

MachXO5-55TD and MachXO5-TDQ devices support JTAG and SSPI Provisioning. The JTAG architecture of the MachXO5-55TD and MachXO5-55TDQ Evaluation Boards is shown in Figure 3.1. The boards have a built-in download controller for provisioning the LFMXO5-55TD and LFMXO5-55TDQ devices. It uses an FT2232H Future Technology Devices International (FTDI) part U1 to convert USB to JTAG from port A. Using the Detect Cable function with the Lattice Radiant programming software installed, you can detect dual ports after powering up the board and connecting the mini-USB to USB-A cable from J11 to your PC. Ensure the FTDI reset control jumper JP9 is not populated as default. The software select option FTUSB-0 is dedicated for JTAG and FTUSB-1 is dedicated for hard I2C that maps with port A and port B from a hardware perspective, as shown in Figure 3.2.

For SSPI provisioning, you can connect Lattice USB 2B cable to J30, and use Propel Provision Tool to perform SSPI provisioning.

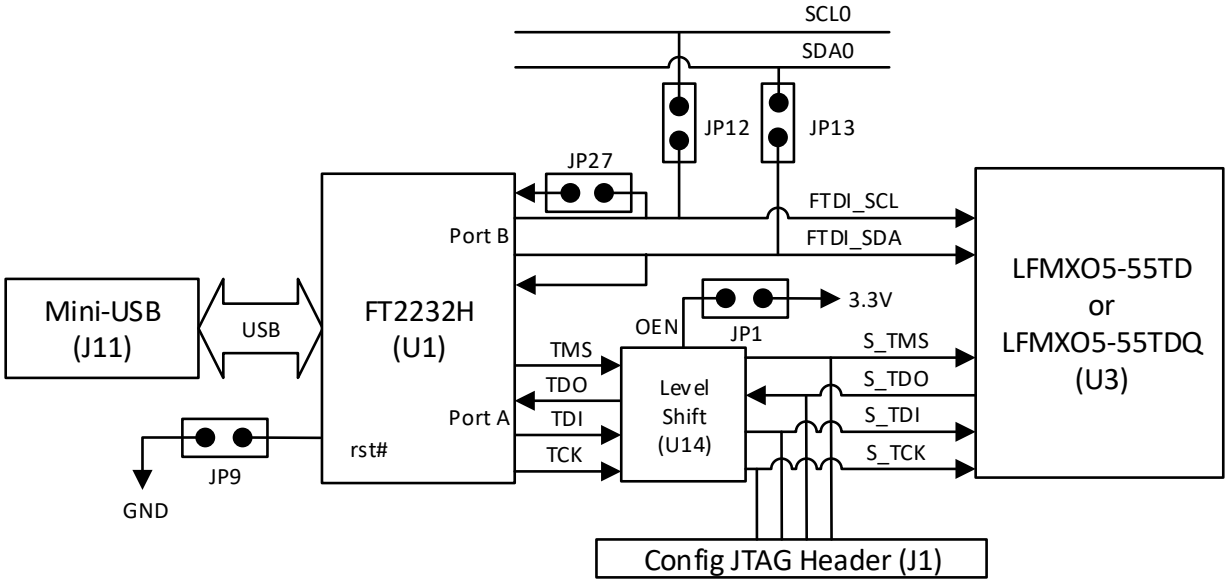

Figure 3.1. JTAG Programming Architecture

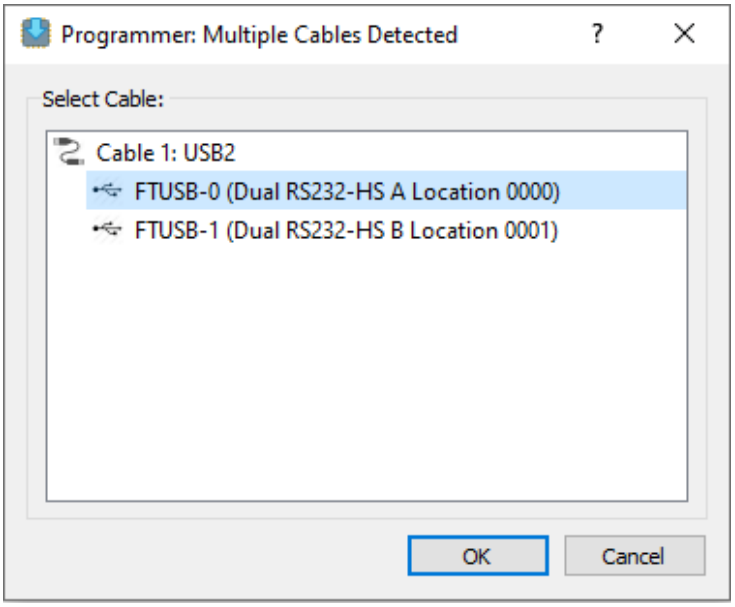

Figure 3.2. Radiant Programmer Detect Dual Ports

3.1. JTAG Download Interface

A level shifter SN74AVC4T774 U14 from TI is inserted between Config FTDI Port A and the LFMXO5-55TD or the LFMXO5-55TDQ JTAG port to make sure the FTDI fixed I/O voltage can adapt with flexible voltage selection of Bank 2 of the FPGA, as shown in Figure 3.3. An 8-pin header J1 (Figure 3.4) allows you to probe the JTAG signals to access the LFMXO5-55TD or the LFMXO5-55TDQ JTAG port from the external JTAG host, such as an external Lattice HW-USBN-2B Programming Cable available separately. In those cases, the jumper JP1 must be added to pull OEN high and ensure U14 enters a tri-state mode so as to avoid multi-drivers on those shared signals. The JTAG connections between J1 and the LFMXO5-55TD or the LFMXO5-55TDQ device are listed in Table 3.1.

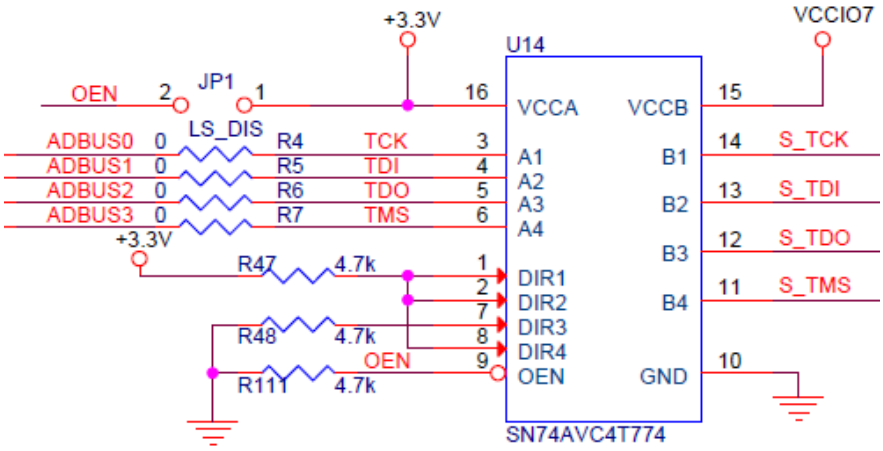

Figure 3.3. Level Shift for JTAG Download Interface

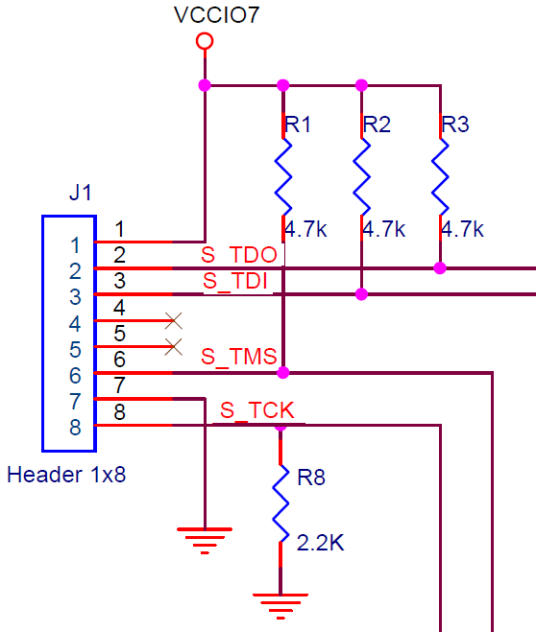

Figure 3.4. JTAG Test Header

Table 3.1. Config JTAG Connections

J1 Pin Number	JTAG Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location for JTAG
1	VCCIO7	—
2	S_TDO	H2
3	S_TDI	H4
4	—	—
5	—	—
6	S_TMS	H1
7	GND	—
8	S_TCK	H3

The MachXO5-55TD and MachXO5-55TDQ Evaluation Boards also provide test points for other dedicated JTAG configuration pins, as shown in Table 3.2.

Table 3.2. Other Config JTAG Control Signals

Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location	LED Indicator	Test Point
PROGRAMN	G10	—	—
INITN	H10	D11	TP5
DONE	H11	D10	TP6

Using the SW5 push button with PROGRAMN reloads the bitstream from the internal Flash when the PROGRAMN_PORT function is enabled by the software.

4. Soft JTAG/UART User Interface

The soft JTAG/UART user interface for the MachXO5-55TD and MachXO5-55TDQ Evaluation Boards is shown in Figure 4.1. Supposedly it also uses an FT2232H FTDI part U18 to convert USB to user JTAG from port A, or convert USB to UART from port B. Using the Detect Cable function with the Lattice Radiant programming software installed and ensuring FTDI reset control jumper JP8 is not populated in default (Figure 3.2), you can detect other dual ports after powering up the board. You can then connect the mini-USB to USB-A cable from J19 to your PC. The software select option FTUSB-0 is targeted for user JTAG, and FTUSB-1 is targeted for UART that is mapped with port A and port B from the hardware perspective.

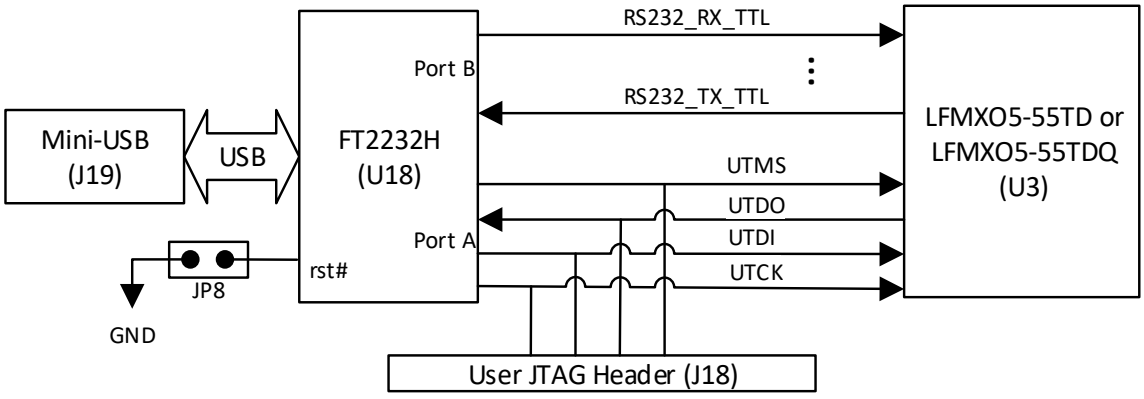

Figure 4.1. JTAG/UART User Interfacing

4.1. Soft JTAG User Interface

User FTDI Port A is connected with GPIOs in bank 1 directly. You need to allocate GPIOs for adaptation with JTAG signals by programmable logic, which is defined by FTDI Port A when converting USB to JTAG through FTUSB-0. J18 is an eight-pin standalone JTAG header that is used with an external Lattice download cable available separately when the FTDI part is disabled from the JTAG chain after setting JP8. J18 can also be used as a test point when USB to JTAG is working.

Table 4.1. Soft JTAG Connections

J18 Pin Number	FTDI Signal	JTAG Net Name	LFMXO5-55TD/Q Ball Location
1	—	VCCIO1	—
2	UADBUS2	UTDO	F12
3	UADBUS1	UTDI	F13
4	—	—	—
5	—	—	—
6	UADBUS3	UTMS	G13
7	—	GND	—
8	UADBUS0	UTCK	G14

4.2. Soft UART User Interface

User FTDI Port B is also connected with GPIOs in Bank 0 directly. You need to allocate GPIOs for adaptation with UART signals by the programmable logic, which is defined by FTDI Port B when converting USB to UART through FTUSB-1.

Table 4.2. Soft UART Connections

FTDI Signal	UART Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location for Port A
UBDBUS0	RS232_RX_TTL	C15
UBDBUS1	RS232_TX_TTL	D15
UBDBUS2	RTSn	B15
UBDBUS3	CTSn	A15
UBDBUS4	DTRn	E13
UBDBUS5	DSRn	E12
UBDBUS6	DCDn	D14
UBDBUS7	RI	E15

5. LFMXO5-55TD and LFMXO5-55TDQ Clock Sources

The MachXO5-55TD and MachXO5-55TDQ Evaluation Boards have multiple external clock options for the LFMXO5-55TD and LFMXO5-55TDQ applications respectively, as shown in Figure 5.1.

- 12 MHz from U1 (FTDI)
- 27 MHz from ×4 (OSC MEM)
- External clock source from J10 (SMA)
- Differential 100 MHz from ×7
- Differential 100 MHz from ×8
- Differential 125 MHz from ×9
- Differential external clock source from SMA4 and SMA5 (SMA pair)

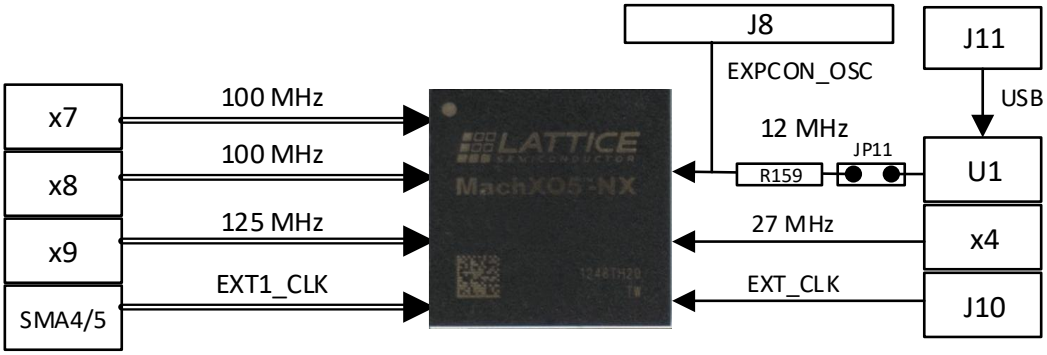

Figure 5.1. On-board Clock Resources

Make sure 12 MHz clocks from the FT2232H FTDI U1 device are not always on without some hardware configuration. SMA clocks need source from external boards. Refer to Table 5.1 for the clock utilization and enable conditions.

Table 5.1. Input Clock Options

Clock Frequency	Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location	Clock Source	I/O Type	Enable Conditions
12 MHz	EXPCON_OSC	J16	U1	LVCMOS33	Need add R159 and JP11. USB header J11 connected upon power on.
27 MHz	27M_OSC_IN	C2	X4	LVCMOS33	Always on. Use J25 to disable or control the clock output.
EXT_CLK	OSC_IN	A17	J10	LVCMOS33 or LVCOMS25	Need to add J10 SMA. Connected to the external clock generator through the SMA cable.
100 MHz	EXT0_CLKp/ EXT0_CLKn	C11/C12	X7	LVDS	Always on. Dedicated reference clock for PCS.
100 MHz	LVSTLD_100MHzp/ LVSTLD_100MHzn	U19/U20	X8	LVSTLD	Always on. Generated by the HSCL clock and AC coupled to the 1.1 V I/O bank for LPDDR4.
125 MHz	LVDS_125MHzp/ LVDS_125MHzn	R3/P3	X9	LVDS	Always on. Dedicated reference clock for PCS.
SMA_CLK	EXT1_CLKp/EXT1_ CLKn	B13/C13	SMA4/ SMA5	LVDS	Needs to add SMA4 and SMA5. Connected to the external differential clock generator through SMA cables.

6. SGMII Ethernet Connections

This section describes the MachXO5-55TD and MachXO5-55TDQ Evaluation Boards SGMII application for Ethernet connections. The boards can support two independent Ethernet connections through on-board SGMII PHY devices PHY0 and PHY1, which is GPY115C0VI from Maxlinear, as shown in Figure 6.1. Table 6.1 lists the signals from the FPGA interfacing with SGMII PHY devices.

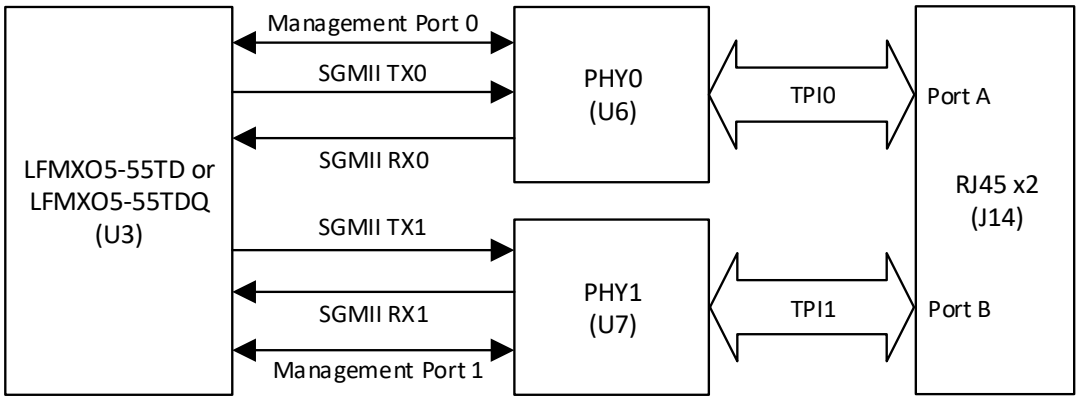

Figure 6.1. SGMII ×2 Interfacing

Table 6.1. SGMII Ethernet PHY Interfacing

PHY Interface	LFMXO5-55TD and LFMXO5-55TDQ Ball Location	Net Name	Pin Number of PHY Device
PHY0 (U6)	P6	PHY0_MDIO	10
	U2	PHY0_MDC	11
	R4	PHY0_MDINT	12
	T5	PHY0_EXINT0	13
	P2	SGMII_FPGA_RX0P	25
	R2	SGMII_FPGA_RX0N	24
	T1	SGMII_FPGA_TX0P	27
	U1	SGMII_FPGA_TX0N	28
PHY1 (U7)	P7	PHY1_MDIO	10
	T2	PHY1_MDC	11
	P4	PHY1_MDINT	12
	U5	PHY1_EXINT0	13
	R5	SGMII_FPGA_RX1P	25
	P5	SGMII_FPGA_RX1N	24
	P1	SGMII_FPGA_TX1P	27
	R1	SGMII_FPGA_TX1N	28

The pin strapping configuration for both SGMII PHY devices has been implemented on-board, as shown in Table 6.2 and Table 6.3.

Table 6.2. SGMII Ethernet PHY0 Strapping Configuration

U6 Pin Number	Configuration Item Description	Logic Value in Default	1K Pull-up Resistor	1K Pull-down Resistor
37	PS_PHY_MADDR(0)	0	R182 (DNI)	R172
35	PS_PHY_MADDR(1)	0	R178 (DNI)	R173
34	PS_PHY_MADDR(2)	0	R179 (DNI)	R174
3	PS_PHY_MADDR(3)	0	R180 (DNI)	R175
2	PS_PHY_MADDR(4)	0	R181 (DNI)	R176
12	PS_MINT_POL	0	R183 (DNI)	R171
18	PS_RJ45_TAP	0	R184 (DNI)	R170
19	PS_MDIO_VOLTAGE	0	NA	R177

Table 6.3. SGMII Ethernet PHY1 Strapping Configuration

U7 Pin Number	Configuration Item Description	Logic Value in Default	1K Pull-up Resistor	1K Pull-down Resistor
37	PS_PHY_MADDR(0)	0	R224(DNI)	R215
35	PS_PHY_MADDR(1)	0	R220(DNI)	R216
34	PS_PHY_MADDR(2)	0	R221(DNI)	R217
3	PS_PHY_MADDR(3)	0	R222(DNI)	R218
2	PS_PHY_MADDR(4)	0	R223(DNI)	R219
12	PS_MINT_POL	0	R225(DNI)	R214
18	PS_RJ45_TAP	0	R226(DNI)	R213
19	PS_MDIO_VOLTAGE	0	—	R202

The MachXO5-55TD and MachXO5-55TDQ Evaluation Boards provide two options to supply the VDD power of PHY devices, as shown in Table 6.4. One option is to supply the VDD with on-board 1.0 V regulator. The other option needs additional power from the on-board 3.3 V LDO and converts to 1.0 V output by the internal regulator of PHY devices. It is recommended to use the first option to improve power efficiency and offload the 3.3V LDO on the board.

Table 6.4. PHY device VDD Power Supply Options

PHY VDD	Jumper	Supply from On-board Regulator	Supply from In-chip Regulator
U6	J26	Pin 2-3 (U12)	Pin 1-2 (U6)
U7	J28	Pin 2-3 (U12)	Pin 1-2 (U7)

7. PCIe Gold Finger

The MachXO5-55TD and MachXO5-55TDQ Evaluation Boards support ×1 PCIe Gen2, as shown in Figure 7.1. The signal connections are listed in Table 7.1.

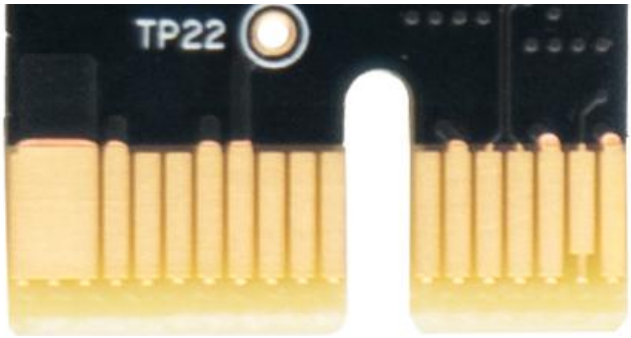

Figure 7.1. Top Side of PCIe Edge Connector

Table 7.1. Gold Finger Pin Connections

CN1 Pin Number	Net Name	LFMXO5-55TD and MachXO5-55TDQ Ball Location
A1	PRSNT1n	—
A2,A3,B1,B2,B3	12_IN_PCIE	—
A4,A12,A15,A18,B4,B7,B13,B16,B18	GND	—
A9,A10,B8	PCIE_3V3	—
A11	PCIE_PERSTn	K6[1]
A13	PCIE_CLKP	C7
A14	PCIE_CLKN	B7
A16	x1_PERp0	A5
A17	x1_PERn0	A6
B14	x1_PETp0	A2
B15	x1_PETn0	A3
B17	PRSNT2n	—
—	R0_ext	C4
—	RET0_ref	B4

Note:

1. Needs to add JP10 to bridge with FPGA control I/O.

8. Optional SMA Headers

The MachXO5-55TD and MachXO5-55TDQ Evaluation Boards provide two pairs of high-speed SMA footprints to support flexible Serdes Protocol validation, with x1 RX and TX signal pairs, as shown in Figure 8.1. Their SMA footprint is compatible with SF2921-61345-2S from Amphenol. The signal mapping is shown in Table 8.1.

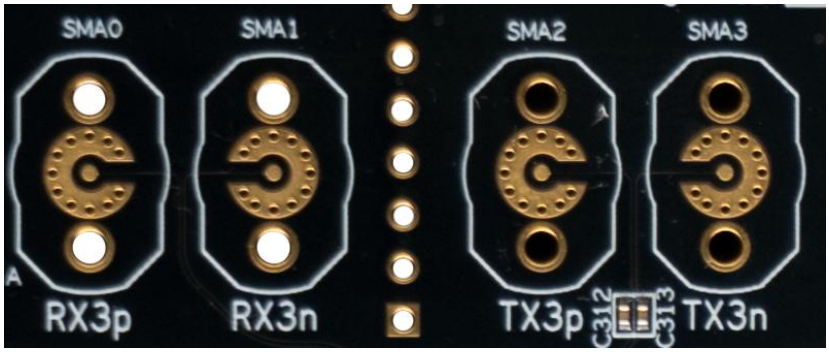

Figure 8.1. SMA Interfacing for x1 Serdes RX and TX

Table 8.1. Connections for SMA Serdes Signal Pair

Reference	Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location
SMA0	SD3_RXp	A8
SMA1	SD3_RXn	A9
SMA2	SD3_TXp	A11
SMA3	SD3_TXn	A12

Note: LFMXO5-55TD and LFMXO5-55TDQ engineering samples cannot support additional PCIe lane through the SMA.

The MachXO5-55TD and MachXO5-55TDQ Evaluation Boards also provide a pair of high-speed SMA footprints to support SerDes extension reference clock input as shown in Figure 8.2. Their SMA footprint is compatible with SF2921-61356-2S from Amphenol and the LVDS clock is recommended to be connected. The signal mapping is shown in Table 8.2.

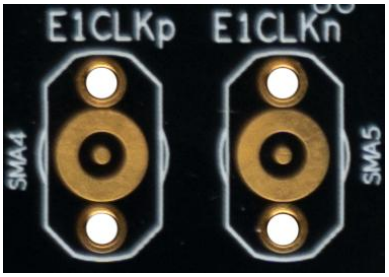

Figure 8.2. SMA Interfacing for x1 SerDes RX and TX

Table 8.2. Connections for External SMA Reference Clock

SMA	Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location
SMA4	EXT1_CLKp	B13
SMA5	EXT1_CLKn	C13

The MachXO5-55TD and MachXO5-55TDQ Evaluation Boards are also designed with a single-end SMA clock header J10, as shown in Figure 8.3. This is a low-cost standard type SMA footprint, such as 5-1814832-2 from TE Connectivity. You need to solder it on the board. Table 8.3 details its connection to the FPGA.

Figure 8.3. SMA Clock Input

Table 8.3. Single-End External SMA Clock

SMA	Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location
J10	EXT_CLK	A17

9. LPDDR4 Memory Controller Interface

Table 9.1 lists all LPDDR4 memory controller Interface signals. The LFMXO5-55TD and LFMXO5-55TDQ devices Memory Controller is used to interface with the on-board 16-bit parallel data and 8 Gb capacity LPDDR4 memory device, Micron MT53E512M16D1, which is supported with 512 Meg ×16 configurations. The MahXO5-55TD and MachXO5-55TDQ Evaluation Boards are designed to use on-die termination in default and reserved on-board termination options.

Table 9.1. LPDDR4 Memory Controller Interconnections

LPDDR4 Net Name (U9)	LFMXO5-55TD and LFMXO5-55TDQ Ball Location
DQ0_A	N18
DQ1_A	N20
DQ2_A	P18
DQ3_A	P17
DQ4_A	P16
DQ5_A	N19
DQ6_A	M17
DQ7_A	M16
DMI0_A	N17
DQS0_T_A	P19
DQS0_C_A	P20
DQ8_A	R15
DQ9_A	T14
DQ10_A	R14
DQ11_A	T15
DQ12_A	V14
DQ13_A	W14
DQ14_A	V15
DQ15_A	U14
DMI1_A	U15
DQS1_T_A	Y15
DQS1_C_A	Y14
CA0_A	W19
CA1_A	V18
CA2_A	T19
CA3_A	V19
CA4_A	V20
CA5_A	T20
CK_T_A	R19
CK_C_A	R20
CKE0_A	W20
CS0_A	W18
ODT_CA_A	R16
RESET_N	N16
ZQ0[1]	—

Note:
1. ZQ0 is pulled up to VDDQ through a 240 Ω resistor.

Caution: The MachXO5-55TD and MachXO5-55TDQ Evaluation Boards are designed to support ×16 bits with default population but are reserved to support x24 bits configuration if you change the memory to a x32 LPDDR4 device.

10. Generating the Programming File

The demo project on the MachXO5-55TD and MachXO5-55TDQ Evaluation Rev A Boards can be downloaded from the corresponding board webpages. To generate the Bitstream (.bit) file:

1. Open the Lattice Radiant software Version 2024.2.1 or later for MachXO5-55TD devices and 2025.1 or later for MachXO5-TDQ devices.
2. Make sure the licenses below are supported by the Lattice Radiant software:
   For MachXO5-NX-55TD devices
   - Device License:
     - LSC_CTL_LFMXO5-55TD for the Lattice Radiant software and Lattice Propel 2025.1 or earlier
     - LSC_CTL_LFMXO5_SECURE for the Lattice Radiant software and Lattice Propel 2025.1.1 or later
   - ESFB License:
     - LSC_ESFB55D_CS (License ID: D4FF) for production shipment release (PSR) devices.

   For MachXO5-NX-55TDQ devices
   - Device License:
     - LSC_CTL_LFMXO5-55TDQ for the Lattice Radiant software and Lattice Propel 2025.1 or earlier
     - LSC_CTL_LFMXO5_SECURE for the Lattice Radiant software and Lattice Propel 2025.1.1 or later
   - ESFB License:
     - LSC_ESFB55DQ_CS (License ID: D1EF) for production shipment release (PSR) device.
3. From the **File** menu, choose **Open** > **Project**.
4. In the **Open Project** dialog box, select the *RoT_Soc.rdf* file and click **Open**, as shown in Figure 10.1. This opens the demo project.

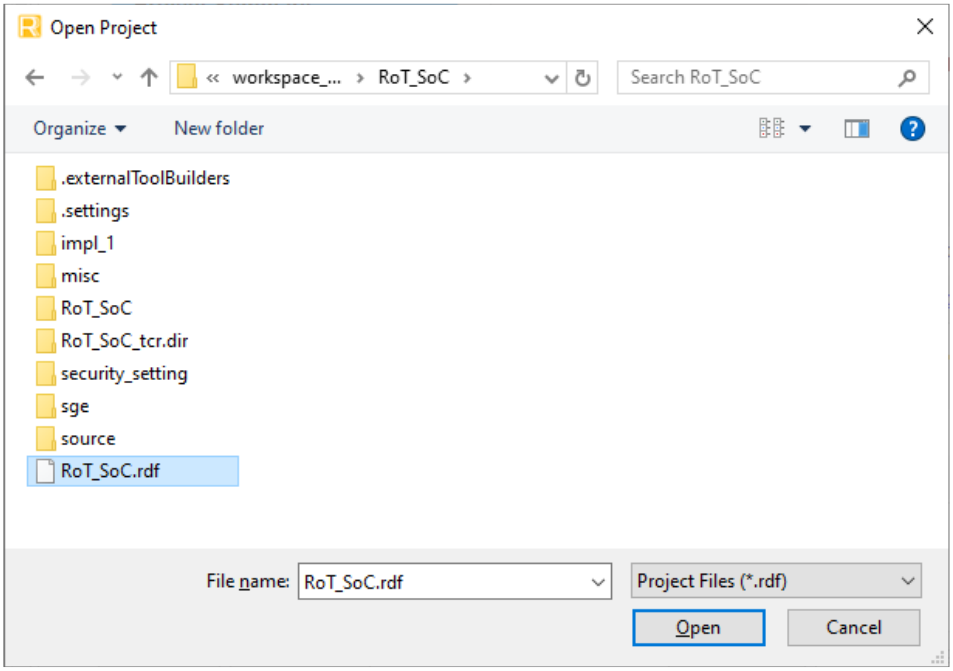

Figure 10.1. Lattice Radiant Software – Open Project Dialog Box

5. In the **Process Toolbar**, click the **Run All** icon, as shown in Figure 10.2.

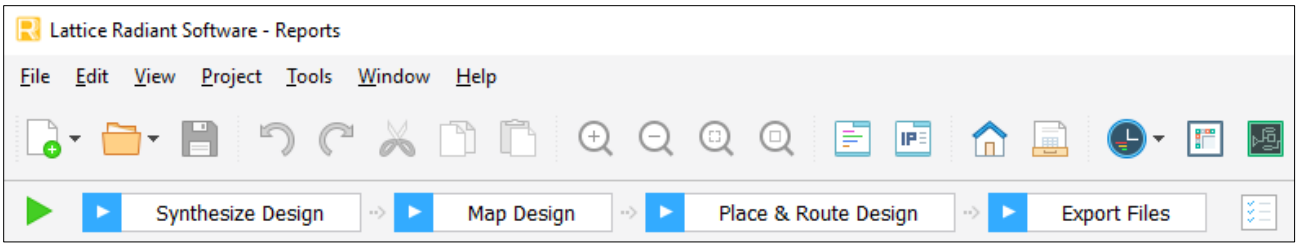

Figure 10.2. Radiant Software – Process Toolbar Initial State

Green checkmarks appear on each successfully completed step, including the generation of the file, as shown in Figure 10.3. The generated .bit file should be located in the impl_1 folder.

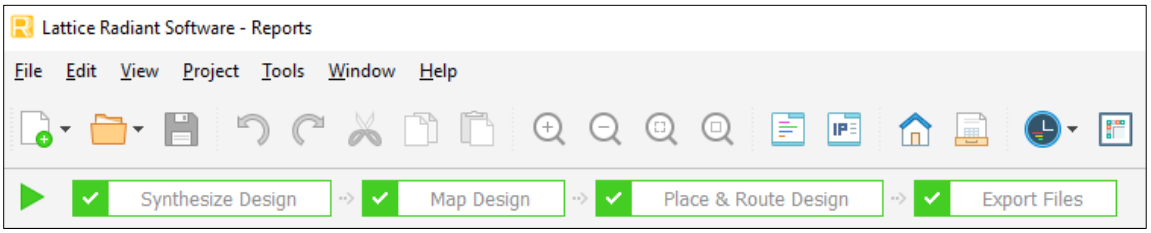

Figure 10.3. Radiant Software – State of the Processes Toolbar Completion

Note: The demo project contains the generated .bit file and shows all steps successfully completed. Click **Clean up Process** or **Force Run from Start** after right-clicking on each process button to rerun this flow.

6. Generate the customer Policy/Key/Lock .bin files for Flash provisioning upon the instruction in MachXO5-NX Root-of-Trust Device Provisioning User Guide (FPGA-TN-02333).

11. Programming the MachXO5-NX Device

The MachXO5-55TD evaluation board comes loaded with a working user design. You can re-provision the device by setting SW7-1 and SW7-3 to the OFF position and SW7-2 to the ON position followed by a power cycle or pressing the SW5 push button to toggle PROGRAMN low.

Radiant Programmer can be used to program the bitstream file to the MachXO5-NX embedded flash after necessary files are generated. The details are shown in the Generating the Programming File section. The Radiant Programmer is integrated into the Lattice Radiant software and is also available as a standalone version.

To program the MachXO5-NX embedded flash, you need to erase the default demo design shipped with the kit:

1. Connect the PC and the MachXO5-55TD Evaluation Board (J11) using the USB cable.
2. In the Lattice Radiant Software, click **Tools** > **Programmer**, as shown in Figure 11.1.

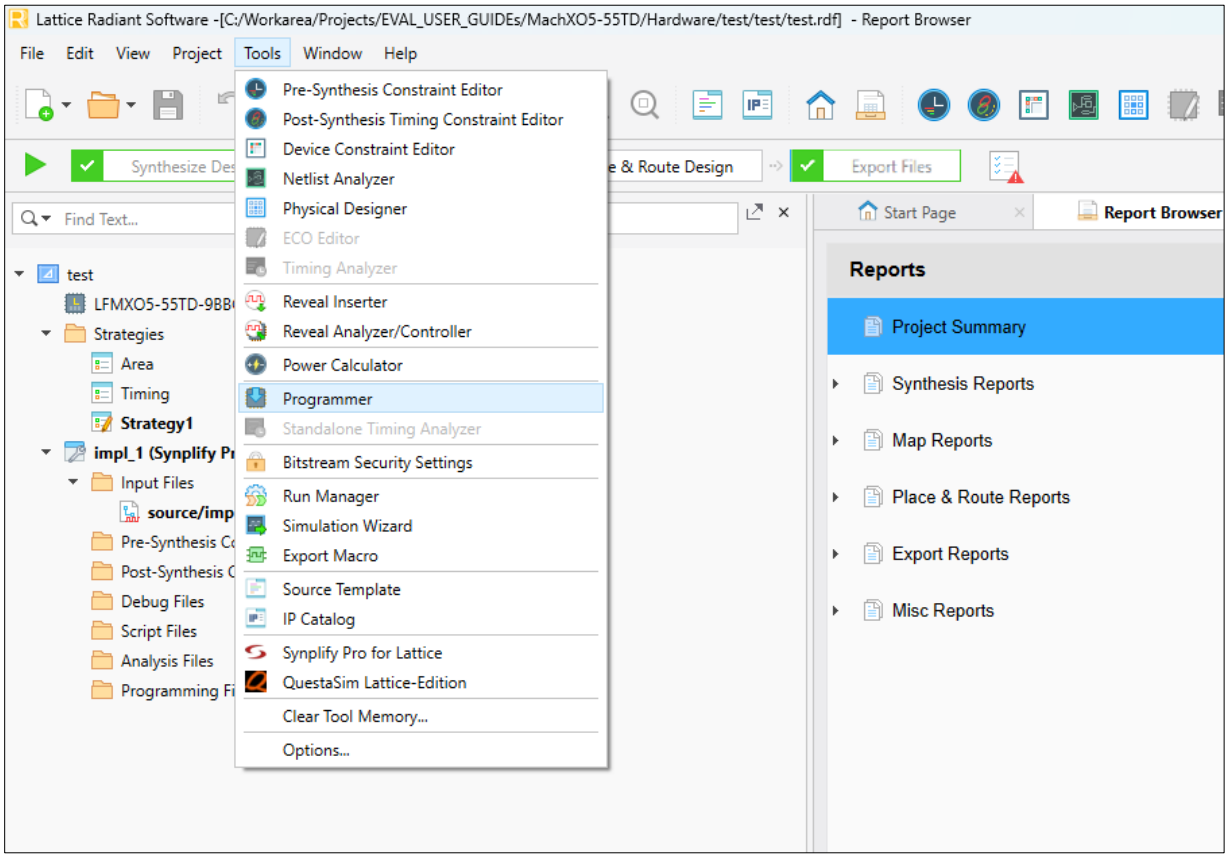

Figure 11.1. Radiant Software – Radiant Programmer

3. After the Radiant Programmer interface opens (Figure 11.2), power up the MachXO5-55TD Evaluation Board by correctly positioning the power switch **SW6**.

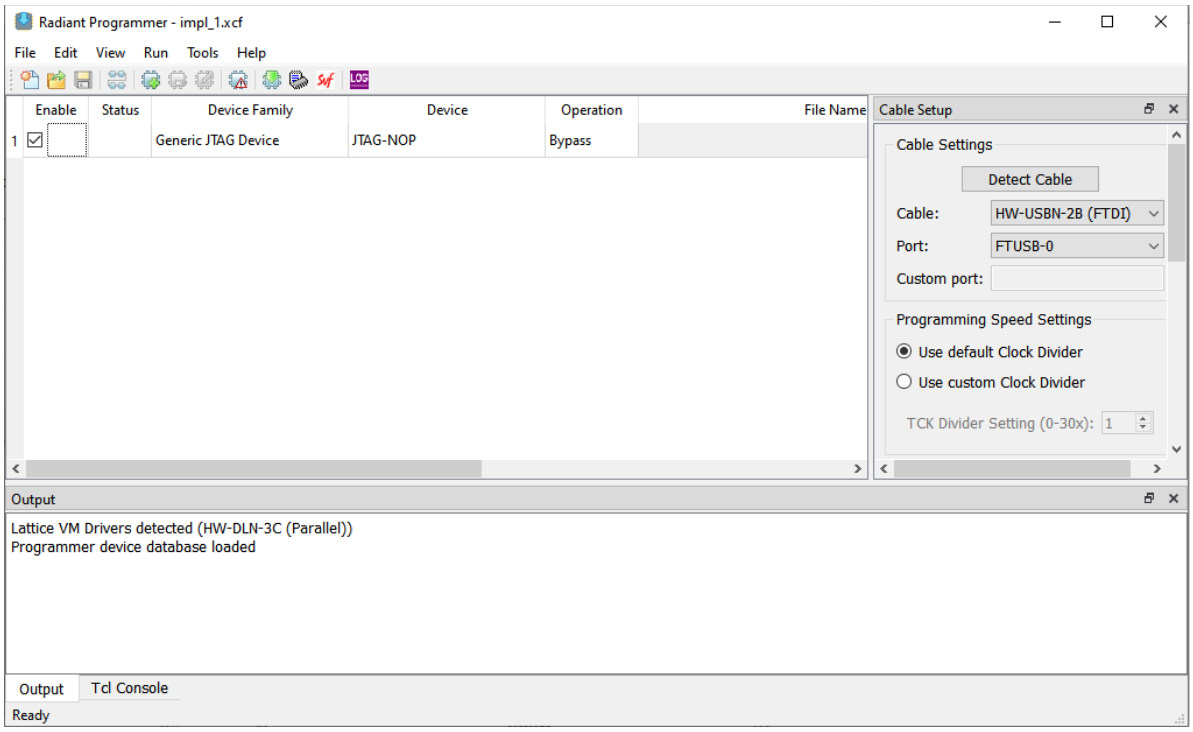

Figure 11.2. Radiant Programmer – Initial Window

4. The LFMXO5-55TD device is detected, as shown in Figure 11.3.

Figure 11.3. Radiant Programmer – Device Detection

5. Open the **Device Properties** dialog and select the example policy and user bitstream file with the respective settings shown in Figure 11.4. Click the **OK** button to close the dialog box.

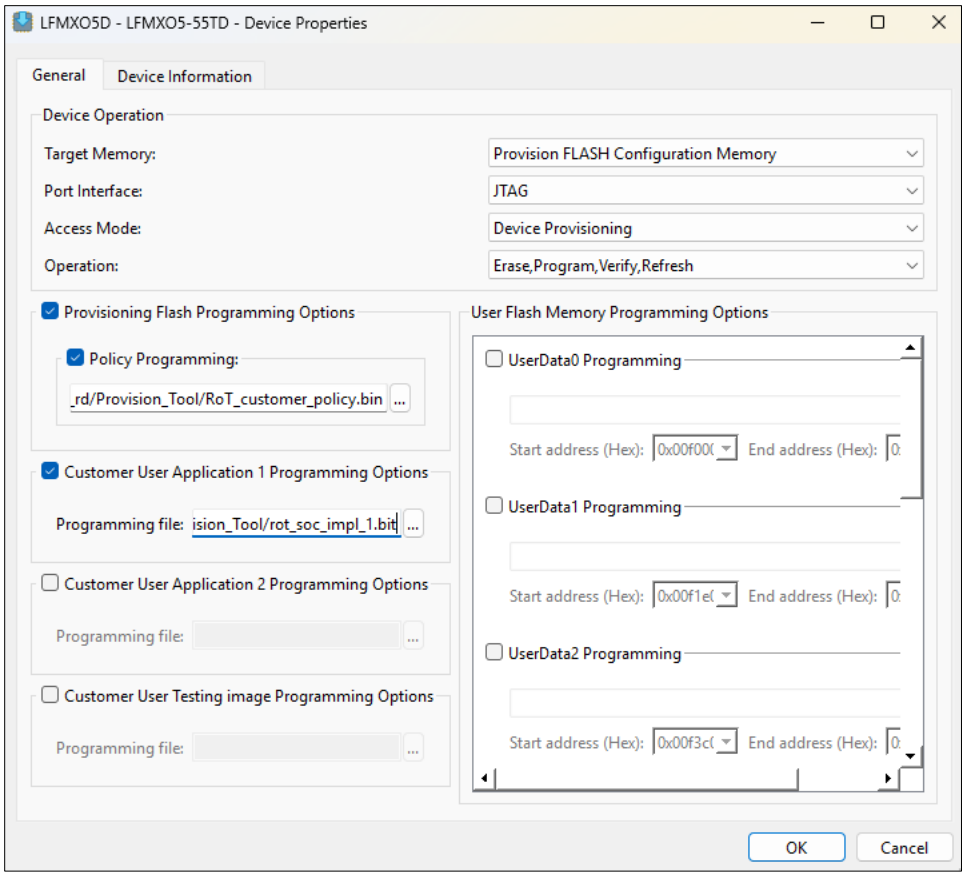

Figure 11.4. Radiant Programmer – Device Provisioning

6. Click the Program Device button to start the provisioning. The device provisioning starts immediately (Figure 11.5).

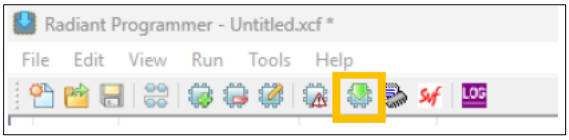

Figure 11.5. Radiant Programmer – To start the Provisioning

7. After the provisioning is completed, set SW7-1, SW7-2, and SW7-3 to the OFF position. Power cycle the board or press the SW5 push button to toggle PROGRAMN low to load the user design.

   Note: The above method is to provision and preprogram the MachXO5-NX TD device. In MachXO5-NX Root-of-Trust Device Provisioning User Guide (FPGA-TN-02333), the Provisioning using Radiant Programmer section is for MachXO5-TD device and the Provisioning using Propel Provision Tool section is for MachXO5-NX TDQ devices.

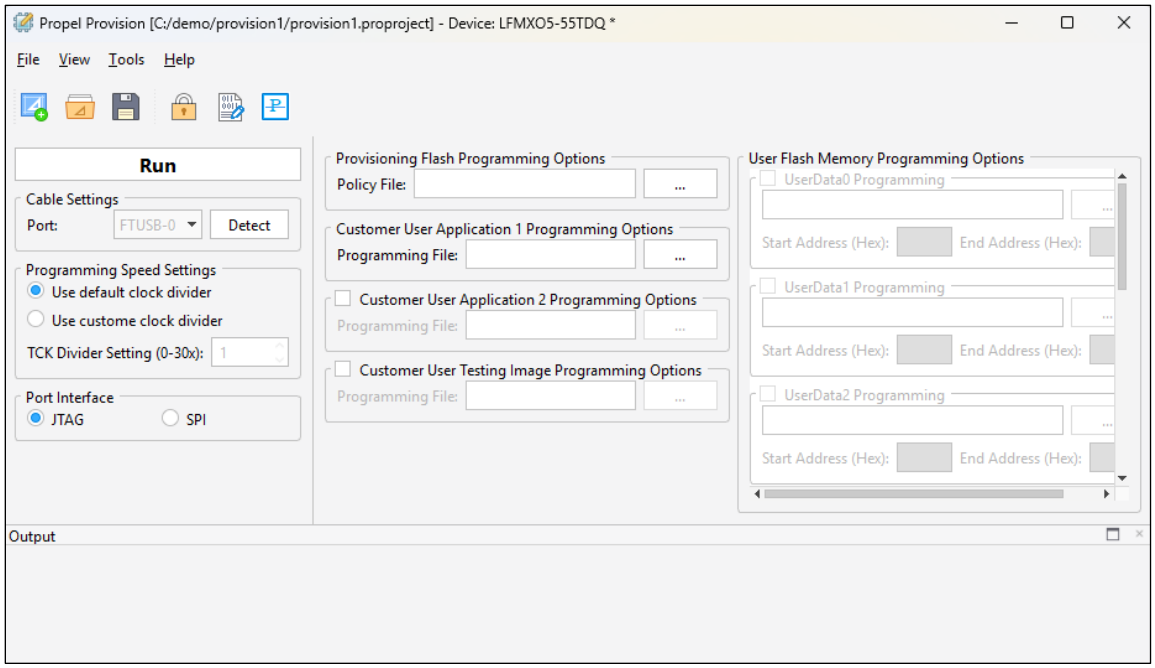

Figure 11.6. Propel Provision Tool

For MachXO5-NX TDQ devices, you can use the Propel Provision tool in Lattice Propel Builder for device provisioning (Figure 11.6). Refer to the instructions in the Using Propel Provision Tool section of MachXO5-NX Root-of-Trust Device Provisioning User Guide (FPGA-TN-02333) to create a new provision project or open an existing provision project. Perform the following upon the window shown in Figure 11.6:

1. In the **Cable Settings** section, click **Detect**. The detected port of the programming cable is listed in the **Output** pane.
2. Select the port that connects to the MachXO5-NX RoT device JTAG port from the **Port** drop-down list.
3. In the **Programming Speed Settings** section, select **Use customer clock divider** and set **TCK Divider Setting** to 3 or above.
4. In the **Port Interface** section, select either **JTAG** or **SPI**.
5. In the **Provisioning Flash Programming Options** section, click the … (browse) button to select the policy file generated in the Generating Customer Policy File section of MachXO5-NX Root-of-Trust Device Provisioning User Guide (FPGA-TN-02333). This field is mandatory for device provisioning.
6. In the **Customer User Application 1 Programming Options** section, click the **…** (browse) button to select the CUA image 1. This field is mandatory if CUT image is not selected.
7. In the **Customer User Application 2 Programming Options** section, click the **…** (browse) button to select the CUA image 2. This field is optional.
8. In the **Customer User Testing Image Programming Options** section, click the **…** (browse) button to select the CUT image. This field is optional.
9. In the **User Flash Memory Programming Options** section, the available options depend on the **Policy File** you selected. The number of available User Data Programming options follows the number of UFM sectors defined in the **Policy File**. **Start Address** and **End Address** of each UFM sector follows the start address and UFM size of the corresponding UFM sector defined in the **Policy File**.
10. Click **Run** to start device provisioning.

12. Headers and Test Connections

This section describes the MachXO5-55TD and MachXO5-55TDQ Evaluation Boards headers and test connections.

12.1. Versa Headers

The MachXO5-55TD and MachXO5-55TDQ Evaluation Boards provide two headers, J8 and J9, for expansion purposes.

Table 12.1. Versa J8 Header Pin Connections

J8 Pin Number	Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location
1	GND	—
2	NC	—
3	EXPCON_2V5[1]	—
4	EXPCON_IO29	J10
5	EXPCON_IO30	J11
6	EXPCON_IO31	K10
7	EXPCON_IO32	J17
8	EXPCON_IO33	J12
9	EXPCON_IO34	H20
10	EXPCON_IO35	H19
11	EXPCON_IO36	K11
12	EXPCON_IO37	J19
13	EXPCON_IO38	J14
14	EXPCON_IO39	J13
15	EXPCON_IO40	K16
16	EXPCON_IO41	J15
17	EXPCON_IO42	K14
18	EXPCON_IO43	K15
19	EXPCON_IO44	K12
20	EXPCON_IO45	K13
21	5VIN[1]	—
22	GND	—
23	EXPCON_2V5[1]	—
24	GND	—
25	+3.3V	—
26	GND	—
27	+3.3V	—
28	GND	—
29	EXPCON_OSC	J16
30	GND	—
31	EXPCON_CLKIN	J18
32	GND	—
33	EXPCON_CLKOUT	J20
34	GND	—
35	EXPCON_3V3[2]	—
36	GND	—
37	EXPCON_3V3[2]	—
38	GND	—

J8 Pin Number	Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location
39	EXPCON_3V3[2]	—
40	GND	—

Notes:

1. The Net is optionally connected to power source through resistor DNI.
2. The Net is optionally connected to power source through resistor DI.

Table 12.2. Versa J9 Header Pin Connections

J9 Pin Number	Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location
1	HPE_RESOUT#	H14
2	GND	—
3	EXPCON_IO0	H15
4	EXPCON_IO1	H13
5	EXPCON_IO2	F15
6	EXPCON_IO3	H16
7	EXPCON_IO4	D16
8	EXPCON_IO5	F16
9	EXPCON_IO6	C17
10	EXPCON_IO7	A16
11	EXPCON_IO8	B18
12	EXPCON_IO9	B17
13	EXPCON_IO10	F17
14	EXPCON_IO11	E17
15	EXPCON_IO12	E18
16	EXPCON_IO13	B20
17	EXPCON_IO14	F18
18	EXPCON_IO15	G16
19	GND	—
20	EXPCON_3V3[2]	—
21	EXPCON_IO16	G17
22	GND	—
23	EXPCON_IO17	C19
24	GND	—
25	EXPCON_IO18	C20
26	GND	—
27	EXPCON_IO19	D20
28	EXPCON_IO20	D19
29	EXPCON_IO21	E19
30	GND	—
31	EXPCON_IO22	F19
32	EXPCON_IO23	E20
33	EXPCON_IO24	F20
34	GND	—
35	EXPCON_IO25	G20
36	EXPCON_IO26	G19
37	EXPCON_IO27	H17

J9 Pin Number	Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location
38	CARDSEL#[1]	—
39	EXPCON_IO28	H18
40	GND	—

Notes:
1. The Net is optionally connected to power source through resistor DNI.
2. The Net is optionally connected to power source through resistor DI.

12.2. Arduino Board GPIO Headers

The board provides four headers, J2, J3, J4, and J5, for the Arduino Zero board adaptation.

Table 12.3. Arduino J2 Pin Connections

J2 Pin Number	Net Name	Arduino ZERO Board Signal	LFMXO5-55TD/Q Ball Location	Comments
1	AR_IO8	~D8/PA06	K3	—
2	AR_IO9	~D9/PA07	K2	—
3	AR_SS_IO10	~D10/PA18/SS	K1	Defaults to the SS function on the Arduino ZERO Board.
4	AR_MOSI_IO11	~D11/PA16/COPI	L3	Defaults to the COPI function on the Arduino ZERO Board.
5	AR_MISO_IO12	~D12/PA19/CIPO	L1	Defaults to the CIPO function on the Arduino ZERO Board.
6	AR_SCK_IO13	~D13/PA17/SCK	L2	Defaults to the SCK function on the Arduino ZERO Board.
7	GND	GND	—	—
8	AR_AREF	AREF/PA03	L6	AR_AREF connection to AREF through R43.
9	AR_SDA	D20/PA22/SDA	N5	Defaults to the SDA function on the Arduino ZERO Board. It is optionally connected to SDA0 through R44 (DNI).
10	AR_SCL	D21/PA23/SCL	N6	Defaults to the SCL function on the Arduino ZERO Board. It is optionally connected to SCL0 through R45 (DNI).

Table 12.4. Arduino J3 Pin Connections

J3 Pin Number	Net Name	Arduino ZERO Board Signal	LFMXO5-55TD and LFMXO5-55TDQ Ball Location	Comments
1	AR_IO0	D0/RX/PA11	K4	—
2	AR_IO1	D1//TX/PA10	K5	—
3	AR_IO2	D2/PA14	J6	—
4	AR_IO3	~D3/PA09	K7	—
5	AR_IO4	~D4/PA08	J7	—
6	AR_IO5	~D5/PA15	J8	—
7	AR_IO6	~D6/PA20	H9	—
8	AR_IO7	D7/PA21	K8	—

Table 12.5. Arduino J4 Pin Connections

J4 Pin Number	Net Name	Arduino ZERO Board Signal	LFMXO5-55TD and LFMXO5-55TDQ Ball Location	Comments
1	AR_IO14	ATN	L7	—
2	NC	IOREF	—	—

J4 Pin Number	Net Name	Arduino ZERO Board Signal	LFMXO5-55TD and LFMXO5-55TDQ Ball Location	Comments
3	AR_RESET	RESET	K2	Pin K2 should be set high by default. Avoid making the Arduino ZERO Board in Reset status when connected.
4	+3.3V_AR	+3V3	—	3.3 V power supply from the Arduino ZERO Board.
5	AR_5V	+5V	—	Jump to the 5 V on-board power rail through JP6.
6	GND	GND	—	—
7	GND	GND	—	—
8	+12V	VIN	—	Share with the +12 V on-board power rail.

Note:
If JP6 is installed, a 5 V power can be supplied from either the Arduino board, or the MachXO5-55TD or MachXO5-55TDQ Evaluation Board. With JP6 removed, each board needs its own 5 V power.

Table 12.6. Arduino J5 Pin Connections

J5 Pin Number	Net Name	Arduino ZERO Board Signal	LFMXO5-55TD and LFMXO5-55TDQ Ball Location	Comments
1	AR_AD0	D14/ADC0/PA02	M1	Defaults to ADC0 on Arduino ZERO Board.
2	AR_AD1	D15/ADC1/PB08	M2	Defaults to ADC1 on Arduino ZERO Board.
3	AR_AD2	D16/ADC2/PB09	M3	Defaults to ADC2 on Arduino ZERO Board.
4	AR_AD3	D17/ADC3/PA04	M4	Defaults to ADC3 on Arduino ZERO Board.
5	AR_AD4	D18/ADC4/PA05	M5	Defaults to ADC4 on Arduino ZERO Board.
6	AR_AD5	D19/ADC5/PB02	M6	Defaults to ADC5 on Arduino ZERO Board.

12.3. FPC Headers

The board provides two 50-Pin FPC headers, CN2 and CN3, for board signal extension. Each header got 14 pairs of LVDS or SLVS signals for high-speed data transmitter or receiver. CN2 and CN3 are designed to support the loopback test with a standard 50-pin FPC cable.

Table 12.7. FPC Header Pin Connections

CN2 at the Top Side			CN3 at the Bottom Side		
Pin Number	Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location	Pin Number	Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location
1	NC	—	50	NC	—
2	TP3	—	49	TP4	—
3	TP3	—	48	TP4	—
4	TP3	—	47	TP4	—
5	TP3	—	46	TP4	—
6	NC	—	45	NC	—
7	SLVS_TP1	V6	44	SLVS_TP2	W6
8	GND	—	43	GND	—
9	SLVS_DP26	W4	42	SLVS_DP24	Y2
10	SLVS_DN26	Y4	41	SLVS_DN24	Y3
11	GND	—	40	GND	—
12	SLVS_DP27	W5	39	SLVS_DP25	V1

CN2 at the Top Side			CN3 at the Bottom Side		
Pin Number	Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location	Pin Number	Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location
13	SLVS_DN27	Y5	38	SLVS_DN25	W1
14	GND	—	37	GND	—
15	SLVS_DP0	W13	36	SLVS_DP12	U13
16	SLVS_DN0	W12	35	SLVS_DN12	V13
17	GND	—	34	GND	—
18	SLVS_DP1	V11	33	SLVS_DP13	R13
19	SLVS_DN1	U12	32	SLVS_DN13	T13
20	GND	—	31	GND	—
21	SLVS_DP2	Y12	30	SLVS_DP14	P12
22	SLVS_DN2	Y13	29	SLVS_DN14	R12
23	GND	—	28	GND	—
24	SLVS_DP3	W9	27	SLVS_DP15	U10
25	SLVS_DN3	W10	26	SLVS_DN15	V10
26	GND	—	25	GND	—
27	SLVS_DP4	V12	24	SLVS_DP16	U9
28	SLVS_DN4	W11	23	SLVS_DN16	V9
29	GND	—	22	GND	—
30	SLVS_DP5	P13	21	SLVS_DP17	R9
31	SLVS_DN5	P14	20	SLVS_DN17	T9
32	GND	—	19	GND	—
33	SLVS_DP6	Y10	18	SLVS_DP18	W7
34	SLVS_DN6	Y11	17	SLVS_DN18	W8
35	GND	—	16	GND	—
36	SLVS_DP7	Y8	15	SLVS_DP19	N9
37	SLVS_DN7	Y9	14	SLVS_DN19	P9
38	GND	—	13	GND	—
39	SLVS_DP8	Y6	12	SLVS_DP20	N7
40	SLVS_DN8	Y7	11	SLVS_DN20	N8
41	GND	—	10	GND	—
42	SLVS_DP9	U7	9	SLVS_DP21	M12
43	SLVS_DN9	V7	8	SLVS_DN21	N12
44	GND	—	7	GND	—
45	SLVS_DP10	T7	6	SLVS_DP22	R11
46	SLVS_DN10	R7	5	SLVS_DN22	R10
47	GND	—	4	GND	—
48	SLVS_DP11	R8	3	SLVS_DP23	P10
49	SLVS_DN11	P8	2	SLVS_DN23	P11
50	GND	—	1	GND	—

12.4. Aardvark Header (DNI)

The Aardvark I2C/SPI Host Adapter is a fast and powerful I2C bus and SPI bus host adapter through USB. It allows you to interface a Windows, Linux, or Mac OS X PC through USB to a downstream embedded system environment and transfer serial messages using the I2C and SPI protocols.

The MachXO5-55TD and MachXO5-55TDQ Evaluation Boards provide an Aardvark compatible header for customer applications. The I2C bus is optionally connected to a global I2C bus on the board.

Table 12.8. Aardvark J7 Header Pin Connections

J7 Pin Number	Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location
1	AK_SCL	M7
2	GND	—
3	AK_SDA	M8
4	+5V_I2C	—
5	AK_MISO	N1
6	+5V_SPI	—
7	AK_SCLK	N2
8	AK_MOSI	N4
9	AK_SS	N3
10	GND	—

12.5. Raspberry Pi Board GPIO Header

The MachXO5-55TD and MachXO5-55TDQ Evaluation Boards provide a 40-pin receptacle that is compatible with the GPIO header of Raspberry Pi 2/3 serial models.

Table 12.9. Raspberry Pi J6 Header Pin Connections

J6 Pin Number	Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location	J6 Pin Number	Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location
1	3.3V_RASP[1]	—	2	RASP_5V[2]	—
3	RASP_IO02	E8	4	RASP_5V[2]	—
5	RASP_IO03	F6	6	GND	—
7	RASP_IO04	G9	8	RASP_IO14	G8
9	GND	—	10	RASP_IO15	F8
11	RASP_IO17	E7	12	RASP_IO18	G7
13	RASP_IO27	E6	14	GND	—
15	RASP_IO22	E5	16	RASP_IO23	E4
17	3.3V_RASP[1]	—	18	RASP_IO24	E3
19	RASP_IO10	F7	20	GND	—
21	RASP_IO09	E2	22	RASP_IO25	F3
23	RASP_IO11	F2	24	RASP_IO08	F1
25	GND	—	26	RASP_IO07	G3
27	RASP_ID_SD	D1	28	RASP_ID_SC	E1
29	RASP_IO05	G1	30	GND	—
31	RASP_IO06	G2	32	RASP_IO12	F5
33	RASP_IO13	G6	34	GND	—
35	RASP_IO19	H4	36	RASP_IO16	H5
37	RASP_IO26	H6	38	RASP_IO20	H7
39	GND	—	40	RASP_IO21	H8

Notes:

1. The 3.3 V power is supplied from the Raspberry Pi board.

2. The 5 V power can come from either the Raspberry Pi board, or the MachXO5-55TD or MachXO5-55TDQ Evaluation Board when the jumper JP7 is installed. When jumper JP7 is not installed, each board needs its own 5 V power.

12.6. PMOD Headers

The MachXO5-55TD and the MachXO5-55TDQ Evaluation Boards provide two 12-pin receptacle headers that are compatible with the Digilent PMOD™ interface specification.

Table 12.10. J15 Header Pin Connections

J15 Pin Number	Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location	J15 Pin Number	Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location
1	PMOD0_1	K20	7	PMOD0_5	K19
2	PMOD0_2	L16	8	PMOD0_6	L17
3	PMOD0_3	L18	9	PMOD0_7	L20
4	PMOD0_4	L19	10	PMOD0_8	M18
5	GND	—	11	GND	—
6	VCCIO2	—	12	VCCIO2	—

12.7. User I2C Interface

This board provides more options for user I2C access from different LFMXO5-55TD or LFMXO5-55TDQ Wide Range I/O to multiple on-board headers. They are solid connected for target applications, but those connections to bridge SCL0/SDA0 are not populated in default. You need to customize interconnection for I2C applications across the board. For example, if you want to use an Ardvark I2C host to access the Arduino board, you can use the internal fabric logic of the LFMXO5-55TD or LFMXO5-55TDQ device to bridge AK_SCL/AK_SDA with AR_SCL/AR_SDA. Or, you can add bridge resistors according to Table 12.11 to connect all of them to SCL0/SDA0 for bridge interconnections on-board without involving the FPGA. You also need to set up the design with the tri-state mode for output high with pull-up resistors. If there is no pull-up setup on the counterpart boards or internal GPIOs of FPGA, you can add JP12 and JP13 to leverage FTDI's I2C pull up R33 and R34 for SCL0/SDA0. Note that the multi-drives should be disabled for FTDI_SCL/FTDI_SDA in this case. You can add JP9 to disable FTDI output and force FPGA output High-Z from ball location A19/A18.

By adding JP12 and JP13, you can also access FPGA I2C configure interface from those extension boards with I2C host through SCL0/SDA0, which provides the flexibility to update the bitstream from an extension board in some applications.

Table 12.11. I2C Connections

Extend header	LFMXO5-55TD and LFMXO5-55TDQ Bank	LFMXO5-55TD and LFMXO5-55TDQ Ball Location for JTAG	Net Name	Bridge Resistor to SCL0/SDA0
Versa Header (J9)	1	B20	EXPCON_IO13	R35 (DNI)
		G16	EXPCON_IO15	R37 (DNI)
Aardvark Header (J7)	6	M7	AK_SCL	R60 (DNI)
		M9	AK_SDA	R59 (DNI)
Arduino Header (J2)	6	N5	AR_SCL	R45 (DNI)
		N6	AR_SDA	R44 (DNI)
Raspberry Pi Header (J6)	7	E1	RASP_ID_SC	R85 (DNI)
		D1	RASP_ID_SD	R87 (DNI)
Raspberry Pi Header (J6)	7	F6	RASP_IO03	R96 (DNI)
		E8	RASP_IO02	R84 (DNI)

12.8. ADC and Potentiometer

There are two dedicated ADC input pairs for LFMXO5-55TD and LFMXO5-55TDQ devices. The MachXO5-55TD and MachXO5-55TDQ Evaluation Boards provide multiple application options. For default population, one pair of ADC0 is used to measure the core VCC voltage drop through a 10 mΩ resistor R112. Therefore, the core VCC current is calculable, as shown in Figure 12.1. Positive input of another pair ADC1 is connected to a 10 kΩ Trimmer Potentiometers (POT1) that provides voltage variation from 0 V to selectable VCCIO4, as shown in Figure 12.2. The negative input of ADC1 is grounded through 1 kΩ resistor.

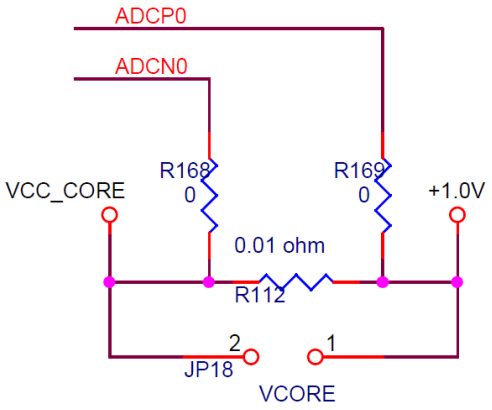

Figure 12.1. Circuit Design for ADC0

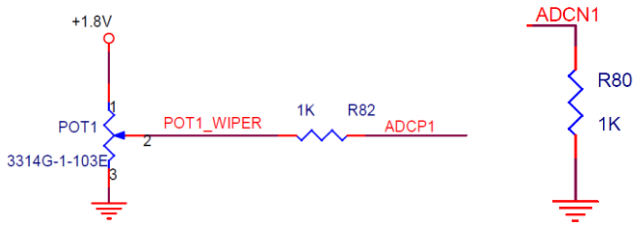

Figure 12.2. Circuit Design for ADC1

Rotate the Trimmer clockwise to decrease the voltage, as shown in Figure 12.3. To increase the voltage to ADCP1, rotate the POT counterclockwise.

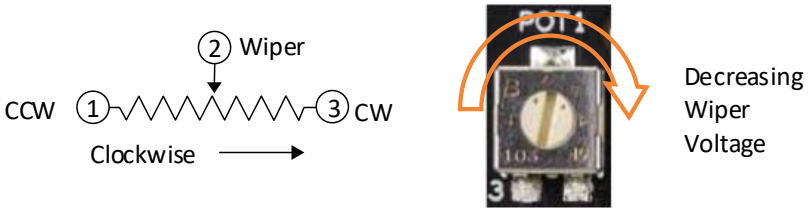

Figure 12.3. Trimmer Wiper Description

13. LEDs and Switches

LEDs and switches of the MachXO5-55TD and MachXO5-55TDQ Evaluation Boards that can be used in demonstrations and customer designs are described in this section.

13.1. 8-Position DIP Switch

Four LFMXO5-55TD or LFMXO5-55TDQ pins are connected to the four switches of SW1, as shown in the circuit design in Figure 13.1. The DIP switches are connected to logic level 0 when in the ON position, as shown in Figure 13.2.

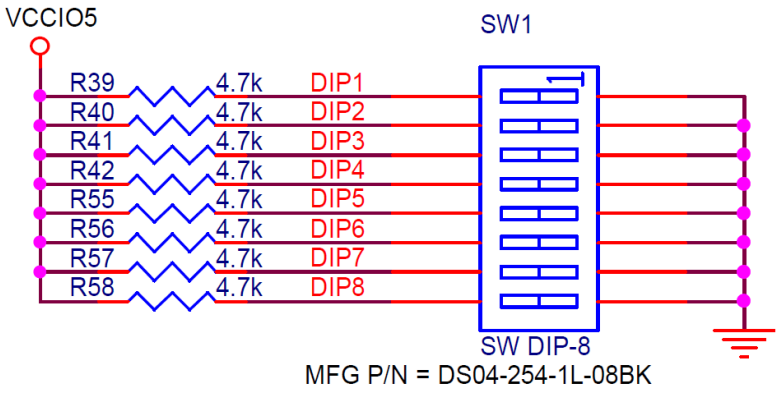

Figure 13.1. Eight-Position DIP Switch Circuits

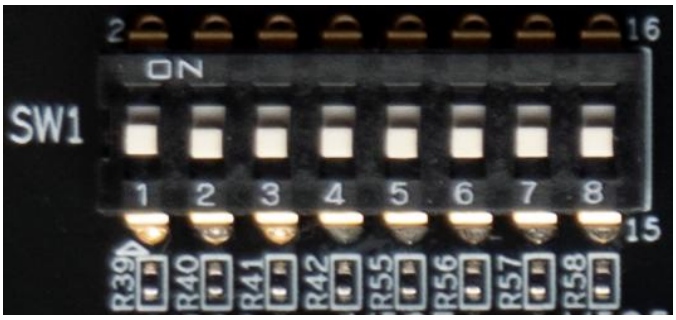

Figure 13.2. Eight-Position DIP Switch

One side of each switch is connected to GPIOs within the VCCIO5 bank and pulled up through 4.7 kΩ resistors. The other side is grounded. The designated pins are connected, as shown in Table 13.1.

Table 13.1. Four-Position DIP Switch Signals

Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location	SW1 DIP Switch Position	4.7 kΩ Pull-up Resistor	Logic Input Level at ON Position
DIP1	V2	1	R39	0
DIP2	V3	2	R40	0
DIP3	W2	3	R41	0
DIP4	W3	4	R42	0
DIP5	U4	5	R55	0
DIP6	V4	6	R56	0
DIP7	T4	7	R57	0
DIP8	V5	8	R58	0

13.2. General Purpose Push Buttons

The MachXO5-55TD and MachXO5-55TDQ Evaluation Boards provide four push button switches, SW2, SW3, SW4 and SW5, for demonstrations and user applications. Pressing these buttons drives a logic level 0 to the corresponding I/O pins.

Table 13.2. Push Button Switch Signals

Push Button Number	Reference name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location	Shared function	Check Conditions
PB1	SW2	K6	PCIE Reset	JP10
PB2	SW3	—	PHY devices Reset	JP3, JP5
PB3	SW4	D19	ASC Reset	JP4
PB4	SW5	G10	PROGRAMN	—

SW2 is designed for general-purpose applications. At the same time, SW2 can be used to trigger PCIE reset by adding JP10 jumper. SW3 can be used to trigger the reset sequency of SGMII PHY devices after adding JP3 and JP5 jumpers. SW4 can be used as the ASC global reset push button when JP4 is set to connect with EXPCON_IO20, which is connected to the MANDATORY_RESET signal when mated with the Lattice ASC Bridge Board. Refer to ASC Bridge Board Evaluation Board User Guide (FPGA-EB-02025) for detailed information with ASC application. SW5 can be used as the PROGRAMN push button to trigger the configuration process without power cycle. For detailed information on PROGRAMN, refer to MachXO5-NX Programming and Configuration User Guide (FPGA-TN-02271).

13.3. General Purpose LEDs

The MachXO5-55TD and MachXO5-55TDQ Evaluation Boards provide eight red LEDs that are connected to general purpose I/O. The LEDs are lighted when the output is driven Low. Table 13.3 lists the red LEDs and their associated pins.

Table 13.3. LED Signals

Red LEDs Ref Name	Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location
D1	XLED0	G11
D2	XLED1	G15
D3	XLED2	G12
D4	XLED3	H12
D5	XLED4	L14
D6	XLED5	L15
D7	XLED6	M20
D8	XLED7	M19

13.4. Test Mode Dip Switches

Three LFMXO5-55TD or LFMXO5-55TDQ pins are connected to the three switches of SW7, as shown in the circuit design in Figure 13.3. The DIP switches are connected to logic level 0 when in the ON position, as shown in Figure 13.4.

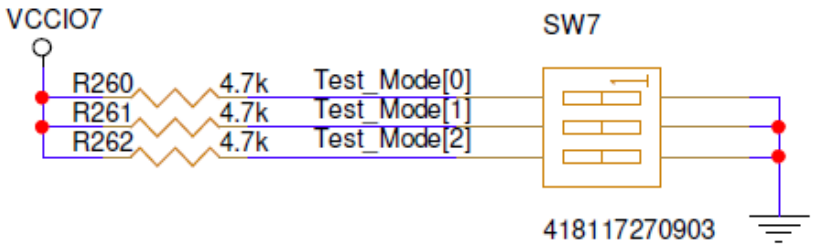

Figure 13.3. Three-Position DIP Switch Circuits

Figure 13.4. Three-Position DIP Switch

One side of each switch is connected to GPIOs within the VCCIO5 bank and pulled up through 4.7 kΩ resistors. The other side is grounded. The designated pins are connected, as shown in Table 13.4.

Table 13.4. Three-Position DIP Switch Signals

Net Name	LFMXO5-55TD and LFMXO5-55TDQ Ball Location	SW7 DIP Switch Position	4.7 kΩ Pull-up Resistor	Logic Input Level at ON Position
DIP1	J1	1	R260	0
DIP2	J2	2	R261	0
DIP3	J3	3	R262	0

14. Software Requirements

The following software are required to develop designs for the MachXO5-55TD and MachXO5-55TDQ Evaluation Boards:

- Lattice Radiant Software 2022.1.1 or later
- Lattice Radiant Programmer 2022.1.1 or later

15. Storage and Handling

Static electricity can shorten the life span of electronic components. Observe these tips to prevent damage that can occur from electrostatic discharge:

- Use antistatic precautions such as operating on an antistatic mat and wearing an antistatic wristband.
- Store the MachXO5-55TD and MachXO5-55TDQ Evaluation Boards in the provided packaging.
- Touch a metal USB housing to equalize voltage potential between you and the board.

16. Ordering Information

Table 16.1 Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
MachXO5-55TD Evaluation Board	LFMXO5-55TD-EVN	
MachXO5-55TDQ Evaluation Board	LFMXO5-55TDQ-EVN	

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Appendix A. MachXO5-55TD Evaluation Board Schematics

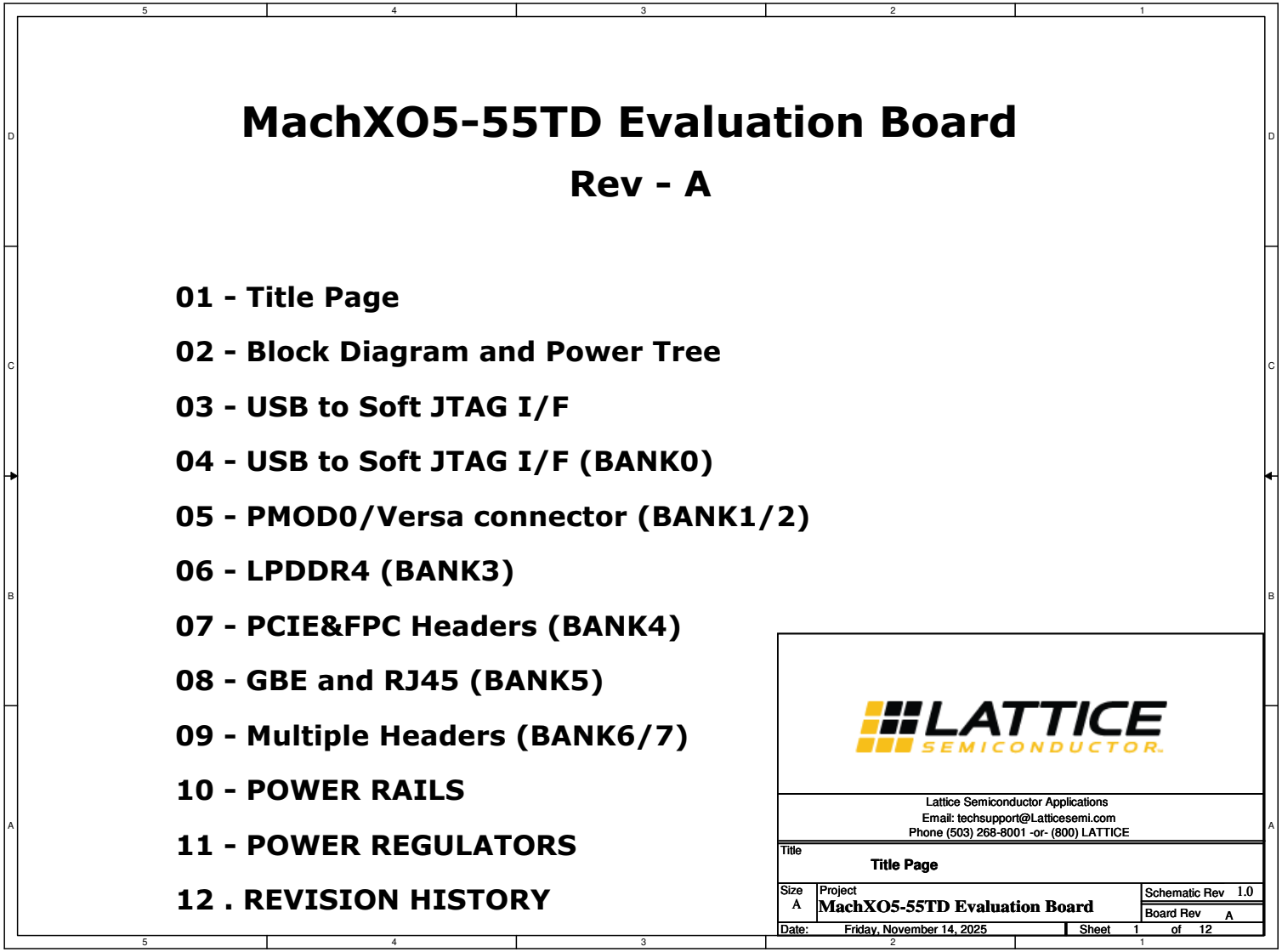

Figure A.1. Title Page

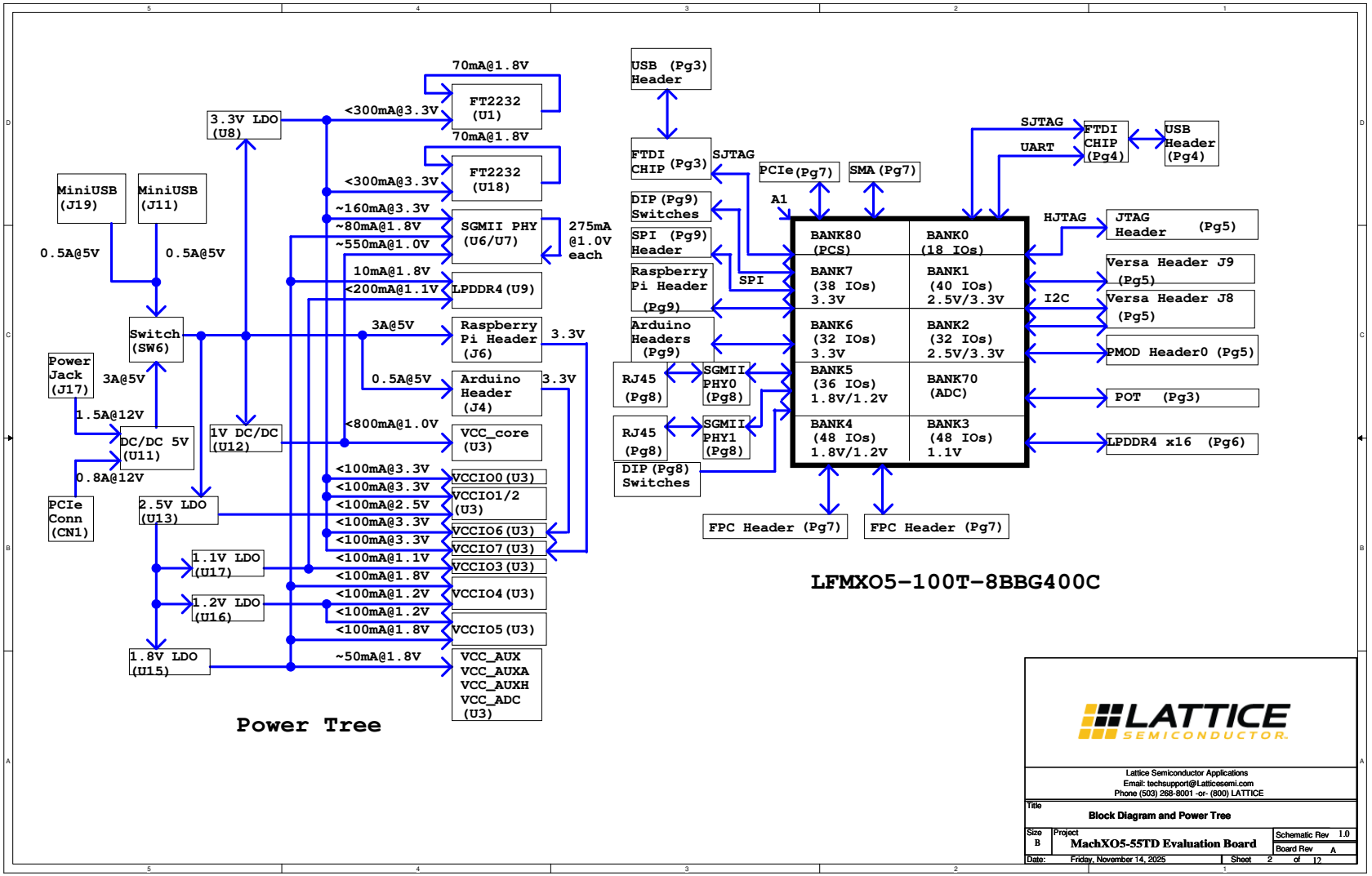

Figure A.2. Block Diagram and Power Tree

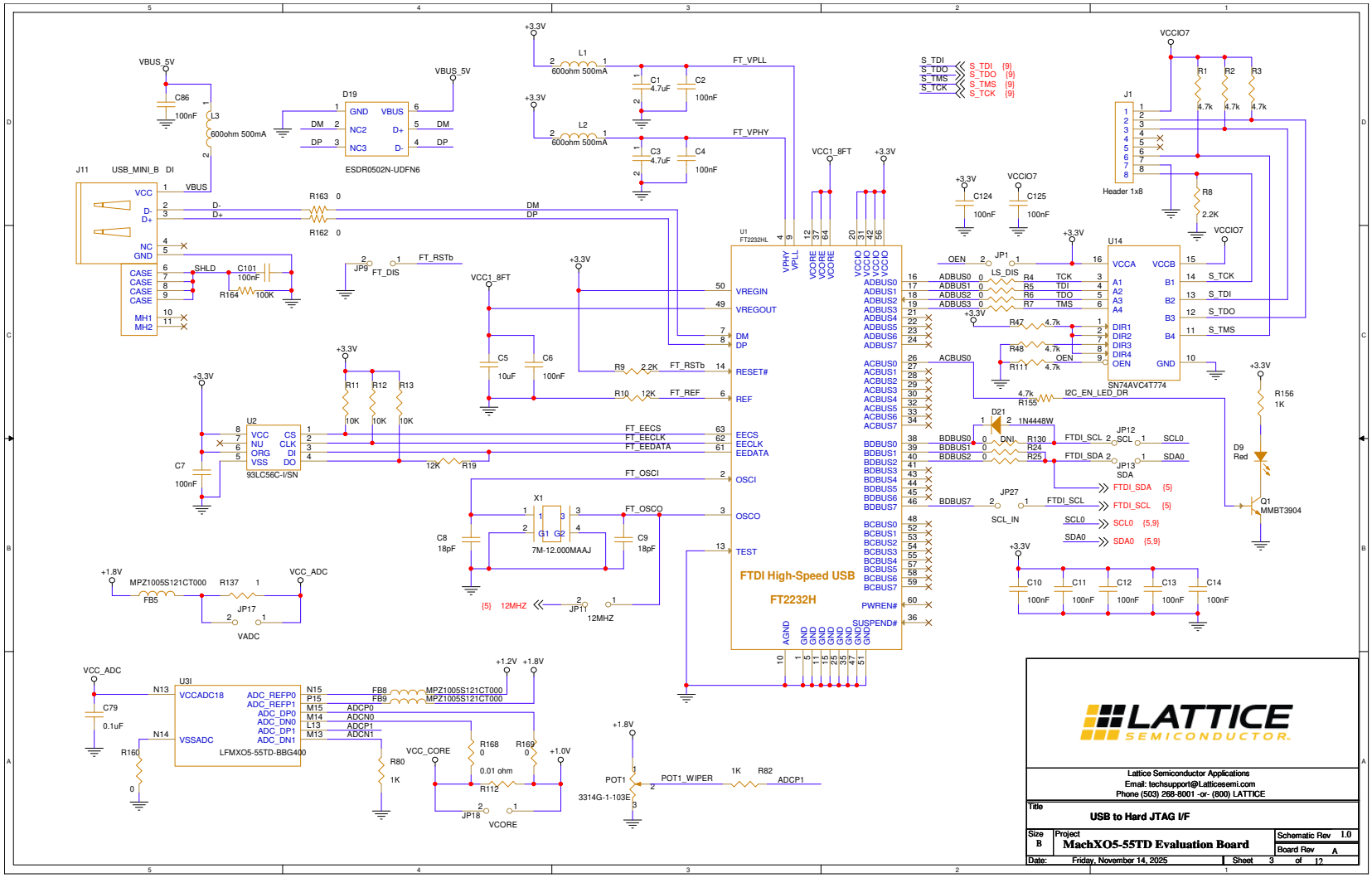

Figure A.3. USB to Hard JTAG I/F

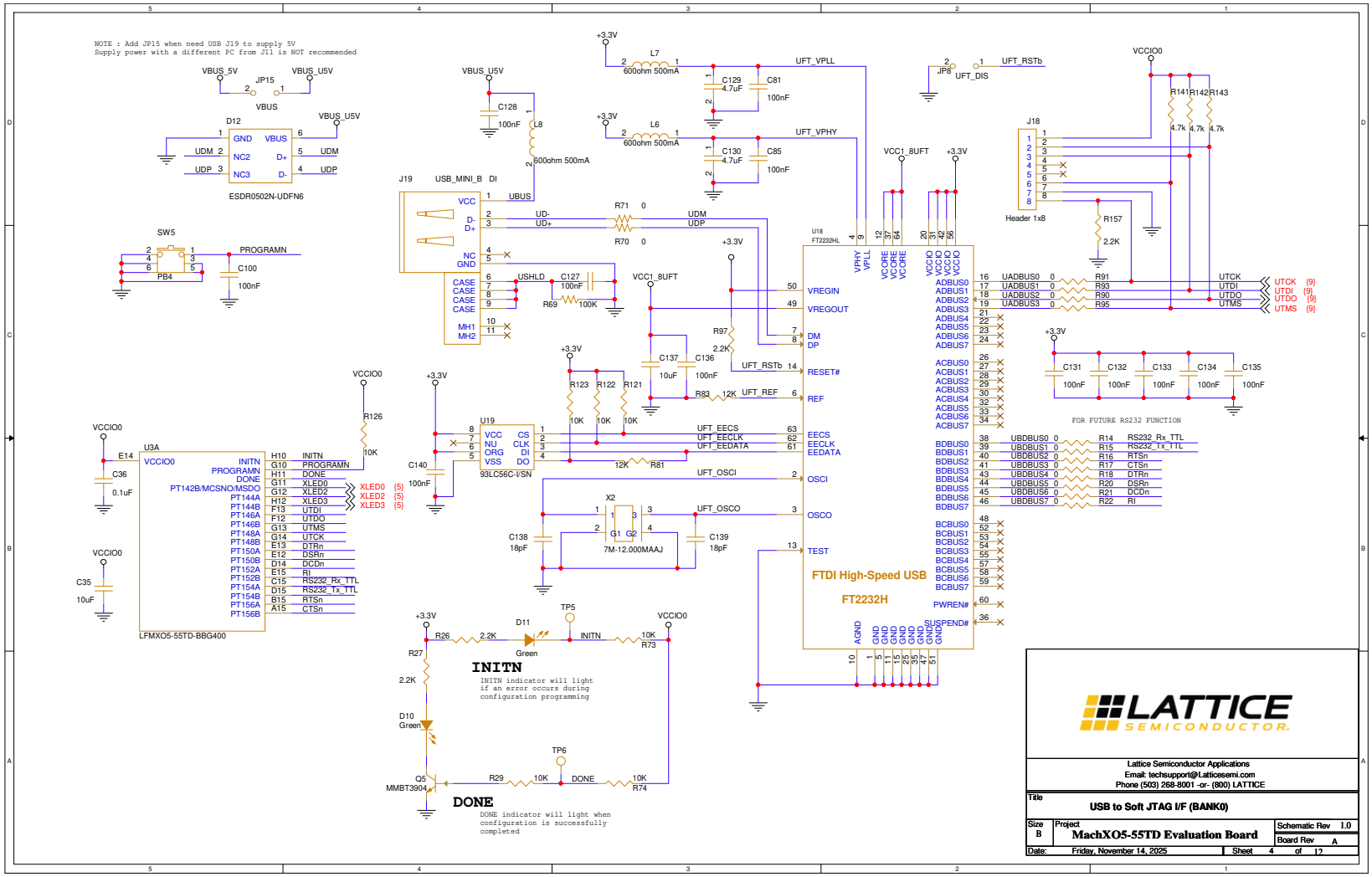

Figure A.4. USB to Soft JTAG I/F (Bank 0)

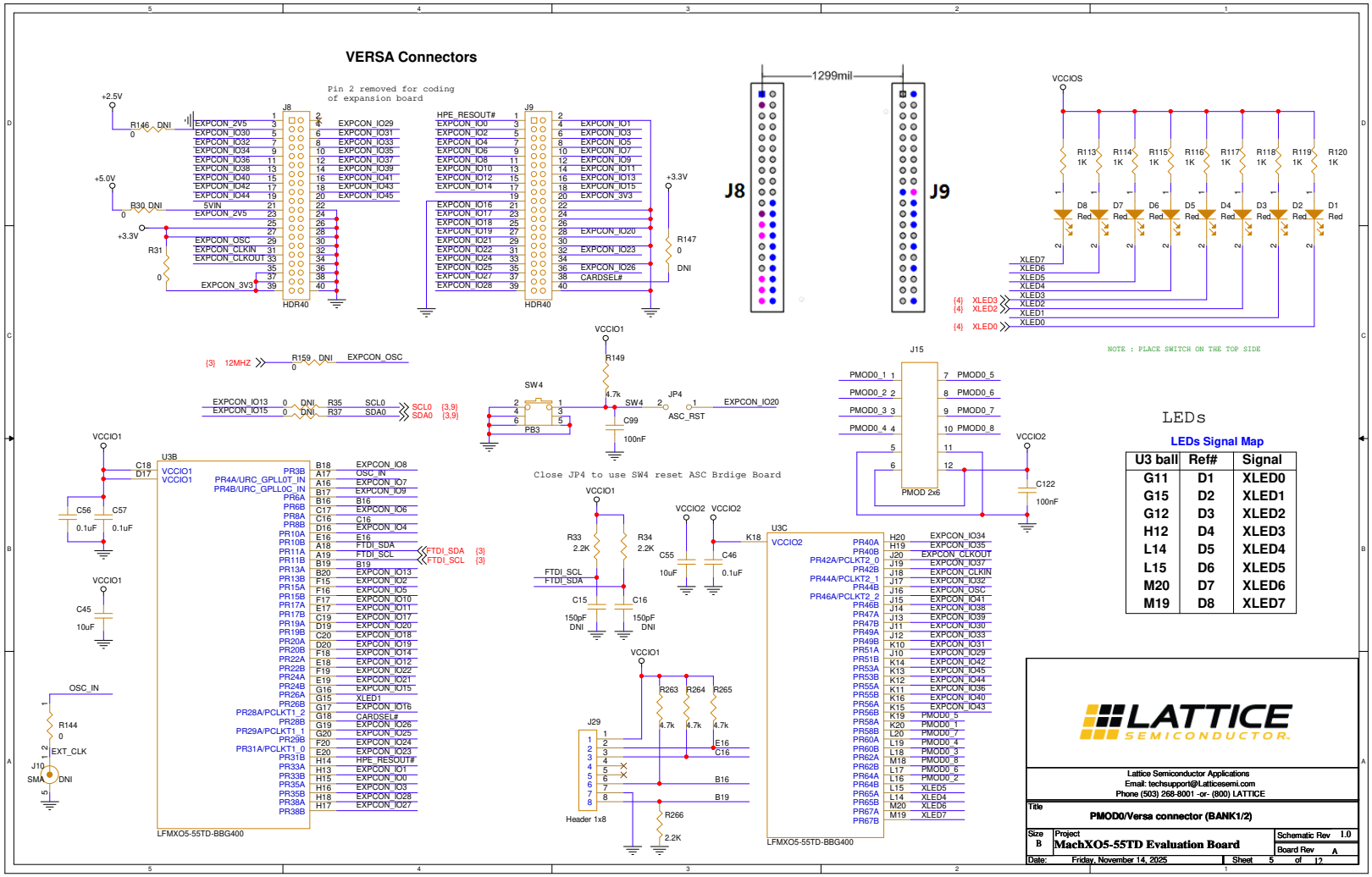

Figure A.5. PMOD0/Versa Connector (Bank 1/2)

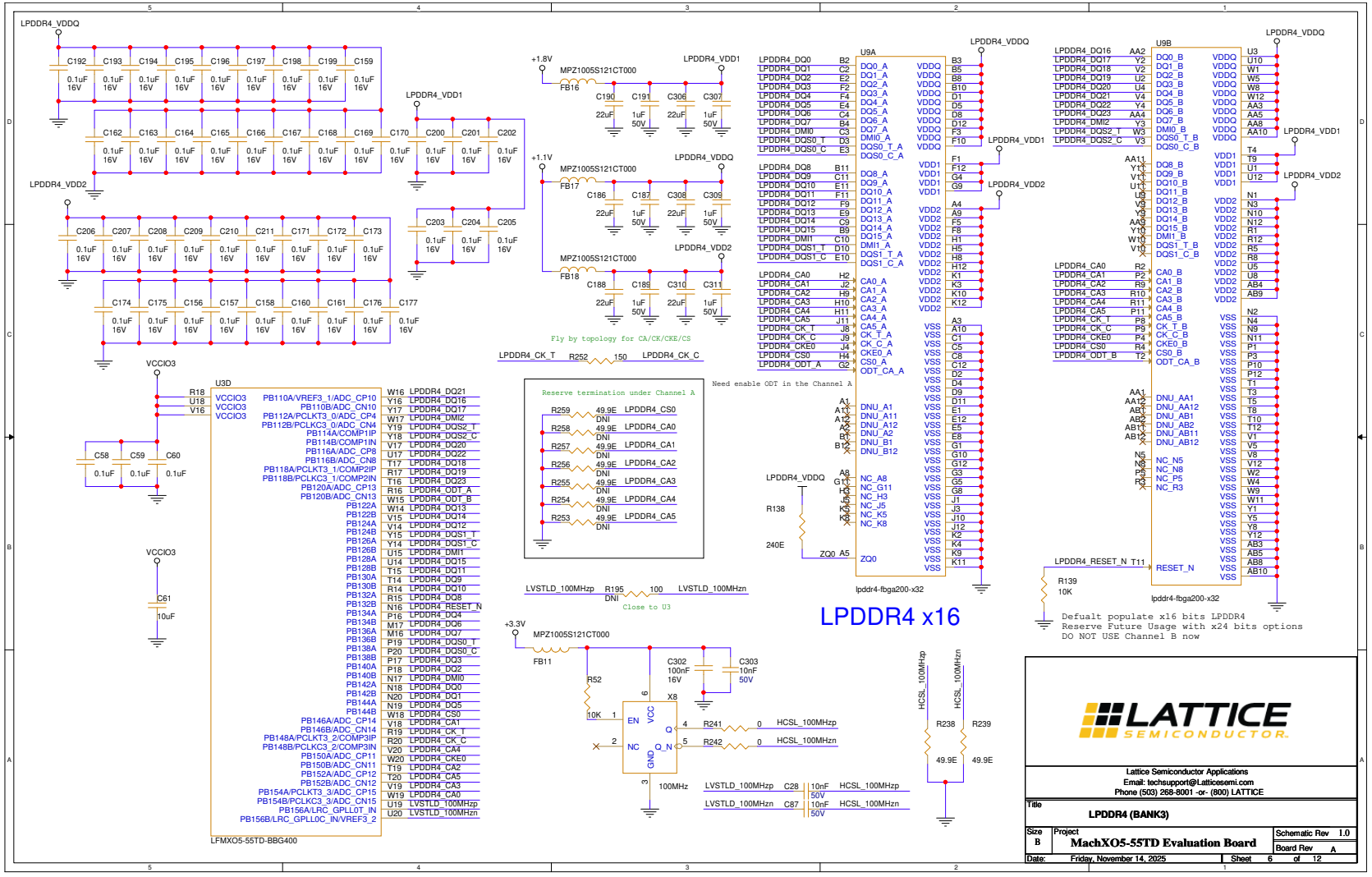

Figure A.6. LPDDR4 (Bank 3)

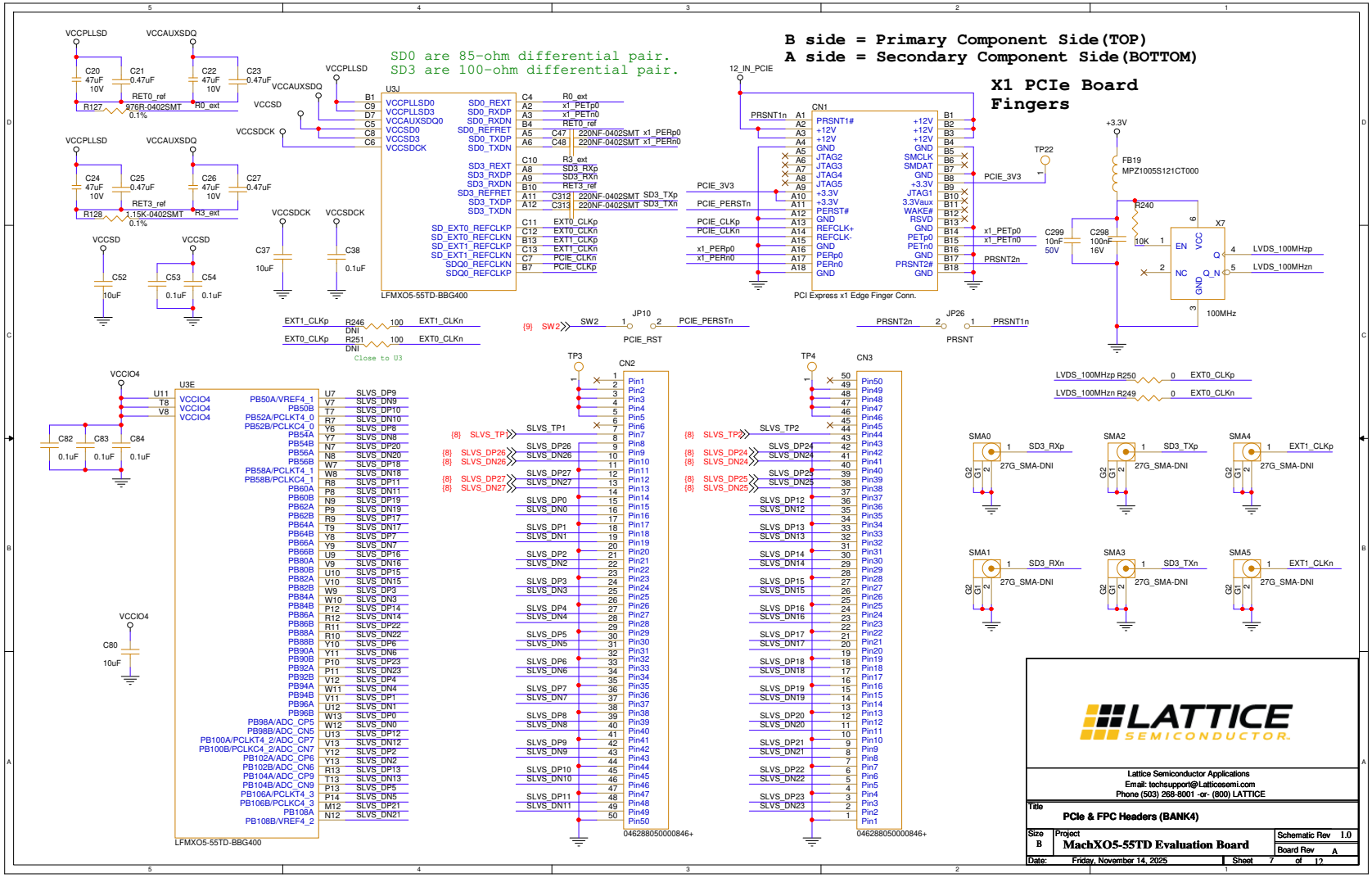

Figure A.7. PCIe & FPC Headers (Bank 4)

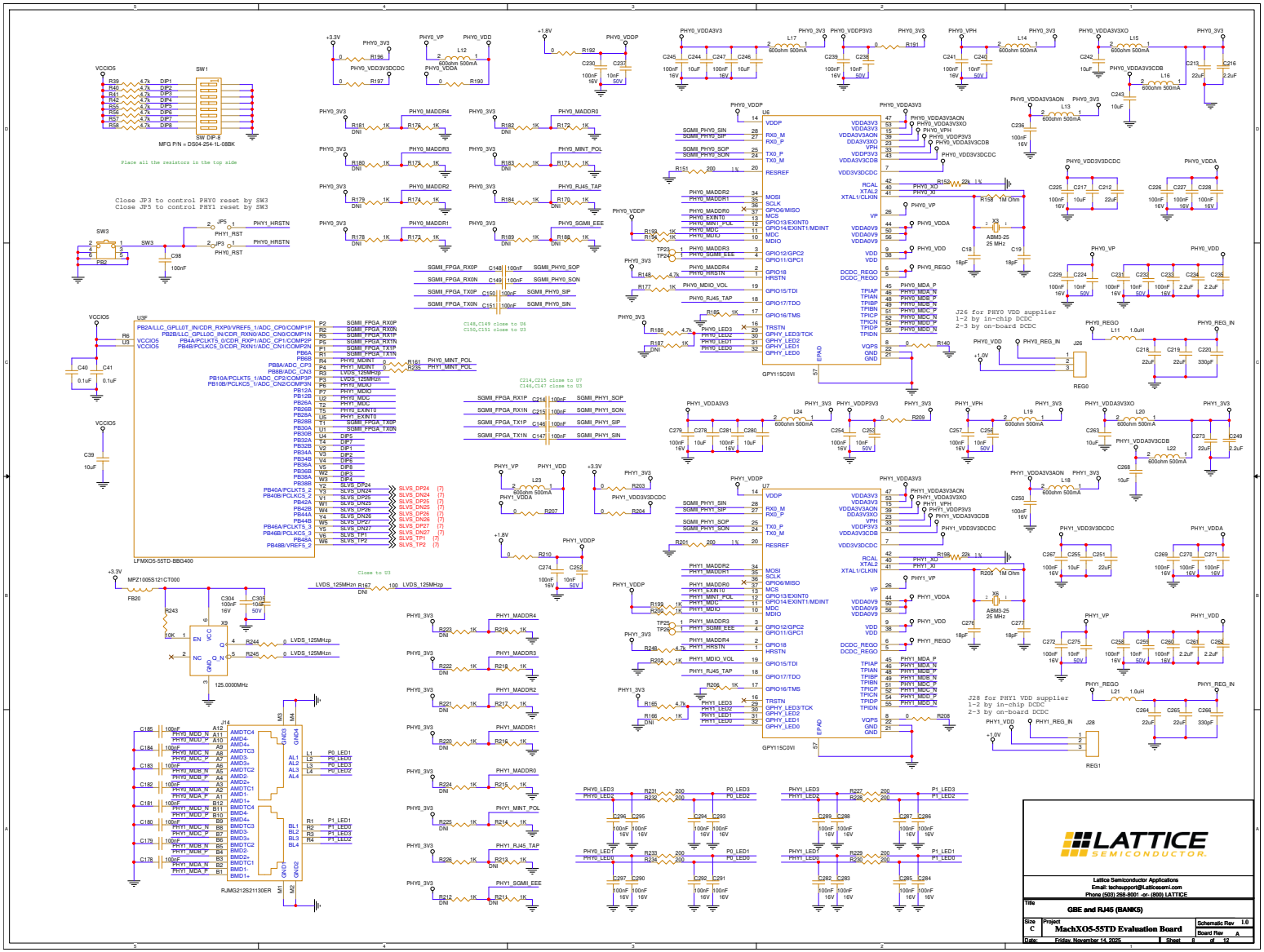

Figure A.8. Gbe and RJ45 (Bank 5)

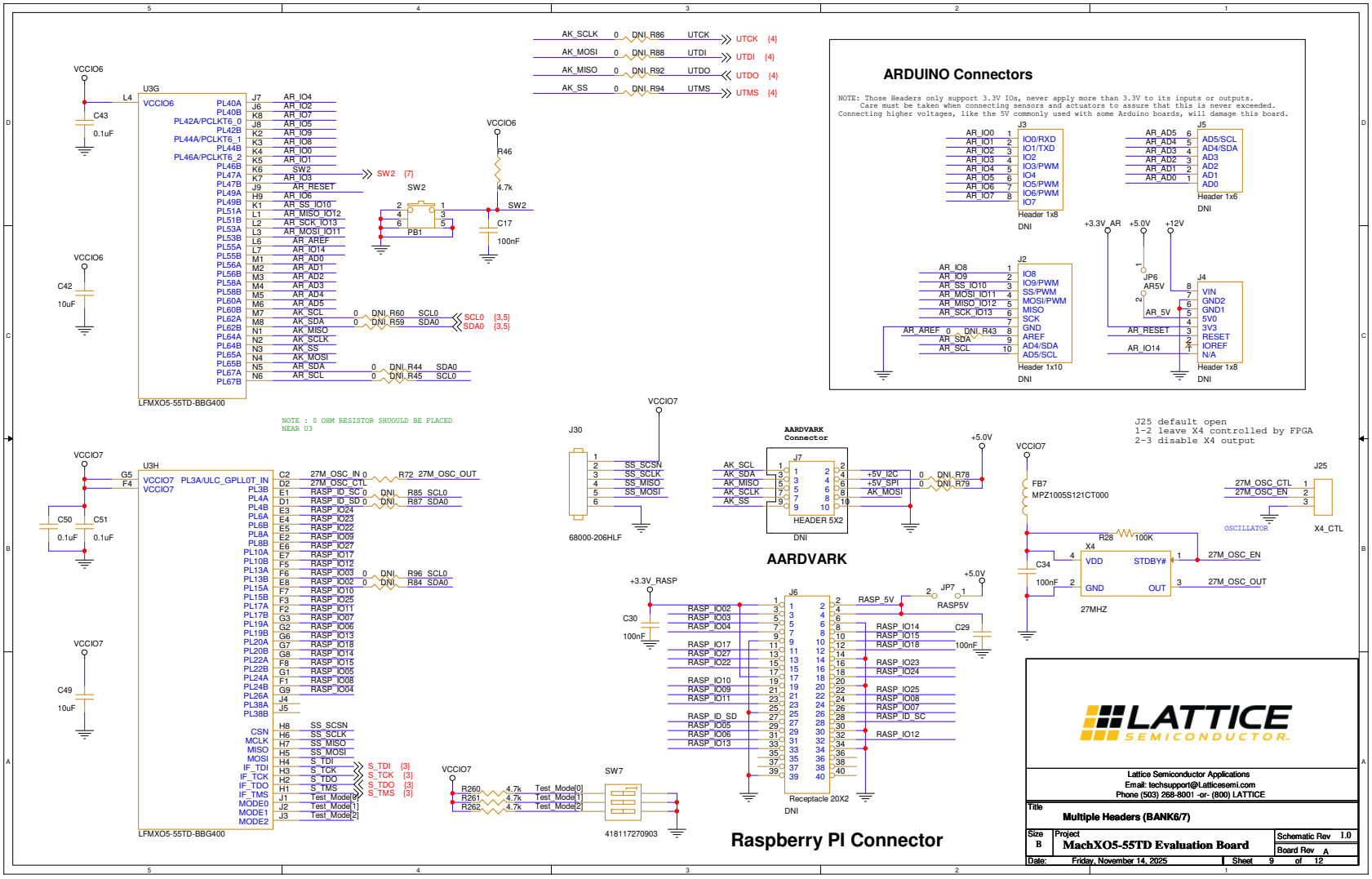

Figure A.9. Multiple Headers (Bank 6/7)

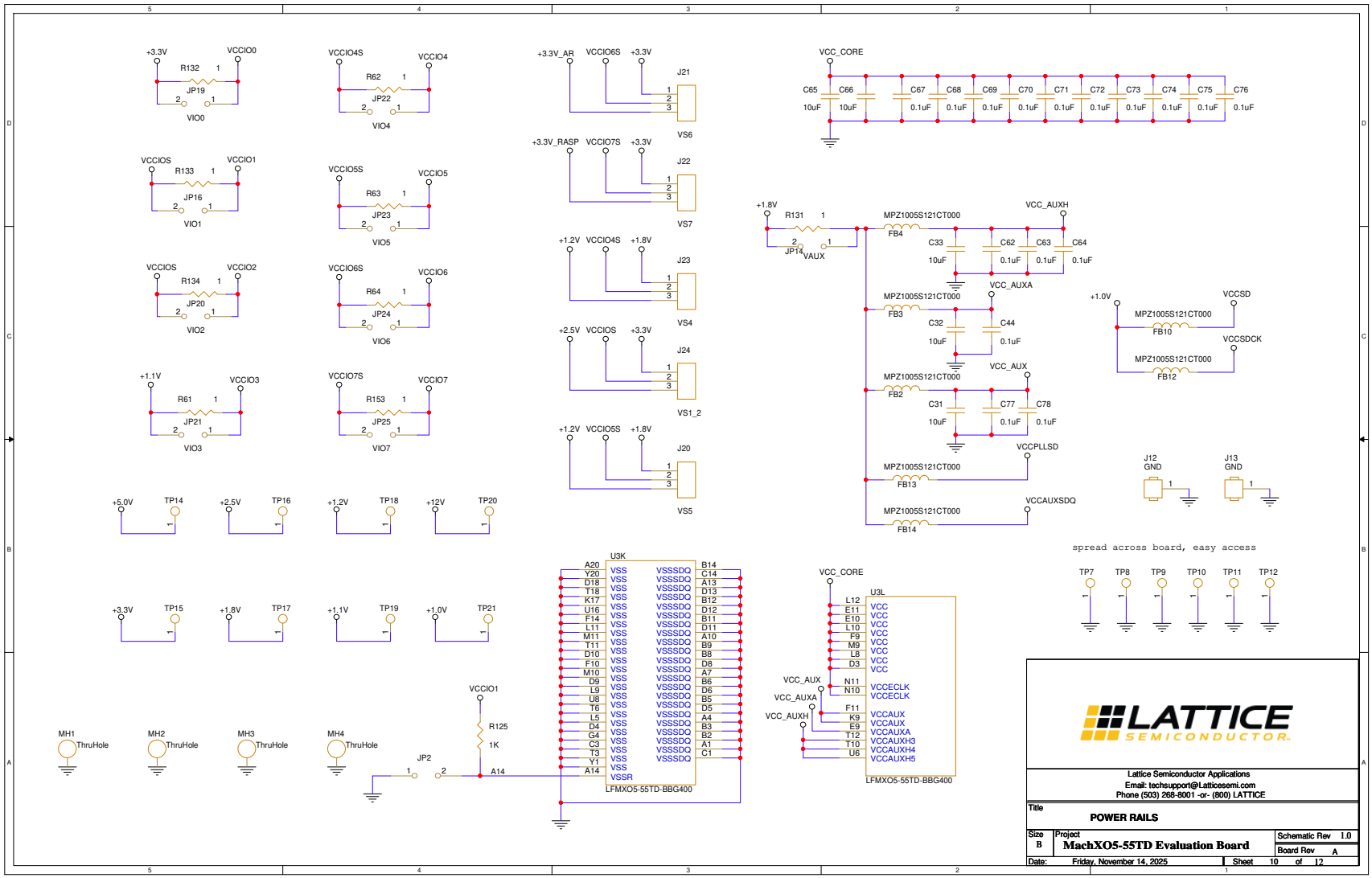

Figure A.10. Power Rails

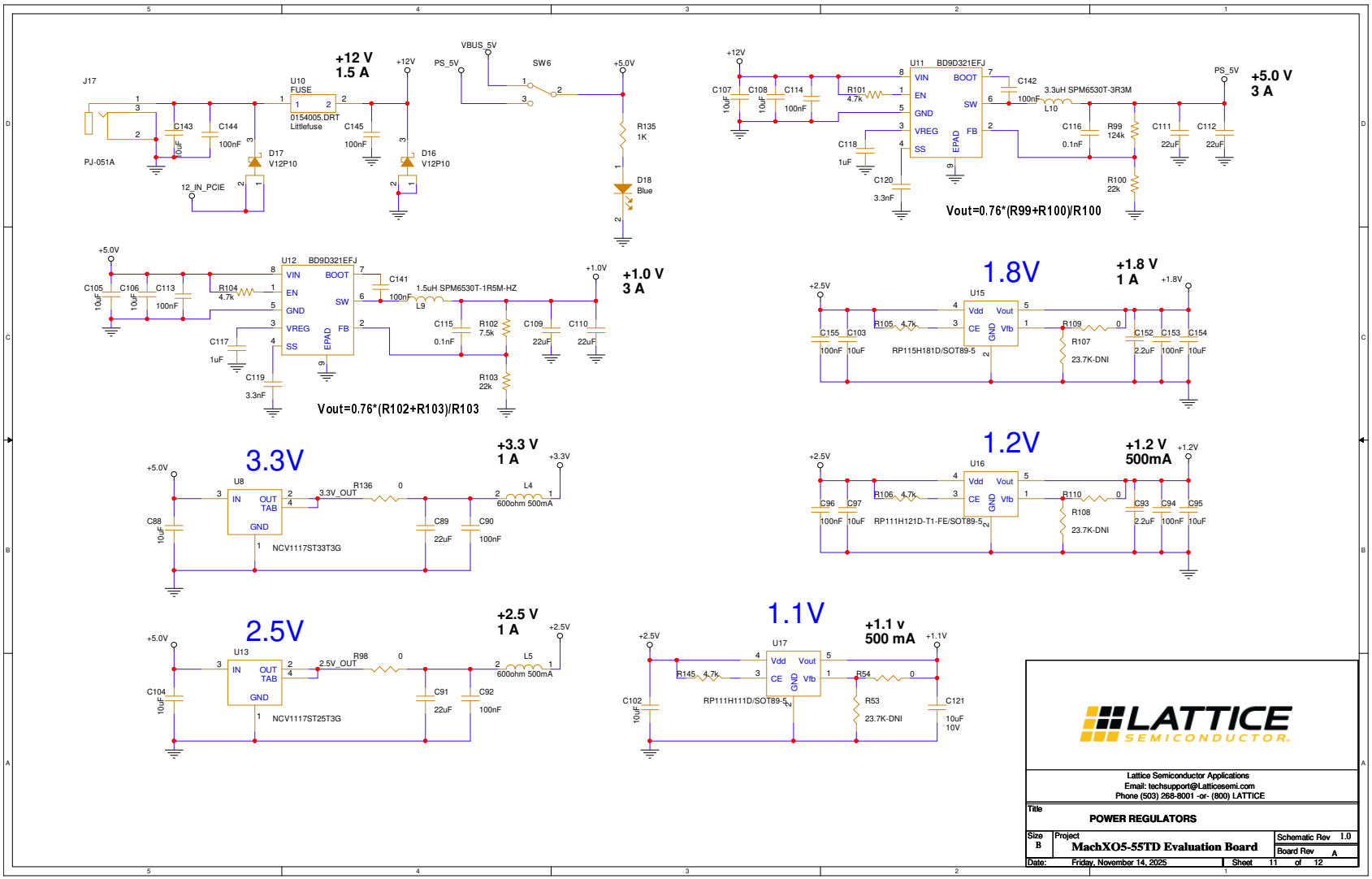

Figure A.11. Power Regulators

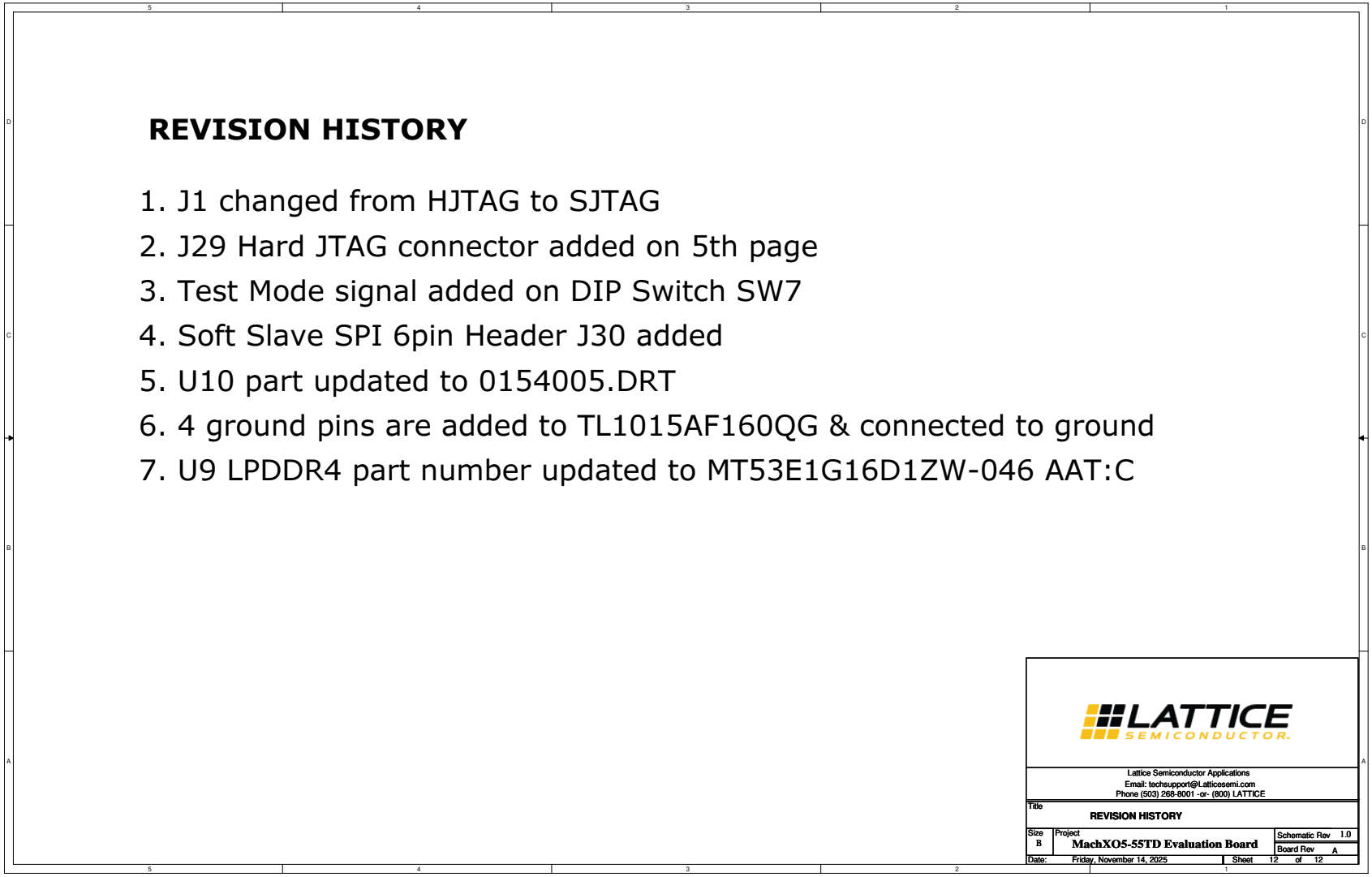

Figure A.12. Revision History

Appendix B. MachXO5-55TD Evaluation Board Bill of Materials

Item	Reference	Qty	Value	PCB Footprint	Assembly Option	Manufacturer Part Number	Manufacturer	Description
1	CN1	1	PCI Express x1 Edge Finger Conn.	PCIE-X1	DNL	—	—	PCIeX1 Edge Finger
2	CN2,CN3	2	0462880500 00846+	0462880 5000846plus	—	046288050000846+	KYOCERA AVX	CONN FFC BOTTOM 50POS 0.5MM R/A
3	C1,C3,C129,C130	4	4.7uF	C0603	—	885012106005	Wurth Elektronik	CAP CER 4.7UF 6.3V X5R 0603
4	C2,C4,C6,C7,C10,C11,C12,C13, C14,C17,C34,C81,C85,C86,C90, C92,C94,C96,C98,C99,C100, C122,C124,C125,C128,C131, C132,C133,C134,C135,C136, C140,C153,C155,C178,C179, C180,C181,C182,C183,C184, C185	42	100nF	C0402	—	GRM155R71H104 KE14D	Murata Electronics	CAP CER 0.1UF 50V X7R 0402
5	C5,C137	2	10uF	C0603	—	0603ZD106KAT2A	KYOCERA AVX	CAP CER 10UF 10V X5R 0603
6	C8,C9,C18,C19,C138,C139, C276,C277	8	18pF	C0402	—	C0402C180K3GAC TU	KEMET	CAP CER 18PF 25V C0G/NP0 0402
7	C15,C16	2	150pF	C0402	DNL	C0402C151K3RAC TU	KEMET	CAP CER 150PF 25V X7R 0402
8	C20,C22,C24,C26	4	47uF	C0603	—	GRM188R60J476 ME15D	Murata Electronics	CAP CER 47UF 6.3V X5R 0603
9	C21,C23,C25,C27	4	0.47uF	C0402	—	EMK105ABJ474KV HF	Taiyo Yuden	CAP CER 0.47UF 16V X5R 0402
10	C28,C87,C224,C232,C237, C238,C240,C252,C253,C256, C259,C275,C299,C303,C305	15	10nF	C0402	—	GRT155R71E103K E01J	Murata Electronics	CAP CER 10000PF 25V X7R 0402
11	C29,C30	2	100nF	C0402	—	04023C104KAT2A-62	KYOCERA AVX	0402 25V X7R 100 NF 10%
12	C31,C32,C33,C35,C37,C39,C42, C45,C49,C52,C55,C61,C65,C66, C80,C95,C97,C103,C121,C154, C217,C242,C243,C244,C246, C255,C263,C268,C278,C280	30	10uF	C0603	—	LMK107BJ106MAL TD	Taiyo Yuden	CAP CER 10UF 10V X5R 0603
13	C36,C38,C40,C41,C43,C44,C46, C50,C51,C53,C54,C56,C57,C58, C59,C60,C62,C63,C64,C67,C68, C69,C70,C71,C72,C73,C74,C75, C76,C77,C78,C79,C82,C83,C84	35	0.1uF	C0201	—	CC0201KRX5R8BB 104	YAGEO	CAP CER 0.1UF 25V X5R 0201
14	C47,C48,C312,C313	4	220NF-0402SMT	C0402	—	GCM155R71C224 KE02D	Murata Electronics	CAP CER 0.22UF 16V X7R 0402
15	C88,C102,C104,C105,C106, C107,C108,C143	8	10uF	C1206	—	CL31B106KBHNN NE	Samsung Electro-Mechanics	CAP CER 10UF 50V X7R 1206

Item	Reference	Qty	Value	PCB Footprint	Assembly Option	Manufacturer Part Number	Manufacturer	Description
16	C89,C91,C109,C110,C111, C112,C186,C188,C190,C212, C213,C218,C219,C251,C264, C265,C273,C306,C308,C310	20	22uF	C0603	—	CL10A226MO7JZNC	Samsung Electro-Mechanics	CAP CER 22UF 16V X5R 0603
17	C93,C152,C216,C234,C235, C249,C261,C262	8	2.2uF	C0805	—	CL21B225KPFNNNE	Samsung Electro-Mechanics	CAP CER 2.2UF 10V X7R 0805
18	C101,C127	2	100nF	C0402	—	GRM155R61C104KA88D	Murata Electronics	CAP CER 0.1UF 16V X5R 0402
19	C113,C114,C141,C142, C144,C145	6	100nF	C0402	—	GRM155R61C104KA88D	Murata Electronics	CAP CER 0.1UF 16V X5R 0402
20	C115,C116	2	0.1nF	C0603	—	CC0603JRNPO9BN101	YAGEO	CAP CER 100PF 50V C0G/NPO 0603
21	C117,C118	2	1uF	C0603	—	TMK107B7105KA-T	Taiyo Yuden	CAP CER 1UF 25V X7R 0603
22	C119,C120	2	3.3nF	C0201	—	GRM033R71E332KA12D	Murata Electronics	CAP CER 3300PF 25V X7R 0201
23	C146,C147,C148,C149,C150, C151,C214,C215	8	100nF	C0402	—	885012205018	Wurth Elektronik	CAP CER 0.1UF 10V X7R 0402
24	C156,C157,C158,C159,C160, C161,C162,C163,C164,C165, C166,C167,C168,C169,C170, C171,C172,C173,C174,C175, C176,C177,C200,C201,C202, C203,C204,C205,C206,C207, C208,C209,C210,C211	34	0.1uF	C0201	—	C0201C104K9PACTU	KEMET	CAP CER 0.1UF 6.3V X5R 0201
25	C187,C189,C191,C307,C309, C311	6	1uF	C0603	—	UMK107AB7105KA-T	Taiyo Yuden	CAP CER 1UF 50V X7R 0603
26	C192,C193,C194,C195,C196, C197,C198,C199	8	0.1uF	C0201	—	C0201C104K9PACTU	KEMET	CAP CER 0.1UF 6.3V X5R 0201
27	C220,C266	2	330pF	C0402	—	C0402C331J5GACTU	KEMET	CAP CER 330PF 50V C0G/NP0 0402
28	C225,C226,C227,C228,C229, C230,C231,C233,C236,C239, C241,C245,C247,C250,C254, C257,C258,C260,C267,C269, C270,C271,C272,C274,C279, C281,C282,C283,C284,C285, C286,C287,C288,C289,C290, C291,C292,C293,C294,C295, C296,C297	42	100nF	C0402	—	GRM155R61C104KA88D	Murata Electronics	CAP CER 0.1UF 16V X5R 0402
29	C298,C302,C304	3	100nF	C0402	—	GRM155R61C104KA88D	Murata Electronics	CAP CER 0.1UF 16V X5R 0402
30	D1,D2,D3,D4,D5,D6,D7,D8	8	Red	led_0603	—	LTST-C190KRKT	Lite-On Inc.	LED RED CLEAR CHIP SMD
31	D9	1	Red	led_0603	—	LTST-C190KRKT	Lite-On Inc.	LED RED CLEAR CHIP SMD

Item	Reference	Qty	Value	PCB Footprint	Assembly Option	Manufacturer Part Number	Manufacturer	Description
32	D10,D11	2	Green	led_0603	—	LTST-C190KGKT	Lite-On Inc.	LED GREEN CLEAR CHIP SMD
33	D12,D19	2	ESDR0502N-UDFN6	UDFN6_040	—	ESDR0502NMUTAG	onsemi	TVS DIODE 5.5VWM 6UDFN
34	D16,D17	2	V12P10	V12P10	—	V12P10-M3/87A	Vishay General Semiconductor - Diodes Division	DIODE SCHOTTKY 100V 12A TO277A
35	D18	1	Blue	led_0603	—	LTST-C190TBKT	Lite-On Inc.	LED BLUE CLEAR CHIP SMD
36	D21	1	1N4448W	1N4448W	Alternate PN : RB751S40T1G	1N4448WT	onsemi	DIODE STANDARD 75V 200MA SOD523F
37	FB2,FB3,FB4,FB5,FB7,FB8,FB9,FB10,FB11,FB12,FB13,FB14,FB16,FB17,FB18,FB19,FB20	17	MPZ1005S121CT000	FB0402	—	MPZ1005S121CT000	TDK Corporation	FERRITE BEAD 120 OHM 0402 1LN
38	JP1	1	LS_DIS	Header_1x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
39	JP2	1	JTAG_DIS	Header_1x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
40	JP3	1	PHY0_RST	Header_1x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
41	JP4	1	ASC_RST	Header_1x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
42	JP5	1	PHY1_RST	Header_1x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
43	JP6	1	AR5V	Header_1x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
44	JP7	1	RASP5V	Header_1x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
45	JP8	1	UFT_DIS	Header_1x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
46	JP9	1	FT_DIS	Header_1x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM

Item	Reference	Qty	Value	PCB Footprint	Assembly Option	Manufacturer Part Number	Manufacturer	Description
47	JP10	1	PCIE_RST	Header_1 x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
48	JP11	1	12MHZ	Header_1 x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
49	JP12	1	SCL	Header_1 x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
50	JP13	1	SDA	Header_1 x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
51	JP14	1	VAUX	Header_1 x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
52	JP15	1	VBUS	Header_1 x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
53	JP16	1	VIO1	Header_1 x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
54	JP17	1	VADC	Header_1 x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
55	JP18	1	VCORE	Header_1 x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
56	JP19	1	VIO0	Header_1 x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
57	JP20	1	VIO2	Header_1 x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
58	JP21	1	VIO3	Header_1 x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
59	JP22	1	VIO4	Header_1 x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
60	JP23	1	VIO5	Header_1 x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
61	JP24	1	VIO6	Header_1 x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM

Item	Reference	Qty	Value	PCB Footprint	Assembly Option	Manufacturer Part Number	Manufacturer	Description
62	JP25	1	VIO7	Header_1 x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
63	JP26	1	PRSNT	Header_1 x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
64	JP27	1	SCL_IN	Header_1 x2	—	861400021YO2LF	Amphenol ICC	CONN HEADER VERT 2POS 2.54MM
65	J1,J18,J29	3	Header 1x8	hdr_amp_87220_8_1x8_100	—	0022284081	Molex	CONN HEADER VERT 8POS 2.54MM
66	J2	1	Header 1x10	CONF1X10-254P_2612X240X850H_TH	DNL	10129378-910002BLF	Amphenol ICC (FCI)	CONN HEADER VERT 10POS 2.54MM
67	J3,J4	2	Header 1x8	CONF1X8-254P_2104X240X850H_TH	DNL	10129378-908002BLF	Amphenol ICC (FCI)	CONN HEADER VERT 8POS 2.54MM
68	J5	1	Header 1x6	CONF1X6-254P_1596X240X850H_TH	DNL	10129378-906002BLF	Amphenol ICC (FCI)	CONN HEADER VERT 6POS 2.54MM
69	J6	1	Receptacle 20X2	HDR254-2X20_socket	DNL	PPTC202LFBN-RC	Sullins Connector Solutions	CONN HDR 40POS 0.1 TIN PCB
70	J7	1	HEADER 5X2	HDR254-2X5_SHROUDED	DNL	30310-6002HB	3M	CONN HEADER VERT 10POS 2.54MM
71	J8,J9	2	HDR40	HDR-20x2	—	PRPC020DFBN-RC	Sullins Connector Solutions	CONN HEADER VERT 40POS 2.54MM
72	J10	1	SMA	bnc5-100-280t	DNL	5-1814832-1	TE Connectivity AMP Connectors	CONN SMA JACK STR 50 OHM PCB
73	J11,J19	2	USB_MINI_B	usb2-0-rec-240-0001-9	—	UX60-MB-5ST(60)	Hirose Electric Co Ltd	CONN RCPT USB2.0 MINI B SMD R/A
74	J12,J13	2	GND	TUR_TH	—	1573-2	Keystone Electronics	TERM TURRET SINGLE L=4.72MM TIN
75	J14	1	RJMG212S21130ER	RJMG212S2XX30XR	—	RJMG212S21130ER	Amphenol ICC	2 Port RJ45Board Edge, Through Hole 10/100/1000 Base-T, AutoMDIX

Item	Reference	Qty	Value	PCB Footprint	Assembly Option	Manufacturer Part Number	Manufacturer	Description
76	J15	1	PMOD 2x6	PPPC062LJBN-RC	—	PPPC062LJBN-RC	Sullins Connector Solutions	CONN HDR 12POS 0.1 GOLD PCB R/A
77	J17	1	PJ-051A	PJ_051A	—	PJ-051A	Same Sky	CONN PWR JACK 2X5.5MM SOLDER
78	J20	1	VS5	HDR1X3	—	PRPC003SAAN-RC	Sullins Connector Solutions	CONN HEADER VERT 3POS 2.54MM
79	J21	1	VS6	HDR1X3	—	PRPC003SAAN-RC	Sullins Connector Solutions	CONN HEADER VERT 3POS 2.54MM
80	J22	1	VS7	HDR1X3	—	PRPC003SAAN-RC	Sullins Connector Solutions	CONN HEADER VERT 3POS 2.54MM
81	J23	1	VS4	HDR1X3	—	PRPC003SAAN-RC	Sullins Connector Solutions	CONN HEADER VERT 3POS 2.54MM
82	J24	1	VS1_2	HDR1X3	—	PRPC003SAAN-RC	Sullins Connector Solutions	CONN HEADER VERT 3POS 2.54MM
83	J25	1	X4_CTL	HDR1X3	—	PRPC003SAAN-RC	Sullins Connector Solutions	CONN HEADER VERT 3POS 2.54MM
84	J26	1	REG0	HDR1X3	—	PRPC003SAAN-RC	Sullins Connector Solutions	CONN HEADER VERT 3POS 2.54MM
85	J28	1	REG1	HDR1X3	—	PRPC003SAAN-RC	Sullins Connector Solutions	CONN HEADER VERT 3POS 2.54MM
86	J30	1	68000-206HLF	CONN_106HLFF_AMP	—	68000-206HLF	Amphenol ICC (FCI)	CONN HEADER VERT 6POS 2.54MM
87	L1,L2,L3,L4,L5,L6,L7,L8,L12, L13,L14,L15,L16,L17,L18,L19, L20,L22,L23,L24	20	600ohm 500mA	fb0603	—	BLM18AG601SN1D	Murata Electronics	FERRITE BEAD 600 OHM 0603 1LN
88	L9	1	1.5uH SPM6530T-1R5M-HZ	SPM6530T-2R2M	Alternate PN : SPM6530T-1R5M100	SPM6530T-1R5M-HZ	TDK Corporation	FIXED IND 1.5UH 11.6A 10.67 MOHM
89	L10	1	3.3uH SPM6530T-3R3M	SPM6530T-2R2M	Alternate PN : SPM6530T-3R3M-HZ	SPM6530T-3R3M	TDK Corporation	FIXED IND 3.3UH 6.8A 29.7MOHM SM

Item	Reference	Qty	Value	PCB Footprint	Assembly Option	Manufacturer Part Number	Manufacturer	Description
90	L11,L21	2	1.0uH	SRP3020TA	—	SRP3020TA-1R0M	Bourns Inc.	FIXED IND 1UH 4A 38 MOHM SMD
91	MH1,MH2,MH3,MH4	4	ThruHole	MTG125	DNL	—	—	Mounting Hole
92	POT1	1	3314G-1-103E	sot23-3314G-1	—	3314G-1-103E	Bourns Inc.	TRIMMER 10K OHM 0.25W GW TOP ADJ
93	Q1,Q5	2	MMBT3904	MMBT3904	—	MMBT3904-7-F	Diodes Incorporated	TRANS NPN 40V 0.2A SOT-23-3
94	R1,R2,R3,R46,R47,R48,R105, R106,R111,R141,R142,R143, R145,R148,R149,R248,R263, R264,R265	19	4.7k	R0402	—	RT0402FRE074K7L	YAGEO	RES SMD 4.7K OHM 1% 1/16W 0402
95	R4,R5,R6,R7,R14,R15,R16,R17, R18,R20,R21,R22,R24,R25,R90, R91,R93,R95,R98,R136,R140, R168,R169,R190,R191,R192, R196,R197,R203,R204,R207, R208,R209,R210	34	0	R0603	—	RC0603JR-070RL	YAGEO	RES 0 OHM JUMPER 1/10W 0603
96	R8,R9,R97,R157,R266	5	2.2K	R0402	—	RC0402FR-072K2L	YAGEO	RES 2.2K OHM 1% 1/16W 0402
97	R10,R19,R81,R83	4	12K	R0603	—	RC0603FR-0712KL	YAGEO	RES 12K OHM 1% 1/10W 0603
98	R11,R12,R13,R29,R52,R73,R74, R121,R122,R123,R126,R240, R243	13	10K	R0402	—	RT0402FRE0710KL	YAGEO	RES SMD 10K OHM 1% 1/16W 0402
99	R26,R27,R33,R34	4	2.2K	R0402	—	ERJ-2RKF2201X	Panasonic Electronic Components	RES SMD 2.2K OHM 1% 1/10W 0402
100	R28,R69,R164	3	100K	R0402	—	AC0402FR-7W100KL	YAGEO	RES 100 KOHM 1% 1/8W 0402
101	R30,R146,R147,R159	4	0	R0603	DNL	RC0603JR-070RL	YAGEO	RES 0 OHM JUMPER 1/10W 0603
102	R31	1	0	R0603	—	RC0603JR-070RL	YAGEO	RES 0 OHM JUMPER 1/10W 0603
103	R35,R37,R43,R44,R45,R59,R60, R78,R79,R130	10	0	R0603	DNL	RC0603JR-070RL	YAGEO	RES 0 OHM JUMPER 1/10W 0603
104	R39,R40,R41,R42,R55,R56,R57, R58,R260,R261,R262	11	4.7k	R0402	—	RT0402FRE074K7L	YAGEO	RES SMD 4.7K OHM 1% 1/16W 0402
105	R53,R107,R108	3	23.7K-DNI	R0603	DNL	CRCW060323K7FKEA	Vishay Dale	RES SMD 23.7K OHM 1% 1/10W 0603
106	R54,R109,R110,R241,R242, R244,R245,R249,R250	9	0	R0402	—	ERJ-2GE0R00X	Panasonic Electronic Components	RES SMD 0 OHM JUMPER 1/10W 0402

Item	Reference	Qty	Value	PCB Footprint	Assembly Option	Manufacturer Part Number	Manufacturer	Description
107	R61,R62,R63,R64,R131,R132, R133,R134,R137,R153	10	1	R0603	—	CRCW06031R00JN EAHP	Vishay Dale	RES SMD 1 OHM 5% 1/3W 0603
108	R70,R71,R144,R162,R163	5	0	R0402	—	ERJ-2GE0R00X	Panasonic Electronic Components	RES SMD 0 OHM JUMPER 1/10W 0402
109	R72	1	0	R0402	—	ERJ-2GE0R00X	Panasonic Electronic Components	RES SMD 0 OHM JUMPER 1/10W 0402
110	R80,R82,R113,R114,R115, R116,R117,R118,R119,R120, R125,R135,R156,R171,R172, R173,R174,R175,R176,R177, R184,R185,R193,R194,R199, R200,R202,R206,R214,R215, R216,R217,R218,R219,R226	35	1K	R0402	—	RC0402FR-071KL	YAGEO	RES 1K OHM 1% 1/16W 0402
111	R84,R85,R86,R87,R88,R92,R94, R96	8	0	R0603	DNL	RC0603JR-070RL	YAGEO	RES 0 OHM JUMPER 1/10W 0603
112	R99	1	124k	R0603	—	RT0603DRD07124 KL	YAGEO	RES SMD 124K OHM 0.5% 1/10W 0603
113	R100,R103,R152,R198	4	22k	R0402	—	AC0402FR-0722KL	YAGEO	RES SMD 22K OHM 1% 1/16W 0402
114	R101,R104,R155	3	4.7k	R0402	—	RT0402FRE074K7L	YAGEO	RES SMD 4.7K OHM 1% 1/16W 0402
115	R102	1	7.5k	R0603	—	RT0603DRD077K5 L	YAGEO	RES SMD 7.5K OHM 0.5% 1/10W 0603
116	R112	1	0.01 ohm	R0603	—	WSL0603R0100FE A	Vishay Dale	RES 0.01 OHM 1% 1/10W 0603
117	R127	1	976R-0402SMT	R0402	—	RT0402BRD07976 RL	YAGEO	RES SMD 976 OHM 0.1% 1/16W 0402
118	R128	1	1.15K-0402SMT	R0402	—	RT0402BRD071K1 5L	YAGEO	RES SMD 1.15KOHM 0.1% 1/16W 0402
119	R138	1	240E	R0402	—	RC0402FR-07240RL	YAGEO	RES 240 OHM 1% 1/16W 0402
120	R139	1	10K	R0402	—	ERJ-2GEJ103X	Panasonic Electronic Components	RES SMD 10K OHM 5% 1/10W 0402
121	R151,R201,R227,R228,R229, R230,R231,R232,R233,R234	10	200	R0603	—	ERJ-3EKF2000V	Panasonic Electronic Components	RES SMD 200 OHM 1% 1/10W 0603
122	R158,R205	2	1M Ohm	R0402	—	AC0402FR-071ML	YAGEO	RES SMD 1M OHM 1% 1/16W 0402

Item	Reference	Qty	Value	PCB Footprint	Assembly Option	Manufacturer Part Number	Manufacturer	Description
123	R160,R161,R235	3	0	R0603	—	RC0603JR-070RL	YAGEO	RES 0 OHM JUMPER 1/10W 0603
124	R165,R186	2	4.7k	R0402	—	RT0402FRE074K7L	YAGEO	RES SMD 4.7K OHM 1% 1/16W 0402
125	R166,R170,R178,R179,R180, R181,R182,R183,R187,R188, R189,R211,R212,R213,R220, R221,R222,R223,R224,R225	20	1K	R0402	DNL	RC0402FR-071KL	YAGEO	RES 1K OHM 1% 1/16W 0402
126	R167,R195,R246,R251	4	100	R0402	DNL	AC0402FR-07100RL	YAGEO	RES SMD 100 OHM 1% 1/16W 0402
127	R238,R239	2	49.9E	R0402	—	RC0402FR-0749R9L	YAGEO	RES 49.9 OHM 1% 1/16W 0402
128	R252	1	150	R0201	—	RC0201FR-07150RL	YAGEO	RES 150 OHM 1% 1/20W 0201
129	R253,R254,R255,R256,R257, R258,R259	7	49.9E	R0201	DNL	RC0201DR-0749R9L	YAGEO	RES 49.9 OHM 0.5% 1/20W 0201
130	SMA1,SMA2,SMA3,SMA0	4	27G_SMA-DNI	SV_SF2921-61345-2S	DNL	SF2921-61345-2S	Amphenol SV Microwave	CONN SMA JACK STR 50 OHM SMD
131	SMA4,SMA5	2	27G_SMA-DNI	SV_SF2921-61356-2S	DNL	SF2921-61356-2S	Amphenol SV Microwave	CONN SMA JACK STR 50 OHM SMD
132	SW1	1	SW DIP-8	DIP_254-8	—	DS04-254-1L-08BK	CUI device	DIP SWITCH, SPST, 2.54 PITCH, RA
133	SW2	1	PB1	sw_sp_st_eswitch_tl1015	—	TL1015AF160QG	E-Switch	SWITCH TACTILE SPST-NO 0.05A 12V
134	SW3	1	PB2	sw_sp_st_eswitch_tl1015	—	TL1015AF160QG	E-Switch	SWITCH TACTILE SPST-NO 0.05A 12V
135	SW4	1	PB3	sw_sp_st_eswitch_tl1015	—	TL1015AF160QG	E-Switch	SWITCH TACTILE SPST-NO 0.05A 12V
136	SW5	1	PB4	sw_sp_st_eswitch_tl1015	—	TL1015AF160QG	E-Switch	SWITCH TACTILE SPST-NO 0.05A 12V
137	SW6	1	1101M2S2CQE2	SWITCH_3P-6A	Alternate PN : 1101M2S3CQE2	1101M2S2CQE2	C&K	Slide Switches
138	SW7	1	418117270903	WS-DITV_418117270903	—	418117270903	Wurth Elektronik	SWITCH SLIDE DIP SPST 0.025A 24V

Item	Reference	Qty	Value	PCB Footprint	Assembly Option	Manufacturer Part Number	Manufacturer	Description
139	TP3,TP4,TP7,TP8,TP9,TP10, TP11,TP12,TP14,TP15,TP16, TP17,TP18,TP19,TP20,TP21, TP22,TP23,TP24,TP25,TP26	21	TP_S_40_63	TP	DNL	—	—	Square test point, 40mil inner diameter, 63mil outer diameter
140	TP5,TP6	2	TP_S_40_63	TP	DNL	—	—	—
141	U1,U18	2	FT2232HL	tqfp64_0p5_12p2x12p2_h1p6	CUSTOMER SUPPLIED	FT2232HL	FTDI	IC USB HS DUAL UART/FIFO 64-LQFP
142	U2,U19	2	93LC56C-I/SN	so8_50_244	—	93LC56C-I/SN	Microchip Technology	IC EEPROM 2KBIT MICROWIRE 8SOIC
143	U3	1	LFMXO5-55TD-BBG400	BGA400-080-17X17-SOCKET	CUSTOMER SUPPLIED	LFMXO5-55TD-BBG400	Lattice	—
144	U6,U7	2	GPY115C0VI	56VQFN_GPY115	—	GPY115C0VI	MaxLinear, Inc.	TRANSVR IC GPY115C0VI VQFN56 SLN
145	U8	1	NCV1117ST33T3G	sot223_4p	—	NCP1117ST33T3G	onsemi	IC REG LINEAR 3.3V 1A SOT223
146	U9	1	lpddr4-fbga200-x32	TFBGA200	—	MT53E1G16D1ZW-046 AAT:C	Micron	IC DRAM 16GBIT PAR 200TFBGA
147	U10	1	FUSE	0154005DRT	—	0154005.DRT	Littelfuse	FUSE BRD MNT 5A 125VAC/VDC 2SMD
148	U11,U12	2	BD9D321EFJ	HTSOP_8_BD9D321	—	BD9D321EFJ-E2	Rohm Semiconductor	IC REG BUCK ADJ 3A 8HTSOP-J
149	U13	1	NCV1117ST25T3G	sot223_4p	—	NCV1117ST25T3G	onsemi	IC REG LINEAR 2.5V 1A SOT223-4
150	U14	1	SN74AVC4T774	tssop16-0p65mm	Alternate PN : 74AVC4T774PWJ	SN74AVC4T774PWR	Texas Instruments	IC TRANSLATOR BIDIR 16TSSOP
151	U15	1	RP115H181D/SOT89-5	SOT89-5	—	RP115H181D-T1-FE	Nisshinbo Micro Devices Inc.	IC REG LINEAR 1.8V 1A SOT89-5
152	U16	1	RP111H121D-T1-FE/SOT89-5	SOT89-5	Alternate PN : RP115H121D-T1-FE	RP111H121D-T1-FE	Nisshinbo Micro Devices Inc.	IC REG LINEAR 1.2V 500MA SOT89-5
153	U17	1	RP111H111D/SOT89-5	SOT89-5	—	RP111H111D-T1-FE	Nisshinbo Micro Devices Inc.	IC REG LINEAR 1.1V 500MA SOT89-5
154	X1,X2	2	7M-12.000MAAJ	xtal_4p_7m	—	7M-12.000MAAJ-T	TXC CORPORATION	CRYSTAL 12.0000MHZ 18PF SMD
155	X3,X6	2	ABM3-25	XTAL_ABM3	—	ABM7-25.000MHZ-D2Y-T	Abracon LLC	CRYSTAL 25.0000MHZ 18PF SMD

Item	Reference	Qty	Value	PCB Footprint	Assembly Option	Manufacturer Part Number	Manufacturer	Description
156	X4	1	27MHZ	x4-2520	—	ASEMB-27.000MHZ-XY-T	Abracon LLC	MEMS OSC XO 27.0000MHZ CMOS SMD
157	X7	1	100MHz	3225-6PIN	—	AK3ADDF1-100.000T3	Abracon LLC	XTAL OSC XO 100MHZ LVDS SMD
158	X8	1	100MHz	3225-6PIN	—	AX3HAF1-100.0000	Abracon LLC	XTAL OSC XO 100MHZ 3.3V HCSL
159	X9	1	125.0000MHz	3225-6PIN	—	AX3DAF1-125.0000	Abracon LLC	XTAL OSC XO 125MHZ 3.3V LVDS
160	LFMXO5-55TD-EVN_REV-A PCB	1	—	—	—	305-PD-25-0130	Pactron	—

Appendix C. User Defined Preference File

```
// These names follow the MachXO5-55TD/Q Evaluation Board schematic but,
// they may be defined by the user. Thus, they can be copied into the
// preference file and edited to match a different naming convention if
// needed or used to fill in the Spreadsheet view.

// LFMXO5-55TD/Q LED Connections
// Note: The following order matches the LED locations on the board
// from top D1 to bottom D8
ldc_set_location -site {G11} [get_ports {LED[0]}]
ldc_set_location -site {G15} [get_ports {LED[1]}]
ldc_set_location -site {G12} [get_ports {LED[2]}]
ldc_set_location -site {H12} [get_ports {LED[3]}]
ldc_set_location -site {L14} [get_ports {LED[4]}]
ldc_set_location -site {L15} [get_ports {LED[5]}]
ldc_set_location -site {M20} [get_ports {LED[6]}]
ldc_set_location -site {M19} [get_ports {LED[7]}]

//DIP Switch Connections
ldc_set_location -site {V2} [get_ports {DIPSW[0]}]
ldc_set_location -site {V3} [get_ports {DIPSW[1]}]
ldc_set_location -site {W2} [get_ports {DIPSW[2]}]
ldc_set_location -site {W3} [get_ports {DIPSW[3]}]
ldc_set_location -site {U4} [get_ports {DIPSW[4]}]
ldc_set_location -site {V4} [get_ports {DIPSW[5]}]
ldc_set_location -site {T4} [get_ports {DIPSW[6]}]
ldc_set_location -site {V5} [get_ports {DIPSW[7]}]


//Push Button Connections
ldc_set_location -site {K6} [get_ports PB1]

//add JP4 to enable PB2 control
ldc_set_location -site {B7}  [get_ports PB3]

//ldc_set_sysconfig {PROGRAMN_PORT=DISABLE}
//ldc_set_location -site {G10} [get_ports PB4]

//Clock inputs

ldc_set_location -site {C2} [get_ports clk_x4]
ldc_set_port -iobuf {IO_TYPE=LVCMOS33} [get_ports clk_x4]

ldc_set_location -site {U19} [get_ports clk_x8]
ldc_set_port -iobuf {IO_TYPE= LVSTLD_I} [get_ports clk_x8]

ldc_set_location -site {R3} [get_ports clk_x9]
ldc_set_port -iobuf {IO_TYPE=LVDS} [get_ports clk_x9]

//SLVS
ldc_set_location -site {W13} [get_ports {slvs_data[0]}]
ldc_set_location -site {V11} [get_ports {slvs_data[1]}]
ldc_set_location -site {Y12} [get_ports {slvs_data[2]}]
ldc_set_location -site {W9} [get_ports {slvs_data[3]}]
ldc_set_location -site {V12} [get_ports {slvs_data[4]}]
```

```
ldc_set_location -site {P13} [get_ports {slvs_data[5]}]
ldc_set_location -site {Y10} [get_ports {slvs_data[6]}]
ldc_set_location -site {Y8} [get_ports {slvs_data[7]}]
ldc_set_location -site {Y6} [get_ports {slvs_data[8]}]
ldc_set_location -site {U7} [get_ports {slvs_data[9]}]
ldc_set_location -site {T7} [get_ports {slvs_data[10]}]
ldc_set_location -site {R8} [get_ports {slvs_data[11]}]
ldc_set_location -site {U13} [get_ports {slvs_data[12]}]
ldc_set_location -site {R13} [get_ports {slvs_data[13]}]
ldc_set_location -site {P12} [get_ports {slvs_data[14]}]
ldc_set_location -site {U10} [get_ports {slvs_data[15]}]
ldc_set_location -site {U9} [get_ports {slvs_data[16]}]
ldc_set_location -site {R9} [get_ports {slvs_data[17]}]
ldc_set_location -site {W7} [get_ports {slvs_data[18]}]
ldc_set_location -site {N9} [get_ports {slvs_data[19]}]
ldc_set_location -site {N7} [get_ports {slvs_data[20]}]
ldc_set_location -site {M12} [get_ports {slvs_data[21]}]
ldc_set_location -site {R11} [get_ports {slvs_data[22]}]
ldc_set_location -site {P10} [get_ports {slvs_data[23]}]
ldc_set_location -site {Y2} [get_ports {slvs_data[24]}]
ldc_set_location -site {V1} [get_ports {slvs_data[25]}]
ldc_set_location -site {W4} [get_ports {slvs_data[26]}]
ldc_set_location -site {W5} [get_ports {slvs_data[27]}]

//LPDDR4

# DQS GROUP 0
ldc_set_location -site {N18} [get_ports {ddr_dq_io[0]}]
ldc_set_location -site {N20} [get_ports {ddr_dq_io[1]}]
ldc_set_location -site {P18} [get_ports {ddr_dq_io[2]}]
ldc_set_location -site {P17} [get_ports {ddr_dq_io[3]}]
ldc_set_location -site {P16} [get_ports {ddr_dq_io[4]}]
ldc_set_location -site {N19} [get_ports {ddr_dq_io[5]}]
ldc_set_location -site {M17} [get_ports {ddr_dq_io[6]}]
ldc_set_location -site {M16} [get_ports {ddr_dq_io[7]}]
ldc_set_location -site {P19} [get_ports {ddr_dqs_io[0]}]
ldc_set_location -site {N17} [get_ports {ddr_dmi_io[0]}]
# DQS GROUP 1
ldc_set_location -site {R15} [get_ports {ddr_dq_io[8]}]
ldc_set_location -site {T14} [get_ports {ddr_dq_io[9]}]
ldc_set_location -site {R14} [get_ports {ddr_dq_io[10]}]
ldc_set_location -site {T15} [get_ports {ddr_dq_io[11]}]
ldc_set_location -site {V14} [get_ports {ddr_dq_io[12]}]
ldc_set_location -site {W14} [get_ports {ddr_dq_io[13]}]
ldc_set_location -site {V15} [get_ports {ddr_dq_io[14]}]
ldc_set_location -site {U14} [get_ports {ddr_dq_io[15]}]
ldc_set_location -site {Y15} [get_ports {ddr_dqs_io[1]}]
ldc_set_location -site {U15} [get_ports {ddr_dmi_io[1]}]

ldc_set_port -iobuf {IO_TYPE=LVSTL_I TERMINATION=40} [get_ports {ddr_dmi_io[*]}]
ldc_set_port -iobuf {IO_TYPE=LVSTL_I TERMINATION=40} [get_ports {ddr_dq_io[*]}]
ldc_set_port -iobuf {IO_TYPE=LVSTLD_I TERMINATION=40} [get_ports {ddr_dqs_io[*]}]

# CK, CKE, CS, CA
ldc_set_location -site {R19} [get_ports {ddr_ck_o[0]}]
ldc_set_location -site {W20} [get_ports {ddr_cke_o[0]}]
```

```
ldc_set_location -site {W18} [get_ports {ddr_cs_o[0]}]
ldc_set_location -site {W19} [get_ports {ddr_ca_o[0]}]
ldc_set_location -site {V18} [get_ports {ddr_ca_o[1]}]
ldc_set_location -site {T19} [get_ports {ddr_ca_o[2]}]
ldc_set_location -site {V19} [get_ports {ddr_ca_o[3]}]
ldc_set_location -site {V20} [get_ports {ddr_ca_o[4]}]
ldc_set_location -site {T20} [get_ports {ddr_ca_o[5]}]
ldc_set_location -site {R16} [get_ports ddr_odt_ca_o]
ldc_set_location -site {N16} [get_ports ddr_reset_n_o]

ldc_set_port -iobuf {IO_TYPE=LVSTLD_I} [get_ports {ddr_ck_o[0]}]
ldc_set_port -iobuf {IO_TYPE=LVSTL_I} [get_ports {ddr_cke_o[0]}]
ldc_set_port -iobuf {IO_TYPE=LVSTL_I} [get_ports {ddr_cs_o[0]}]
ldc_set_port -iobuf {IO_TYPE=LVSTL_I} [get_ports {ddr_ca_o[*]}]
ldc_set_port -iobuf {IO_TYPE=LVSTL_I} [get_ports ddr_odt_ca_o]
ldc_set_port -iobuf {IO_TYPE=LVSTL_I} [get_ports ddr_reset_n_o]

//PMOD0 Connections
ldc_set_location -site {K20} [get_ports PMOD0_1]
ldc_set_location -site {L16} [get_ports PMOD0_2]
ldc_set_location -site {L18} [get_ports PMOD0_3]
ldc_set_location -site {L19} [get_ports PMOD0_4]
ldc_set_location -site {K19} [get_ports PMOD0_5]
ldc_set_location -site {L17} [get_ports PMOD0_6]
ldc_set_location -site {L20} [get_ports PMOD0_7]
ldc_set_location -site {M18} [get_ports PMOD0_8]


//USER JTAG Connections
ldc_set_location -site {F13} [get_ports UTDI]
ldc_set_location -site {F12} [get_ports UTDO]
ldc_set_location -site {G13} [get_ports UTMS]
ldc_set_location -site {G14} [get_ports UTCK]


//USER RS232 Connections
ldc_set_location -site {C15} [get_ports RS232_Rx_TTL]
ldc_set_location -site {D15} [get_ports RS232_Tx_TTL]
ldc_set_location -site {B15} [get_ports RTSn]
ldc_set_location -site {A15} [get_ports CTSn]
ldc_set_location -site {E13} [get_ports DTRn]
ldc_set_location -site {E12} [get_ports DSRn]
ldc_set_location -site {D14} [get_ports DCDn]
ldc_set_location -site {E15} [get_ports RI]

//RASPBERRY PI Connections
ldc_set_location -site {E8} [get_ports RASP_IO02]
ldc_set_location -site {F6} [get_ports RASP_IO03]
ldc_set_location -site {G9} [get_ports RASP_IO04]
ldc_set_location -site {G1} [get_ports RASP_IO05]
ldc_set_location -site {G2} [get_ports RASP_IO06]
ldc_set_location -site {G3} [get_ports RASP_IO07]
ldc_set_location -site {F1} [get_ports RASP_IO08]
ldc_set_location -site {E2} [get_ports RASP_IO09]
ldc_set_location -site {F7} [get_ports RASP_IO10]
ldc_set_location -site {F2} [get_ports RASP_IO11]
```

```
ldc_set_location -site {F5} [get_ports RASP_IO12]
ldc_set_location -site {G6} [get_ports RASP_IO13]
ldc_set_location -site {G8} [get_ports RASP_IO14]
ldc_set_location -site {F8} [get_ports RASP_IO15]
ldc_set_location -site {H5} [get_ports RASP_IO16]
ldc_set_location -site {E7} [get_ports RASP_IO17]
ldc_set_location -site {G7} [get_ports RASP_IO18]
ldc_set_location -site {H4} [get_ports RASP_IO19]
ldc_set_location -site {H7} [get_ports RASP_IO20]
ldc_set_location -site {H8} [get_ports RASP_IO21]
ldc_set_location -site {E5} [get_ports RASP_IO22]
ldc_set_location -site {E4} [get_ports RASP_IO23]
ldc_set_location -site {E3} [get_ports RASP_IO24]
ldc_set_location -site {F3} [get_ports RASP_IO25]
ldc_set_location -site {H6} [get_ports RASP_IO26]
ldc_set_location -site {E6} [get_ports RASP_IO27]
ldc_set_location -site {E1} [get_ports RASP_ID_SC]
ldc_set_location -site {D1} [get_ports RASP_ID_SD]

//VERSA HEADER Connections
ldc_set_location -site {H15} [get_ports EXPCON_IO0]
ldc_set_location -site {H13} [get_ports EXPCON_IO1]
ldc_set_location -site {F15} [get_ports EXPCON_IO2]
ldc_set_location -site {H16} [get_ports EXPCON_IO3]
ldc_set_location -site {D16} [get_ports EXPCON_IO4]
ldc_set_location -site {F16} [get_ports EXPCON_IO5]
ldc_set_location -site {C17} [get_ports EXPCON_IO6]
ldc_set_location -site {A16} [get_ports EXPCON_IO7]
ldc_set_location -site {B18} [get_ports EXPCON_IO8]
ldc_set_location -site {B17} [get_ports EXPCON_IO9]
ldc_set_location -site {F17} [get_ports EXPCON_IO10]
ldc_set_location -site {E17} [get_ports EXPCON_IO11]
ldc_set_location -site {E18} [get_ports EXPCON_IO12]
ldc_set_location -site {B20} [get_ports EXPCON_IO13]
ldc_set_location -site {F18} [get_ports EXPCON_IO14]
ldc_set_location -site {G16} [get_ports EXPCON_IO15]
ldc_set_location -site {G17} [get_ports EXPCON_IO16]
ldc_set_location -site {C19} [get_ports EXPCON_IO17]
ldc_set_location -site {C20} [get_ports EXPCON_IO18]
ldc_set_location -site {D20} [get_ports EXPCON_IO19]
ldc_set_location -site {D19} [get_ports EXPCON_IO20]
ldc_set_location -site {E19} [get_ports EXPCON_IO21]
ldc_set_location -site {F19} [get_ports EXPCON_IO22]
ldc_set_location -site {E20} [get_ports EXPCON_IO23]
ldc_set_location -site {F20} [get_ports EXPCON_IO24]
ldc_set_location -site {G20} [get_ports EXPCON_IO25]
ldc_set_location -site {G19} [get_ports EXPCON_IO26]
ldc_set_location -site {H17} [get_ports EXPCON_IO27]
ldc_set_location -site {H18} [get_ports EXPCON_IO28]
ldc_set_location -site {J10} [get_ports EXPCON_IO29]
ldc_set_location -site {J11} [get_ports EXPCON_IO30]
ldc_set_location -site {K10} [get_ports EXPCON_IO31]
ldc_set_location -site {J17} [get_ports EXPCON_IO32]
ldc_set_location -site {J12} [get_ports EXPCON_IO33]
ldc_set_location -site {H20} [get_ports EXPCON_IO34]
ldc_set_location -site {H19} [get_ports EXPCON_IO35]
```

```
ldc_set_location -site {K11} [get_ports EXPCON_IO36]
ldc_set_location -site {J19} [get_ports EXPCON_IO37]
ldc_set_location -site {J14} [get_ports EXPCON_IO38]
ldc_set_location -site {J13} [get_ports EXPCON_IO39]
ldc_set_location -site {K16} [get_ports EXPCON_IO40]
ldc_set_location -site {J15} [get_ports EXPCON_IO41]
ldc_set_location -site {K14} [get_ports EXPCON_IO42]
ldc_set_location -site {K15} [get_ports EXPCON_IO43]
ldc_set_location -site {K12} [get_ports EXPCON_IO44]
ldc_set_location -site {K13} [get_ports EXPCON_IO45]
ldc_set_location -site {J16} [get_ports EXPCON_OSC]
ldc_set_location -site {J18} [get_ports EXPCON_CLKIN]
ldc_set_location -site {J20} [get_ports EXPCON_CLKOUT]
ldc_set_location -site {H14} [get_ports HPE_RESOUT#]
ldc_set_location -site {G18} [get_ports HPE_CARDSEL#]

//Aardvark Header Connections
ldc_set_location -site {M7} [get_ports AK_SCL]
ldc_set_location -site {M8} [get_ports AK_SDA]
ldc_set_location -site {N1} [get_ports AK_MISO]
ldc_set_location -site {N2} [get_ports AK_SCLK]
ldc_set_location -site {N3} [get_ports AK_SS]
ldc_set_location -site {N4} [get_ports AK_MOSI]


//Arduino Header Connections
ldc_set_location -site {K4} [get_ports AR_IO0]
ldc_set_location -site {K5} [get_ports AR_IO1]
ldc_set_location -site {J6} [get_ports AR_IO2]
ldc_set_location -site {K7} [get_ports AR_IO3]
ldc_set_location -site {J7} [get_ports AR_IO4]
ldc_set_location -site {J8} [get_ports AR_IO5]
ldc_set_location -site {H9} [get_ports AR_IO6]
ldc_set_location -site {K8} [get_ports AR_IO7]
ldc_set_location -site {K3} [get_ports AR_IO8]
ldc_set_location -site {K2} [get_ports AR_IO9]
ldc_set_location -site {K1} [get_ports AR_SS_IO10]
ldc_set_location -site {L3} [get_ports AR_MOSI_IO11]
ldc_set_location -site {L1} [get_ports AR_MISO_IO12]
ldc_set_location -site {L2} [get_ports AR_SCK_IO13]
ldc_set_location -site {L7} [get_ports AR_IO14]
ldc_set_location -site {N5} [get_ports AR_SDA]
ldc_set_location -site {N6} [get_ports AR_SCL]
ldc_set_location -site {J9} [get_ports AR_RESET]
ldc_set_location -site {M1} [get_ports AR_AD0]
ldc_set_location -site {M2} [get_ports AR_AD1]
ldc_set_location -site {M3} [get_ports AR_AD2]
ldc_set_location -site {M4} [get_ports AR_AD3]
ldc_set_location -site {M5} [get_ports AR_AD4]
ldc_set_location -site {M6} [get_ports AR_AD5]
```

Appendix D. MachXO5-55TD Evaluation Board Errata

As shown in Appendix A. MachXO5-55TD Evaluation Board Schematics:

- Page 3 of the Schematics, USB to Hard JTAG I/F
  Pin 1 of J1 and Pin 15 of U14 are connected with VCCIO2. It is recommended to connect them with VCCIO1 to ensure JTAG pins are pulled up to VCCIO1.
- Page 7 of the Schematics, PCIE&FPC Headers (Bank 4)
  PCIE_CLKp and PCIE_CLKn assignments are mismatched with the U3 ball locations. It is recommended to swap them with the correct assignment. PCIE_CLKp should be connected to B7 of U3. PCIE_CLKn should be connected to C7 of U3.

References

For more information, refer to the following documents:

- MachXO5-NX Devices Web Page
- MachXO5-55TD Evaluation Board Web Page
- MachXO5-55TDQ Evaluation Board Web Page
- MachXO5-NX Programming and Configuration User Guide (FPGA-TN-02271)
- Programming Cable User Guide (FPGA-UG-02042)
- MachXO5-NX Family Root of Trust Devices Data Sheet (FPGA-DS-02120)
- ASC Bridge Board Evaluation Board User Guide (FPGA-EB-02025)
- MachXO5-NX Root-of-Trust Device Provisioning User Guide (FPGA-TN-02333)
- Lattice Propel Design Environment web page
- Lattice Radiant Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Revision History

Revision 0.80, October 2025

Section	Change Summary
All	Initial preliminary release.

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