# Tri-Speed Ethernet RGMII

# Reference Design

FPGA-RD-02328-1.0

October 2025

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# Acronyms and Abbreviations in This Document

A list of acronyms and abbreviations used in this document.

| Acronyms/Abbreviations | Definition |
|---|---|
| AHBL | AHB-Lite Bus |
| APB | Advanced eXtensible Interface |
| CAT6 | Category 6 Cable |
| DCS | Dynamic Clock Selection |
| GPIO | General Purpose Input/Output |
| I2C | Inter-Integrated Circuit |
| LED | Light Emitting Diode |
| MAC | Media Access Control |
| MDIO | Management Data Input/Output |
| PC | Personal Computer |
| PHY | Physical Layer Device |
| PLL | Phase-Locked Loop |
| RGMII | Reduced Gigabit Media Independent Interface |
| RX | Receiver |
| TSE | Triple-Speed Ethernet |
| TX | Transceiver |
| UART | Universal Asynchronous Receiver/Transmitter |
| USB | Universal Serial Bus |

# 1. Introduction

This reference design demonstrates a 1G/100M Ethernet application using Lattice Triple-Speed Ethernet (TSE) IP Core in RGMII mode to interoperate with an on-board Ethernet PHY. The sample Ethernet packets are generated through RISC-V MC soft processor and transmitted to an on-board Ethernet PHY via the RGMII interface. The transmitted Ethernet packets are captured on a Personal Computer (PC) host and analyzed or observed using Wireshark software. This reference design also supports loopback mode to receive the transmitted Ethernet packets through RGMII RX interface back to RISC-V MC soft processor for data comparison.

## 1.1. Quick Facts

Download the reference design files from the Lattice reference design web page.

**Table 1.1. Summary of the Reference Design**

| | | |
|---|---|---|
| **General** | Target Devices | MachXO5™-NX (LFMXO5-65T) |
| | Source code format | Verilog |
| **Simulation** | Functional simulation | — |
| | Timing simulation | — |
| | Testbench | — |
| | Testbench format | — |
| **Software Requirements** | Software tool and version | • Lattice Radiant™ software version 2025.1<br>• Lattice Propel™ software version 2025.1 |
| | IP version (if applicable) | • RISC-V MC v2.8.0<br>• System Memory v2.4.0<br>• GPIO v1.6.2<br>• UART v1.3.0<br>• AHBL Interconnect v1.4.0<br>• AHBL-to-APB Bridge v1.2.0<br>• APB Interconnect v1.3.0<br>• APB feedthrough v1.2.0<br>• PLL v1.9.1<br>• TSE MAC IP v2.1.0 |
| **Hardware Requirements** | Board | MachXO5-65T Development Board |
| | Cable | • USB cable for programming<br>• CAT6 ethernet cable |

## 1.2. Features

Key features of the TSE RGMII reference design include the following:

- Interoperates with an on-board Ethernet PHY using RGMII interface
- Supports operation speeds of 1 Gbps and 100 Mbps
- Generates and compares Ethernet packets using the RISC-V MC soft processor
- Configures the on-board Ethernet PHY using the RISC-V MC soft processor through the Management Data Input/Output (MDIO) interface
- AHBL to AXI-Streaming data conversion block to support packets transaction between TSE IP and RISC-V MC

## 1.3. Naming Conventions

### 1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

### 1.3.2. Signal Names

- *_n* are active low (asserted when value is logic 0)
- *_i* are input signals
- *_o* are output signals

# 2. Directory Structure and Files

The figure below shows the directory structure of the reference design.

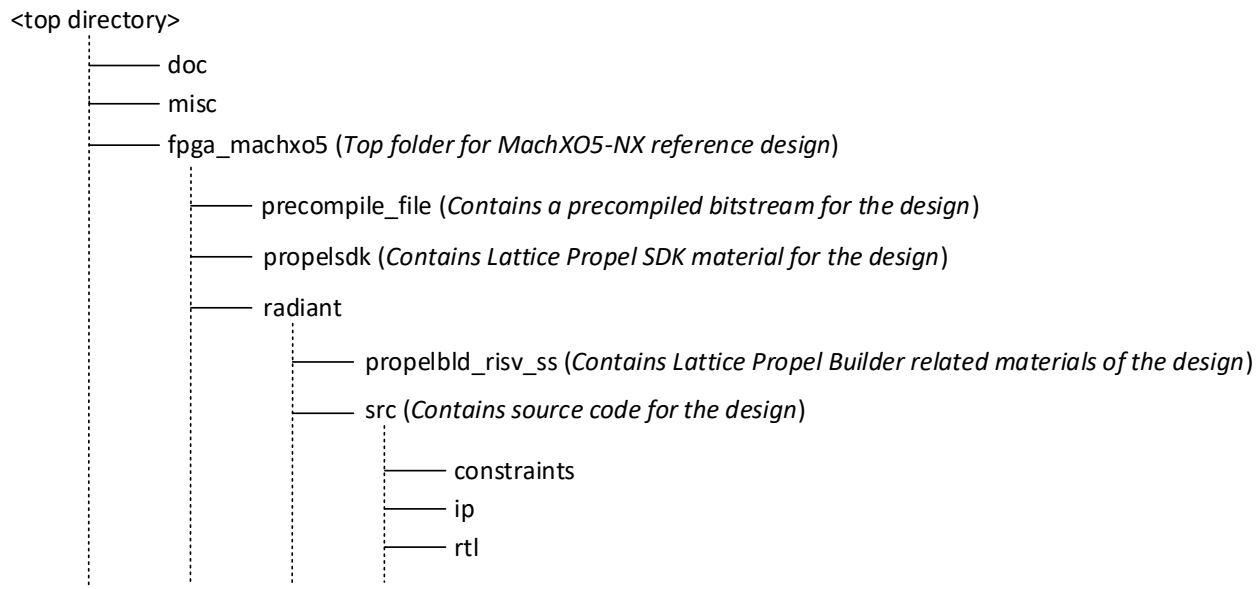


**Figure 2.1. Directory Structure**

The table below lists the important files included in the reference design package.

**Table 2.1. File List**

| Attribute | Description |
|---|---|
| fpga_machxo5/propelsdk/riscv_mc_rmgii/.cproject | Project file for the Lattice Propel SDK used in this reference design. |
| fpga_machxo5/radiant/propelbld_riscv_ss/riscv_ss.sbx | Project file for the Lattice Propel Builder used in this reference design |
| fpga_machxo5/radiant/riscv_rgmii.rdf | Lattice Radiant project file for this reference design |
| fpga_machxo5/precompiled_file/tse_rgmii.bit | Precompiled bitstream for this reference design |

# 3. Functional Description

Figure below shows the block diagram of TSE RGMII reference design. As shown in Figure 3.1, Ethernet packet generation is managed by RISC-V firmware. The Ethernet packets are transmitted to the Ethernet PHY through the AXI-Streaming and RGMII interfaces.

In loopback mode, the transmitted Ethernet packets are looped back within the Ethernet PHY and sent to the RISC-V firmware for data comparison. Register access transactions use the APB and MDIO interfaces.

This reference design supports dynamically configuration of operation in 1 Gbps or 100 Mbps mode through UART.

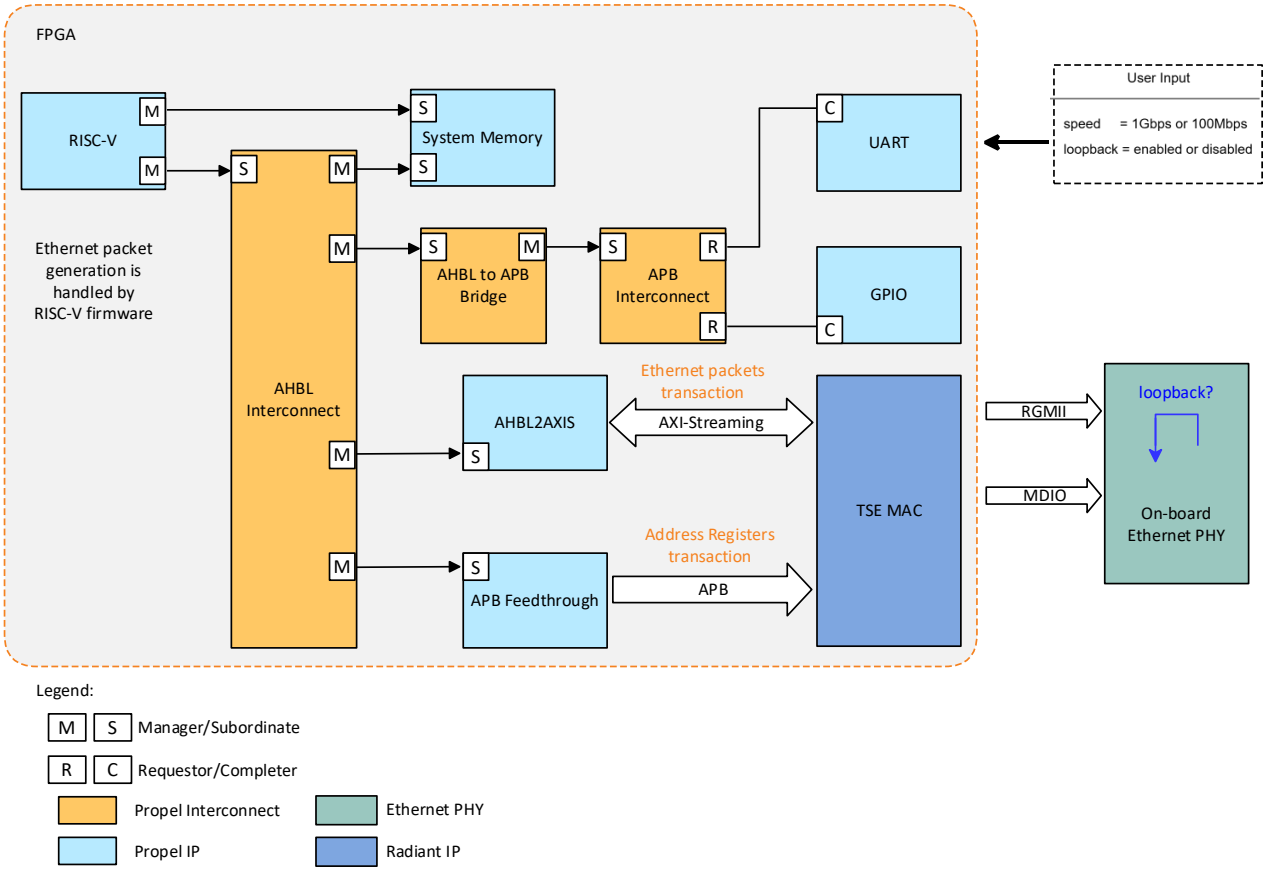


**Figure 3.1. Reference Design Block Diagram**

## 3.1. Design Components

The following list the components and IPs included in the reference design. For more information about the components and IPs, refer to the References section for its respective user guides and release notes.

- RISC-V MC CPU IP
- System Memory Module
- GPIO IP
- UART IP
- PLL Module
- AHB-Lite Interconnect Module
- AHB-Lite to APB Bridge Module
- APB Interconnect Module
- APB Feedthrough Module
- AHB-Lite to AXI-Streaming IP
- TSEMAC IP

### 3.1.1. RISCV MC CPU IP

The RISC-V MC CPU IP is configured with AHB-Lite Bus (AHBL) ports for instruction and data access.

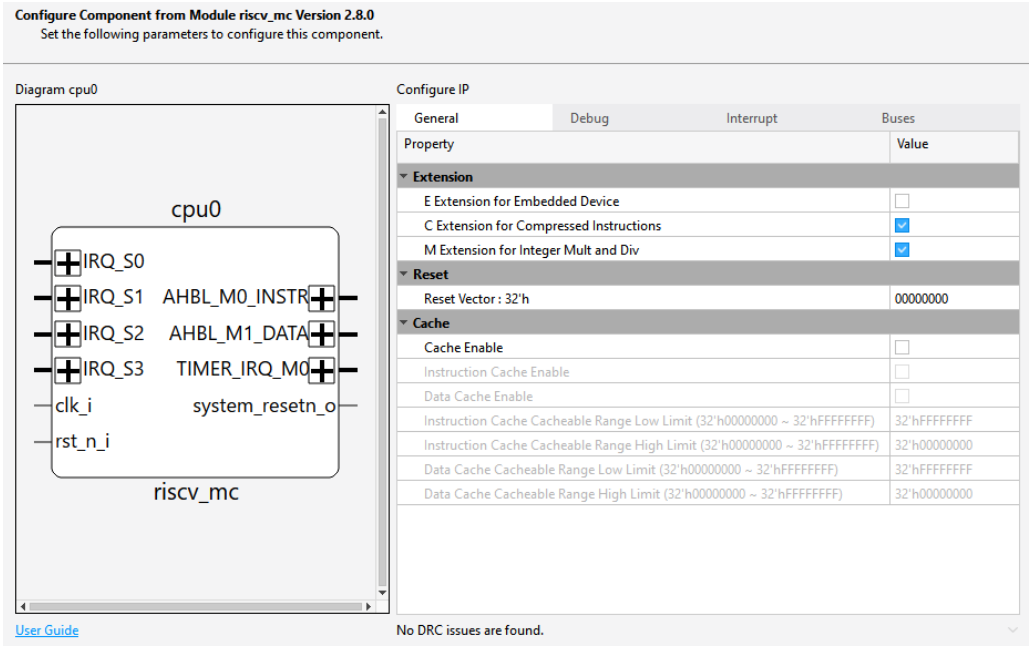


**Figure 3.2. RISC-V MC CPU IP**

The RISC-V software performs several functions in this reference design:

- Configures the Ethernet PHY registers using the MDIO interface
- Generates and compares Ethernet packets
- Dynamically configures the reference design for 1 Gbps or 100 Mbps mode, and for loopback or non-loopback mode, by reading user input from UART

**Note**: The source code for the RISC-V software is located at *<top>/propelsdk/riscv_mc_rgmii/src*. Refer to *main.c* for details on the RISC-V software flow.

### 3.1.2. System Memory Module

The System Memory Module is configured with dual AHBL ports. One port provides instruction memory access and connects directly to the RISC-V MC CPU IP; the other provides data memory access.

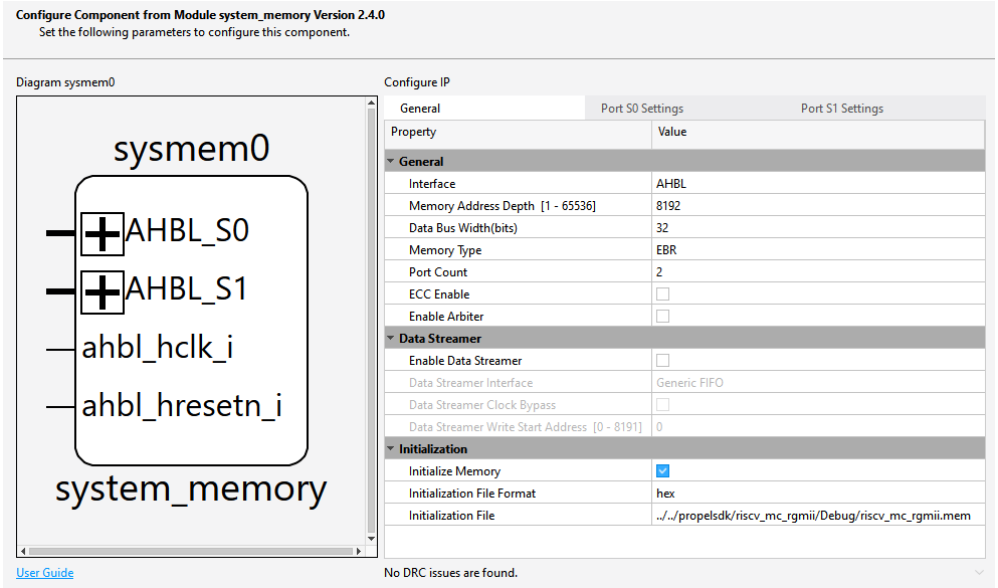


**Figure 3.3. System Memory Module**

### 3.1.3. GPIO IP

The GPIO IP is configured to drive the LED on the evaluation board. It is also used to control the speed mode of the reference design.

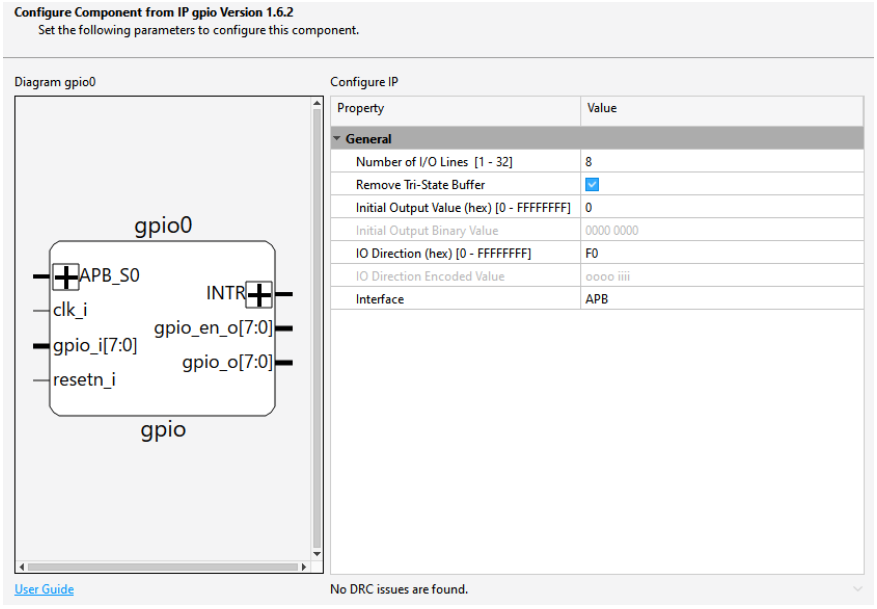


**Figure 3.4. GPIO IP**

### 3.1.4. UART IP

The UART IP is configured with a baud rate of 115200. The input clock is derived from the APB system clock frequency.

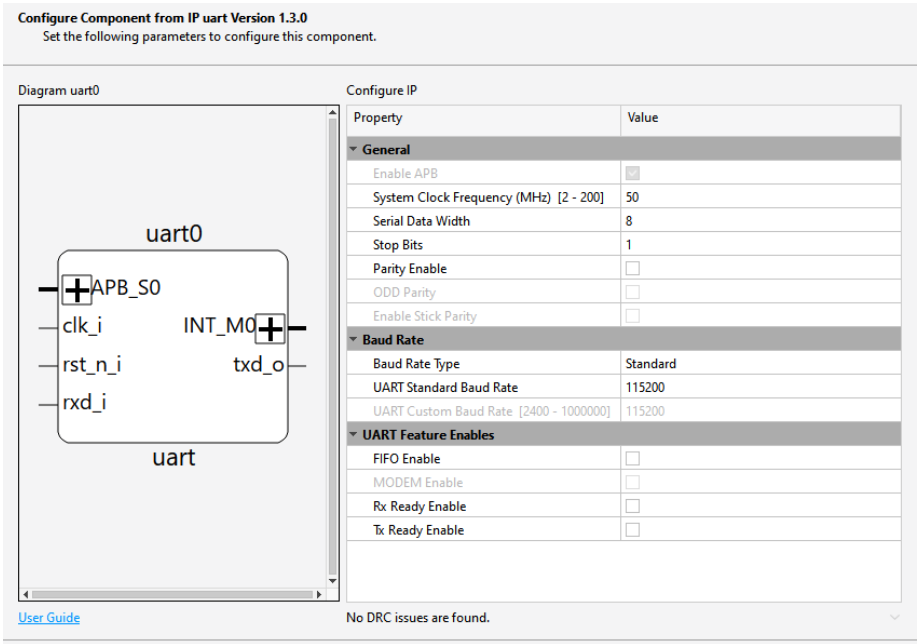


**Figure 3.5. UART IP**

### 3.1.5. APB Feedthrough IP

The APB feedthrough IP is connected to the TSEMAC IP's APB interface.

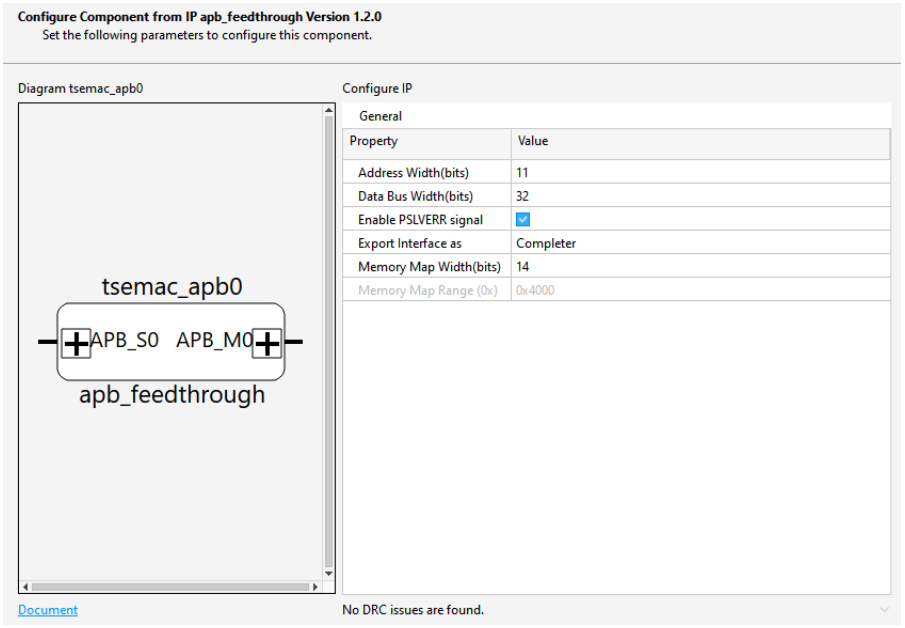


**Figure 3.6. APB feedthrough IP**

### 3.1.6. AHB-Lite to AXI-Streaming IP

This IP acts as a bridge to enable communication between the RISC-V CPU IP and the TSEMAC IP. It converts AHB-Lite data to AXI-S format and vice versa. This is a custom IP developed specifically for this reference design.

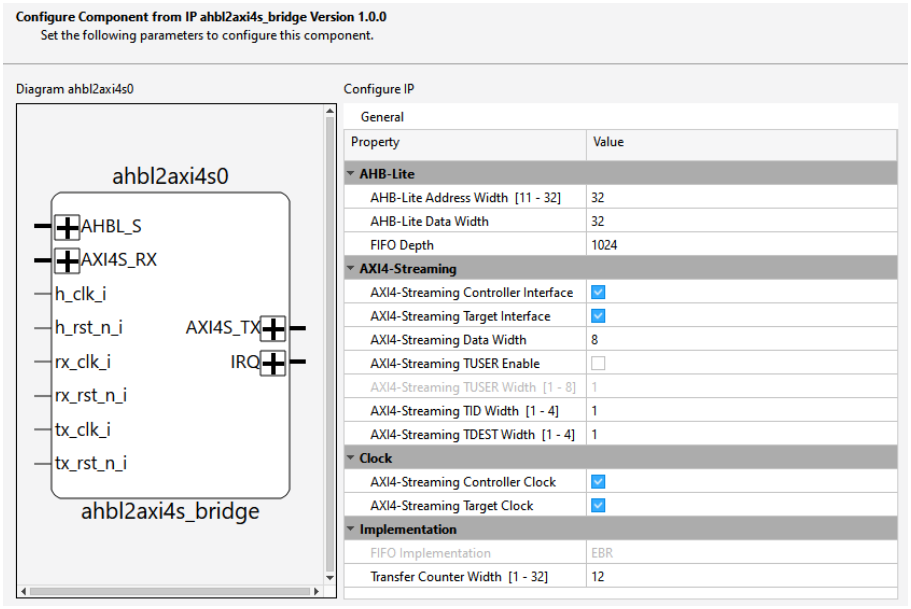


**Figure 3.7. AHB-Lite to AXI-Streaming IP**

### 3.1.7. PLL IP

The PLL module is configured to generate the following:

- MDIO clock
- RGMII TX clock for 1 Gbps mode
- RGMII TX clock for 100 Mbps mode
- RISC-V system clock

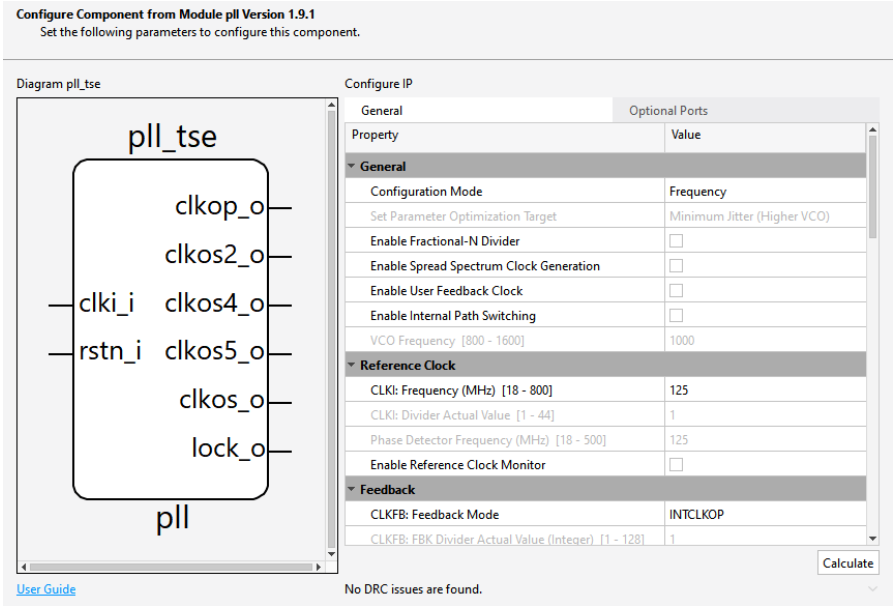


**Figure 3.8. PLL IP**

### 3.1.8. TSE MAC IP

The TSE IP is configured in RGMII mode. The RGMII TX and RX delays are not enabled in the TSE IP. The delays are applied on the Ethernet PHY.

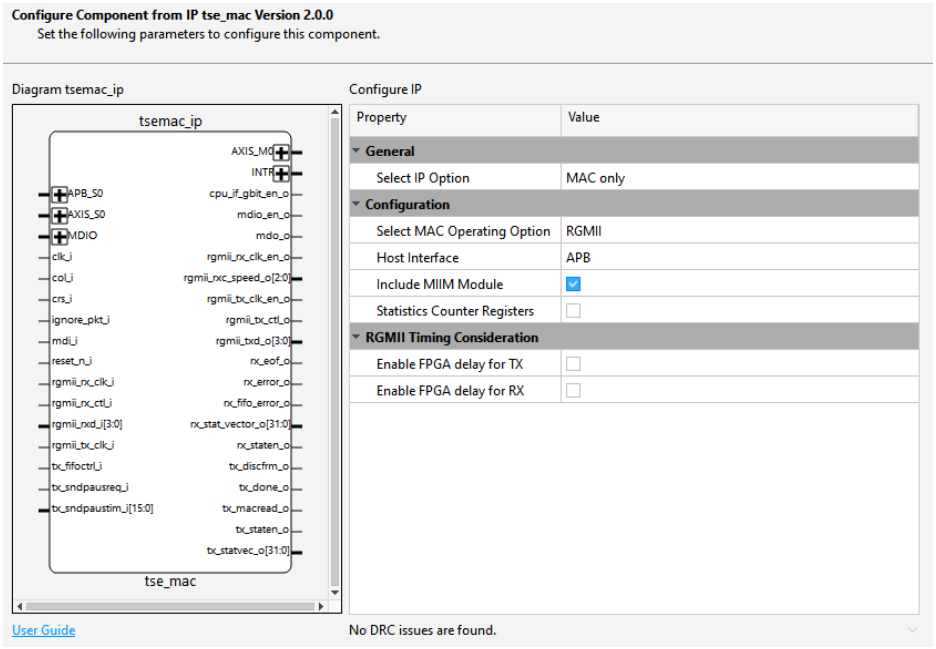


**Figure 3.9. TSE MAC IP**

## 3.2. Clocking Scheme

### 3.2.1. Clocking Overview

Figure below shows the clocking overview of the TSE RGMII reference design. The reference design receives an on-board 125 MHz source clock, which is supplied to the PLL as a reference clock. The PLL then uses this reference clock to generate various clocks for the reference design.

When configured to operate in 1 Gbps mode, the reference design uses RISC-V firmware to controls the Dynamic Clock Selection (DCS) primitive to use 125 MHz as *rgmii_tx_clk*. Similarly, in 100 Mbps mode, the RISC-V firmware uses 25 MHz as *rgmii_tx_clk* through the DCS primitive.

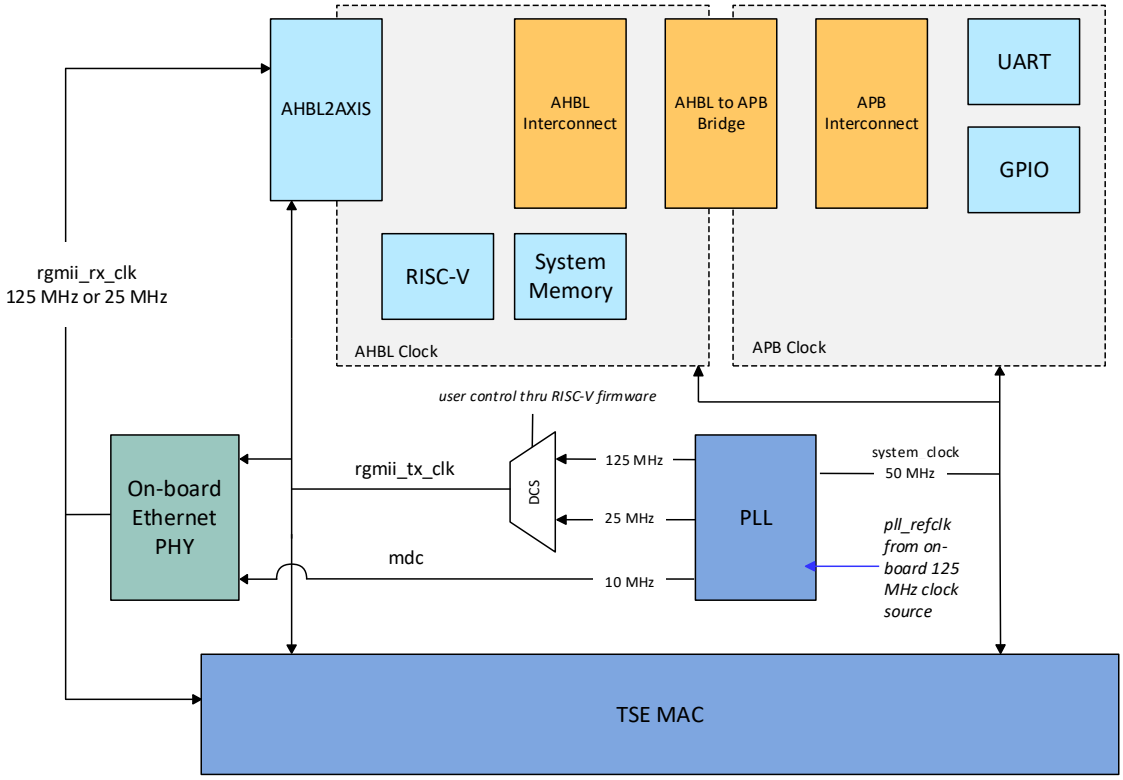


**Figure 3.10. Reference Design Clock Domain Block Diagram**

## 3.3. Reset Scheme

### 3.3.1. Reset Overview

Figure below shows the reset domain overview of the reference design. As shown in Figure 3.11, the main Reset Controller block generates the reset signals for the RISC-V components and the TSEMAC IP.

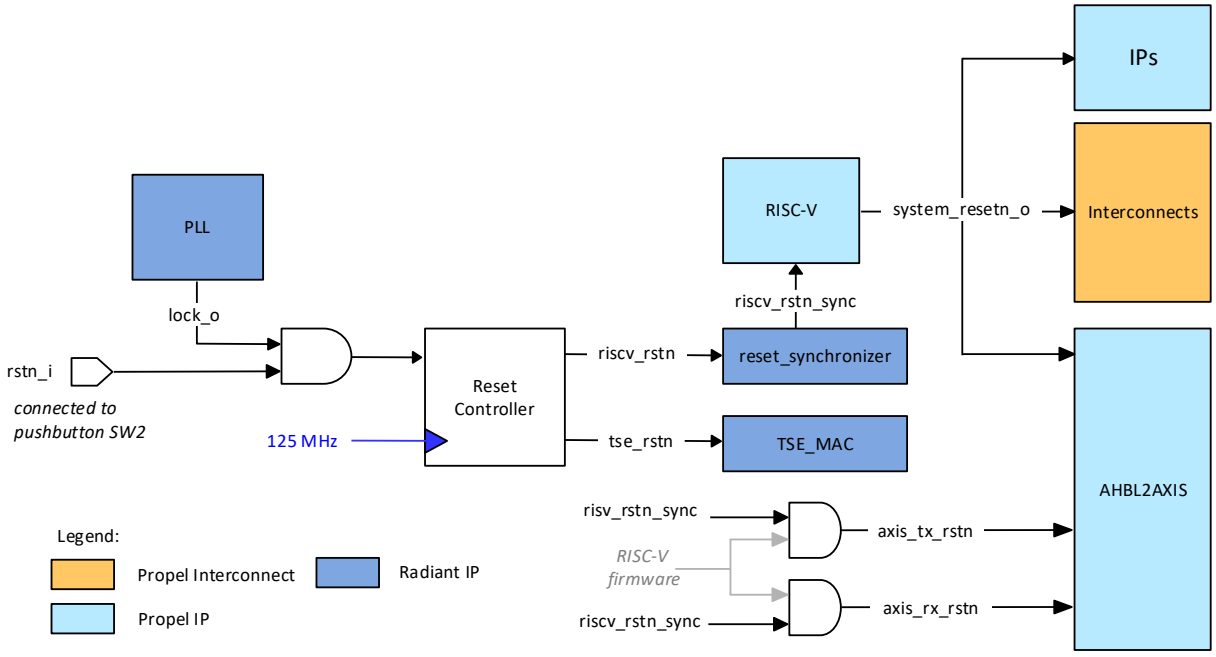


**Figure 3.11. Reference Design Reset Domain Block Diagram**

# 4. Signal Description

The input and output interface signals for the reference design are listed in Table 4.1.

**Table 4.1. Primary I/O for reference design**

| Port Name | I/O | Clock Domain | Description |
|---|---|---|---|
| clk_125_i | In | — | Reference clock for the PLL. The clock frequency is 125 MHz. |
| rst_n_i | In | async | Active-low asynchronous system reset. This signal is connected to pushbutton SW2. |
| uart_rxd_i | In | — | UART interface RX pin to on-board FTDI chip. |
| uart_txd_o | Out | — | UART interface TX pin to on-board FTDI chip |
| rgmii_rxc | In | — | RGMII RX clock from the Ethernet PHY. Frequency is 125 MHz for 1 Gbps mode and 25 MHz for 100 Mbps mode. |
| rgmii_rxctl | In | rgmii_rxc | RGMII RX control signal from Ethernet PHY. |
| rgmii_rxd[3:0] | In | rgmii_rxc | RGMII RX data from Ethernet PHY. |
| rgmii_txc | Out | — | RGMII TX clock output to Ethernet PHY. Frequency is 125 MHz for 1 Gbps mode and 25 MHz for 100 Mbps mode. |
| rgmii_txctl | Out | rgmii_txc | RGMII TX control output signal to Ethernet PHY. |
| rgmii_txd[3:0] | Out | rgmii_txc | RGMII TX output data to Ethernet PHY. |
| rgmii_mdc | Out | — | MDIO output clock to Ethernet PHY. Clock frequency is 10 MHz |
| rgmii_mdio | Inout | rgmii_mdc | MDIO data. Used to configure Ethernet PHY. |
| o_phy_resetn | Out | — | Active-low reset signal for Ethernet PHY. This signal is tied to HIGH. |
| led[7:0] | Out | — | LEDs indicator status for TSE RGMII reference design. |

| LED | Status Indicator |
|---|---|
| 0 | PLL lock |
| 1 | System output of reset |
| 2 | Operating Speed [0] |
| 3 | Operating Speed [1] |
| 4 | Tx link activity |
| 5 | Rx link activity |
| 6 | Packet Generation Done |
| 7 | Compare Packet Fail |

# 5. Running Reference Design

This section describes how to run the TSE RGMII reference design using Lattice Radiant software. For more information, refer to the Lattice Radiant Software User Guide.

## 5.1. Compiling Reference Design and Generate Bitstream File

This section describes the procedure of compiling the reference design and generating the FPGA bitstream file using Lattice Radiant Software.

**Note:** A precompiled bitstream is provided in the *<dir>/fpga_machxo5/precompiled_file* folder. This section may be skipped to directly run the reference design on the board.

1. Open Lattice Radiant software, as shown in Figure 5.1.

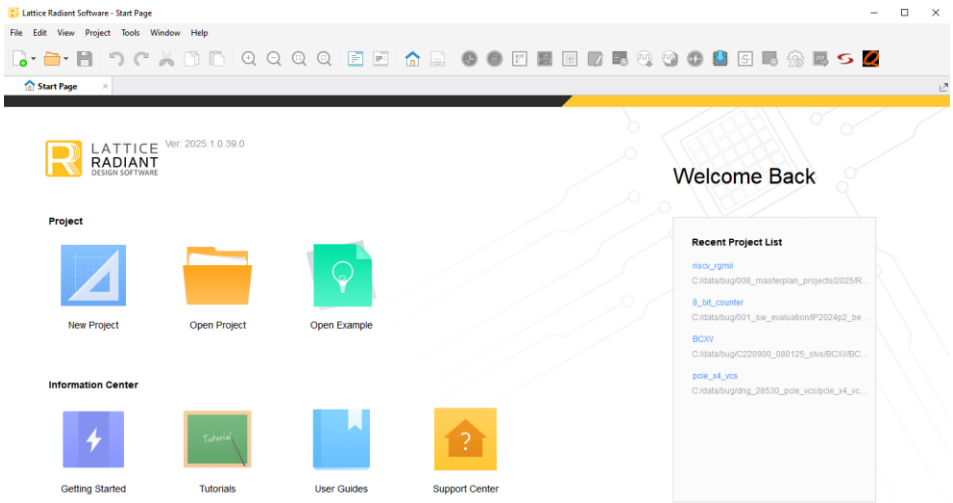


**Figure 5.1. Lattice Radiant Software**

2. Click **File > Open Project**, and open the Radiant project file (.rdf) from the *<dir>/fpga_machxo5/radiant* folder, as shown in Figure 5.2.

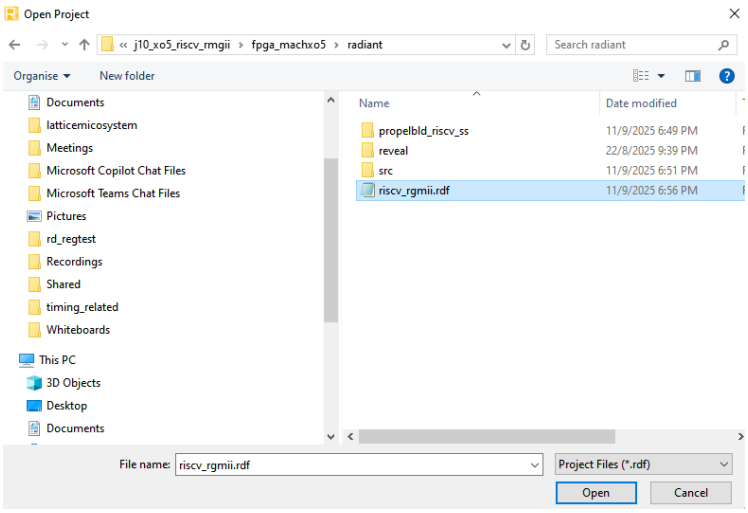


**Figure 5.2. Open Project File**

3. Click **Export Files**. Radiant will begin compiling the reference design from the synthesis stage and generate the bitstream file. View the log messages in the Export Reports folder to verify the generated bitstream..

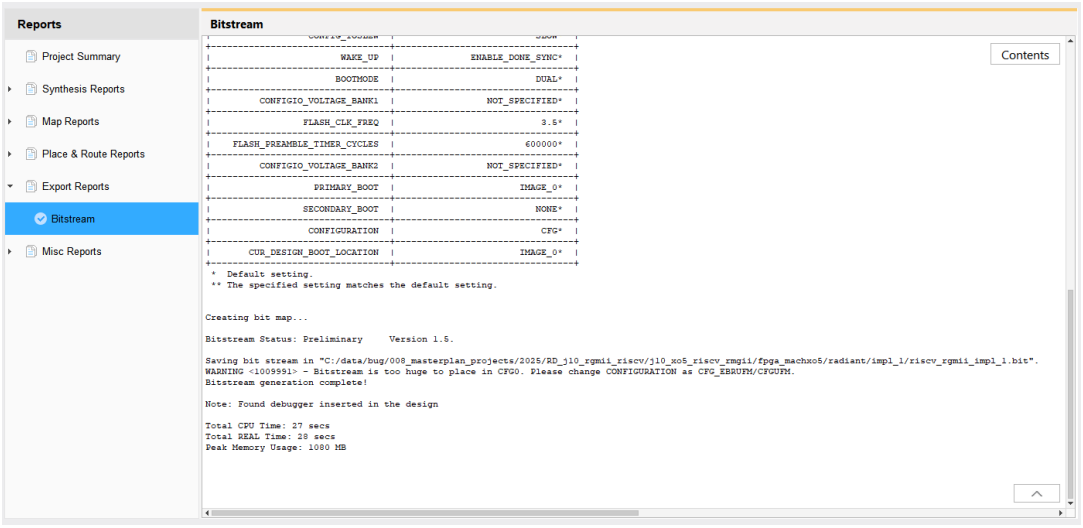


**Figure 5.3. Generated Bitstream Log**

# 6. Implementing Reference Design on Board

This section describes how to program and run the TSE RGMII reference design on the hardware board.

## 6.1. Requirements

The following lists the requirements for implementing the reference design on the board:

- Hardware
  - MachXO5-65T Evaluation Board
  - USB cable for programming
  - 12 V Power supply
  - CAT6 Ethernet cable
- Software
  - Lattice Radiant software version 2025.1
  - Lattice Propel software version 2025.1
  - Wireshark version 4.20 – Wireshark software download web page.

## 6.2. Hardware Testing on MachXO5-65T Development Board

Figure 6.1 shows the hardware setup for the TSE RGMII reference design. The MachXO5-65T Development Board includes an on-board Ethernet PHY (Texas Instruments, DP83867ERGZT). Therefore, no additional external Ethernet PHY is required for this hardware test.

**Note**: The on-board Ethernet PHY is configured to boot in RGMII mode on Revision B board. For older board revision, remove resistor R124 to force the Ethernet PHY to boot in RGMII mode.

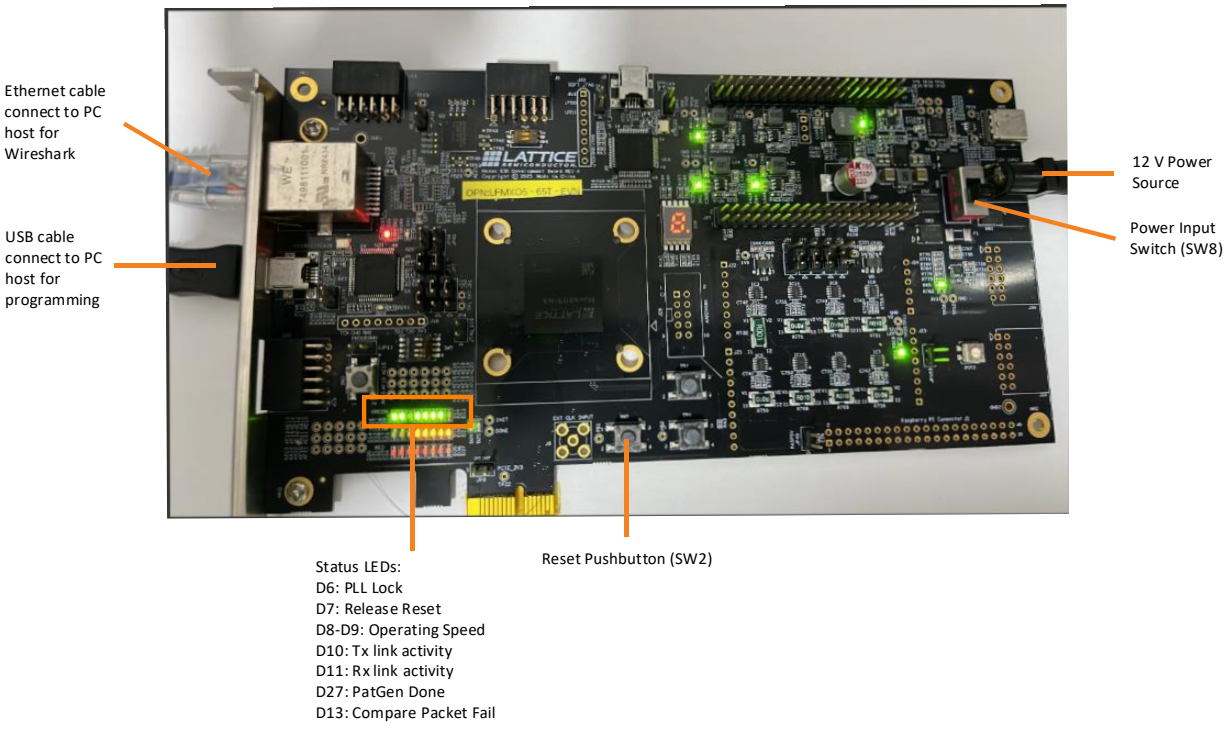


**Figure 6.1. Hardware Test Setup**

A UART terminal is required for this hardware test. This reference design uses Bus channel B of the on-board FTDI to operate as UART communication. By default, bus channel B is configured for I2C. Therefore, use a jumper to short pins 2 and 3 on both the J51 and J52 headers to enable UART communication. See Figure 6.2 for reference.

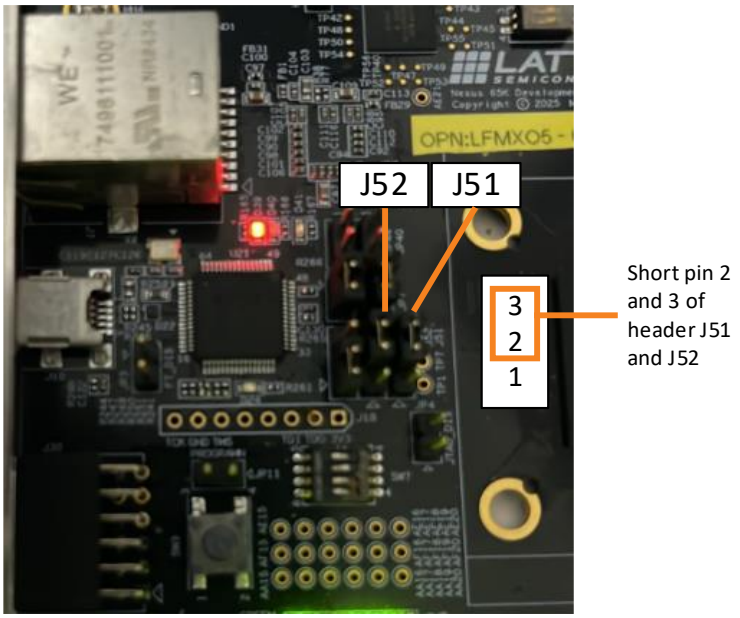


**Figure 6.2. Enable UART on MachXO5-65T board**

The table below explains the purpose and usage of LEDs and switches on board used in hardware testing.

**Table 6.1. LEDs and Switches on Board**

| Label | Type | Purpose/Description |
|---|---|---|
| SW2 | Push button | System reset. Press to reset entire design. |
| SW8 | Switch | Input Power Source Selection switch. |
| D6 | LED | Indicates PLL lock status. LED is ON when PLL is locked. |
| D7 | LED | Indicates reset status. LED is ON when the design is out of reset. |
| D8 | LED | Indicates operating speed.<br>• 1 Gbps mode : Both D9 and D8 LEDs are ON.<br>• 100 Mbps mode : D9 is ON; D8 is OFF. |
| D9 | LED | |
| D10 | LED | Blinks when packets are transmitting. |
| D11 | LED | Blinks when receiving packets. |
| D27 | LED | Indicates whether all sample Ethernet packets are generated. LED is ON when all packets are generated. |
| D13 | LED | Indicates packet mismatch when comparing receiving packet during loopback mode. LED is ON if any packet mismatch occurs. |

### 6.2.1. Capture Ethernet packet using Wireshark

To run this hardware test, set up the hardware as shown in Figure 6.1. Hardware Test Setup, then follow the steps below:

1. Power up the board and program the provided bitstream in the *precompiled_file* directory (*<top>/fpga_machxo5/precompiled_file/tse_rgmii.bit*).
2. **Open *Wireshark* software**, then apply filter ***ip.src==160.0.18.52*** to display only the sample Ethernet packets generated by RISC-V. Click the Click the **Start Capturing Packets** icon.

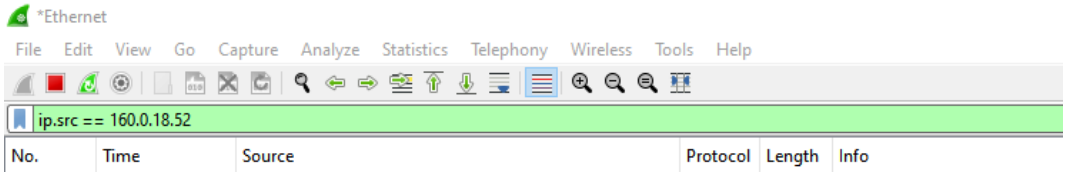


**Figure 6.3. Wireshark Packet Capture Setup**

3. Open serial terminal in Propel SDK and configure it as shown in the figure below. Use **Device Manager** to identify the COM port. Other serial terminals may also be used.
   **Note**: Ensure UART is enabled on the board. Short pins 2 and 3 of the J51 and J52 headers .

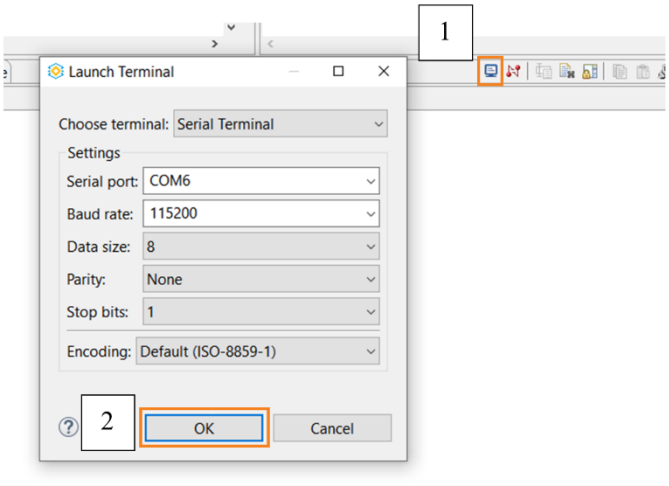


**Figure 6.4. Serial Terminal Configuration in Propel SDK**

4. **Press** and release **Pushbutton SW2**. This will restart the reference design.
5. At the serial terminal, the message ***Welcome to Tri-Speed Ethernet RGMII Reference Design*** should appears, as shown in the figure below.

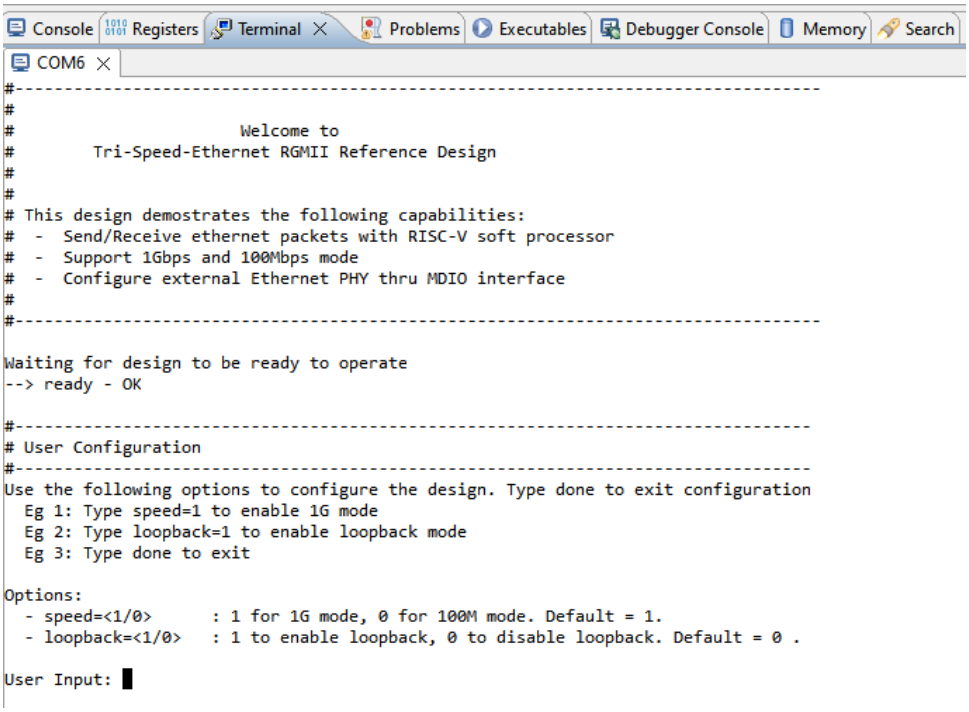


**Figure 6.5. Serial Terminal Welcome Message**

6. Follow the instructions in the serial terminal. By default, 1 Gbps mode is enabled, and loopback is disabled. To capture Ethernet packets on the PC host using Wireshark, loopback mode must remain disabled. For 1 Gbps mode, no configuration is needed. Type ***done*** to exit user configuration.

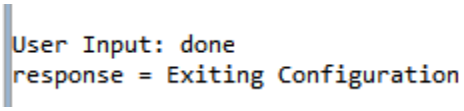


**Figure 6.6. Serial Terminal User Configuration Prompt**

7. The RISC-V software configures the Ethernet PHY and generate ten sample Ethernet packets.
8. Return to Wireshark application. Ten Ethernet packets captured, as shown in the figure below.

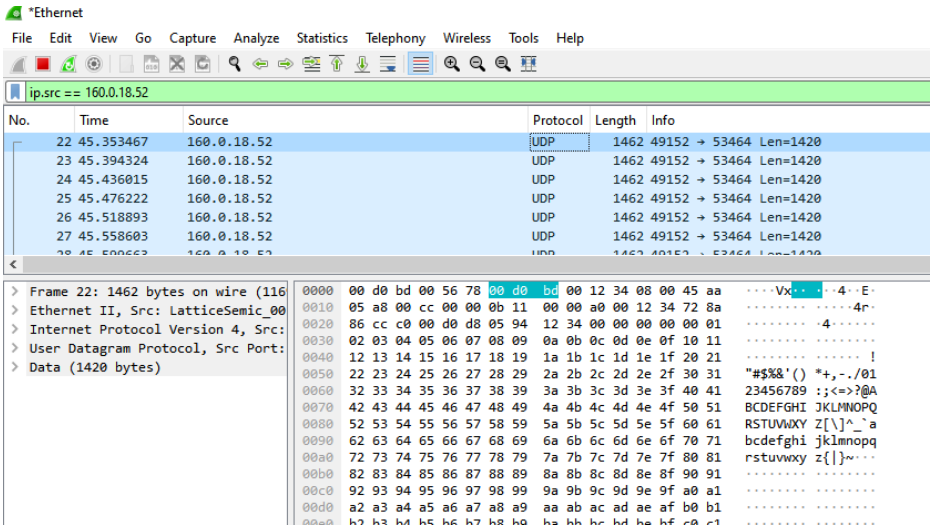


**Figure 6.7. Captured Ethernet Packets in Wireshark**

9. At the serial terminal, the message ***Flow – End*** appears, as shown in the figure below. Note that the data comparison test is skipped because loopback is disabled.

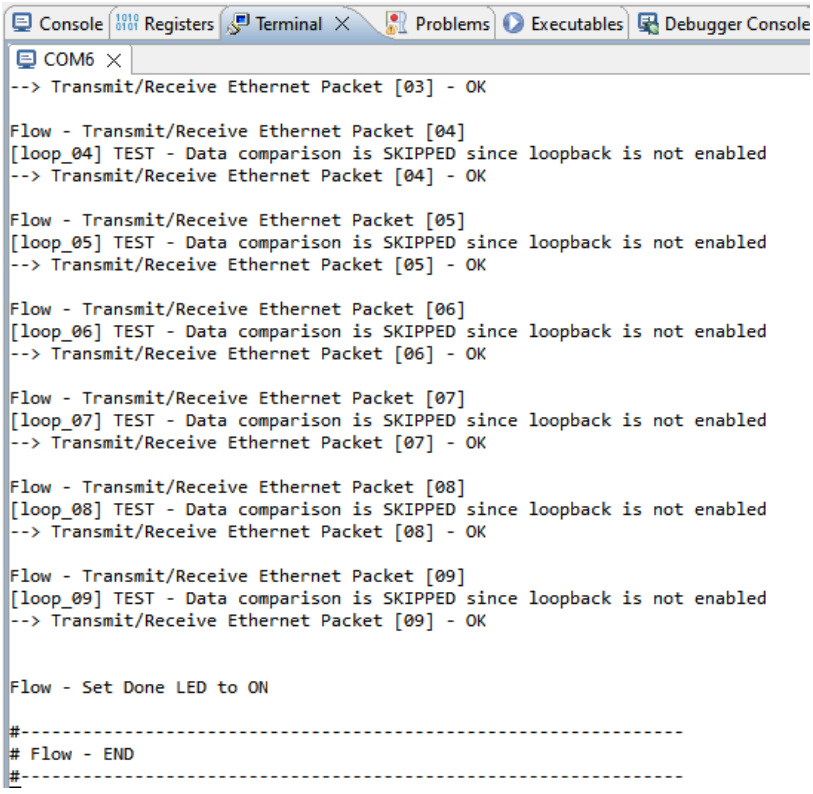


**Figure 6.8. Serial Terminal Flow Completion Message**

10. On the board, the Done LED (D27) lights up.
11. To test 100 Mbps mode, repeat from step 4. At step 6, type speed=0 to enable 100 Mbps mode, then follow the remaining steps as usual.

### 6.2.2. Loopback Test

To run the hardware loopback test, set up the hardware as shown in Figure 6.1. The Texas Instruments (TI) Ethernet PHY is configured to operate in digital loopback mode. Therefore, no modification to the hardware setup is required.

To begin the test, follow the steps below:

1. Power up the board and program the provided bitstream located in the *precompiled_file* directory (*<top>/fpga_machxo5/precompiled_file/tse_rgmii.bit*).
2. Open the serial terminal in Propel SDK and configure it as shown in the figure below. Use **Device Manager** to identify the COM port. Other serial terminals may also be used.
   **Note**: Ensure UART is enabled on the board. Short pins 2 and 3 of the J51 and J52 headers.

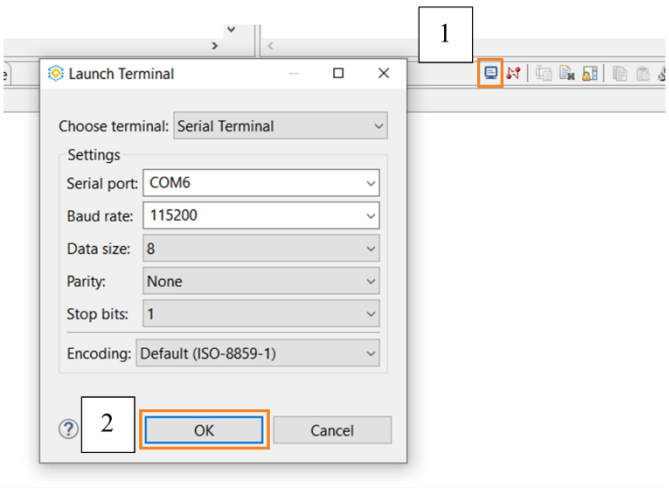


**Figure 6.9. Loopback Test - Serial Terminal Configuration in Propel SDK**

3. **Press** and release **Pushbutton SW2**. This will restart the reference design .
4. At the serial terminal, the message ***Welcome to Tri-Speed Ethernet RGMII Reference Design*** appears, as shown in the figure below.

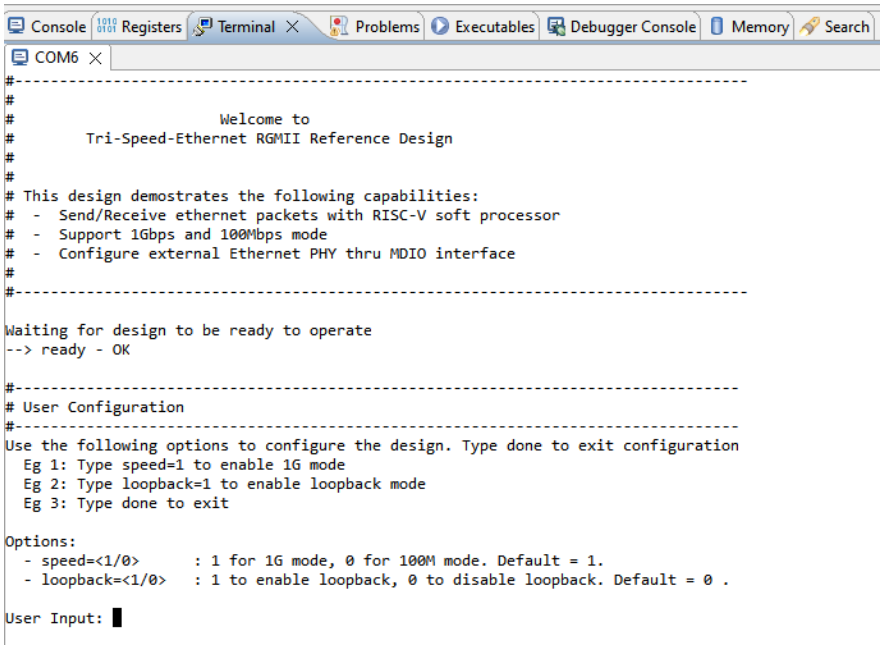


**Figure 6.10. Loopback Test - Serial Terminal Welcome Message**

5. Follow the instructions in the serial terminal. By default, 1 Gbps mode is enabled, and loopback is disabled. Type ***loopback=1*** to enable for loopback mode. Type ***done*** to exit user configuration. This test uses 1 Gbps mode.

```
User Input: loopback=1
response = enable loopback
User Input: done
response = Exiting Configuration
```

**Figure 6.11. Loopback Test - Serial Terminal User Configuration Prompt**

6. The RISC-V software configures the Ethernet PHY and generate ten sample Ethernet packets. In loopback mode, the transmitted packets are received for comparison testing.
7. When the flow completes, the message ***Flow – End*** appears in the serial terminal, as shown in the figure below. All ten of the Ethernet packets received should match.

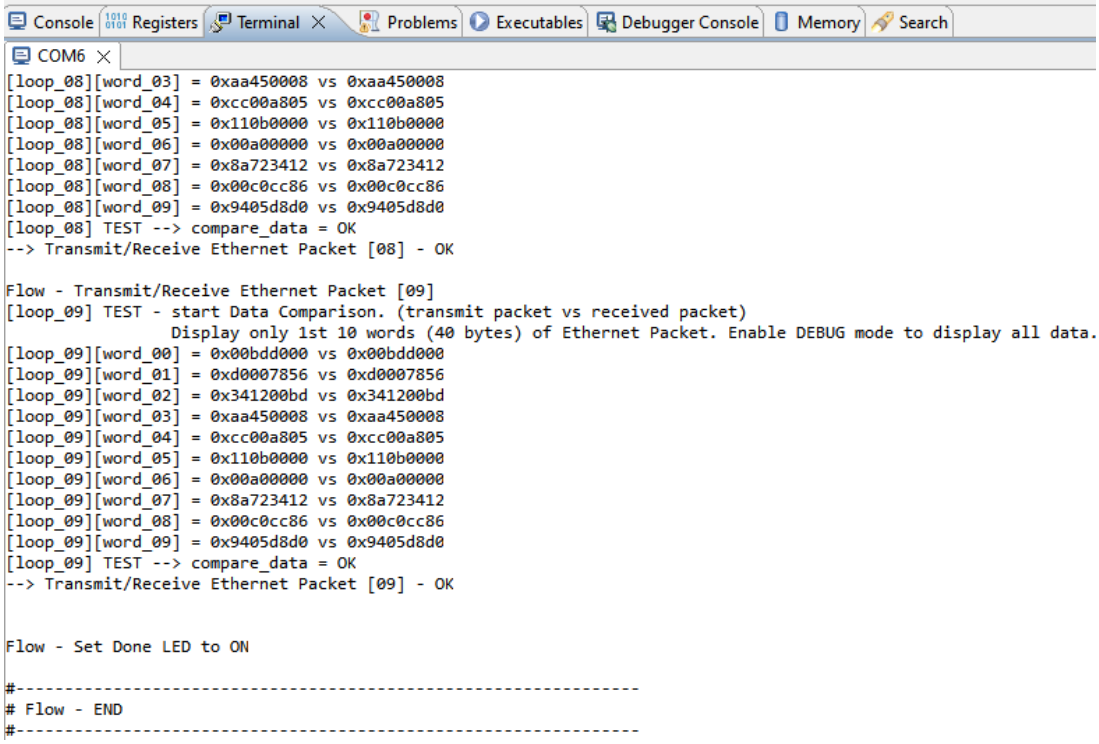


**Figure 6.12. Loopback Test - Serial Terminal Flow Completion Message**

8. On the board, the Done LED (D27) lights ON, and the Compare Packet Fail LED (D13) remains off.
9. To test 100 Mbps mode, repeat from step 3. At step 5, enter ***speed=0*** to enable 100 Mbps mode, then follow the remaining steps.

# 7. Customizing the Reference Design

This section provides guidance on how to reuse and customize this reference design for specific application or usage.
**Note**: The functionality of the reference design may be affected if any modification are made.

## 7.1. Modify RISC-V firmware

The Propel SDK project is included in this reference design.

1. Open Lattice Propel and **select** *<top>/fpga_machxo5/propelsdk* as the workspace.

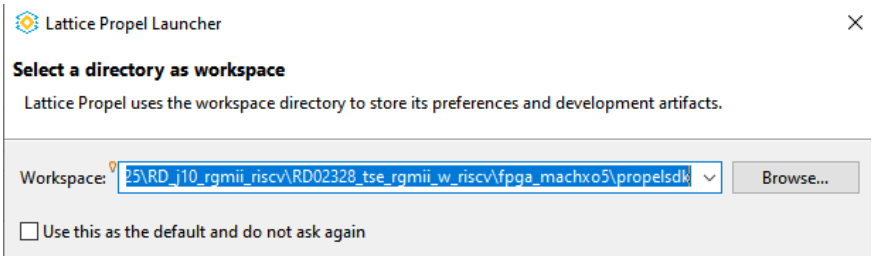


**Figure 7.1. Propel Workspace Selection**

2. Click **Launch**. The *risv_mc_rgmii* project should load as shown below.

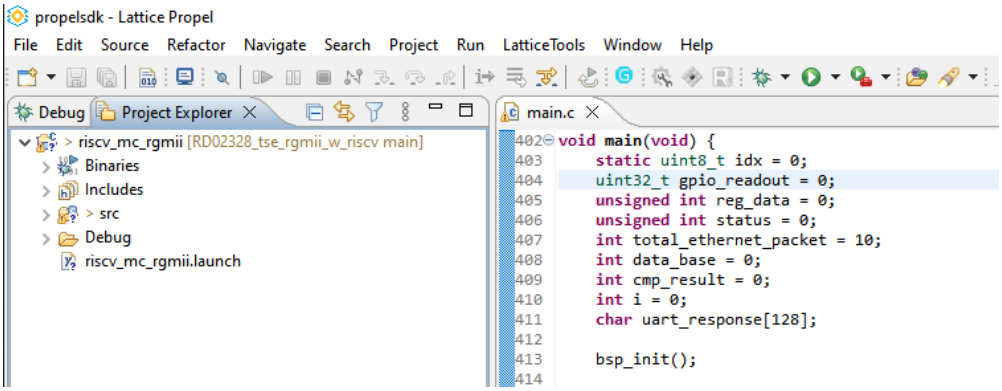


**Figure 7.2. Launching the risv_mc_rgmii Project in Propel**

3. The **main.c** is the entry point of the RISC-V firmware for this reference design. After making modification, recompile the SDK project to generate a new memory hex file.
   To integrate the new memory hex file into Radiant project bitstream, regenerate **system_memory IP** with the updated memory hex file, then recompile Radiant project.

   **Note**: User may use OCD flow to test the modified firmware without recompiling Radiant project. Refer to section 3.5 Programming and On Chip Debugging Flow of Lattice Propel SDK User Guide (FPGA-UG-02234).

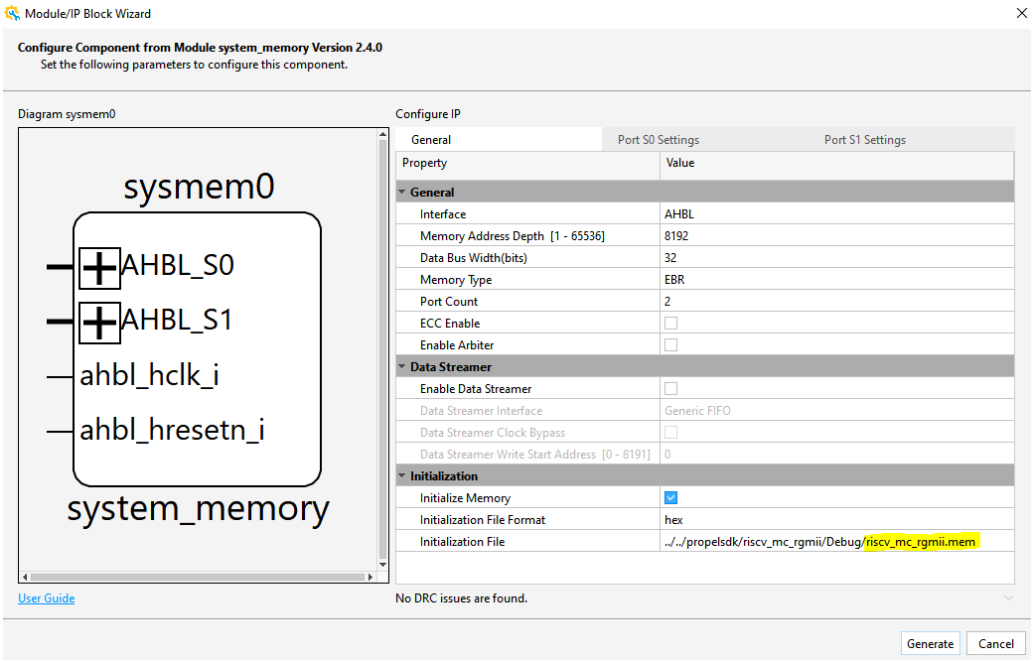


**Figure 7.3. System Memory IP Wizard**

## 7.2. Reconfiguring IPs

In this reference design, some IPs are generated using Propel Builder and others using Radiant. IPs generated in Propel Builder must be reconfigured using Propel Builder and IPs generated in Radiant must be reconfigured using Radiant.

### 7.2.1. Propel Builder IPs

To reconfigure IPs generated from Propel Builder:

1. Open the Propel Builder software and load the following Propel Builder project file (.sbx):
   *<top>/fpga_machxo5/radiant/propelbld_riscv_ss/riscv_ss.sbx*
2. In the **Schematic** view, double-click the desired IP instance to reconfigure the specific IP.

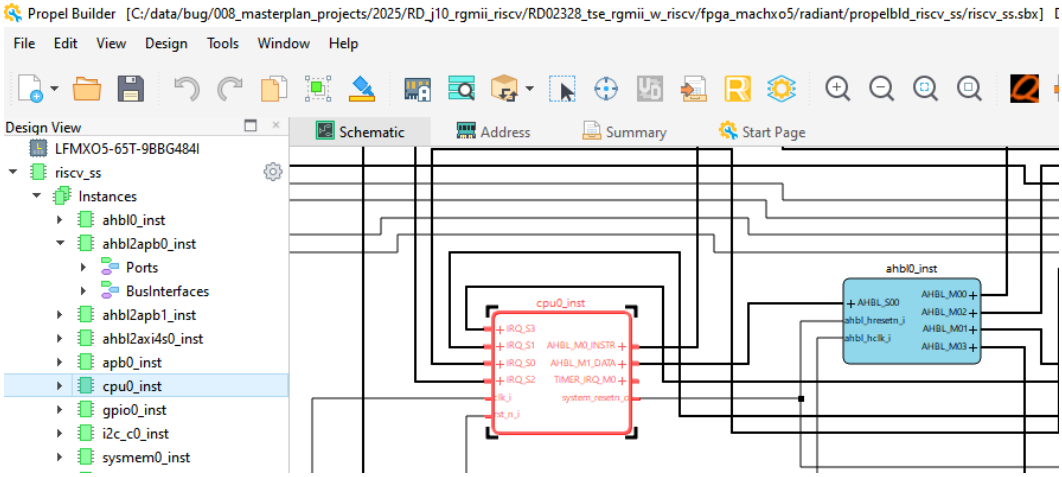


**Figure 7.4. Reconfigure an IP Instance in the Schematic View**

3. **Note**: IPs must be installed locally for reconfiguration. For IPs not installed locally, obtain the IP from IP server. Go to the **IP Catalog** and select **IP on Server** tab to locate and install the required IP.

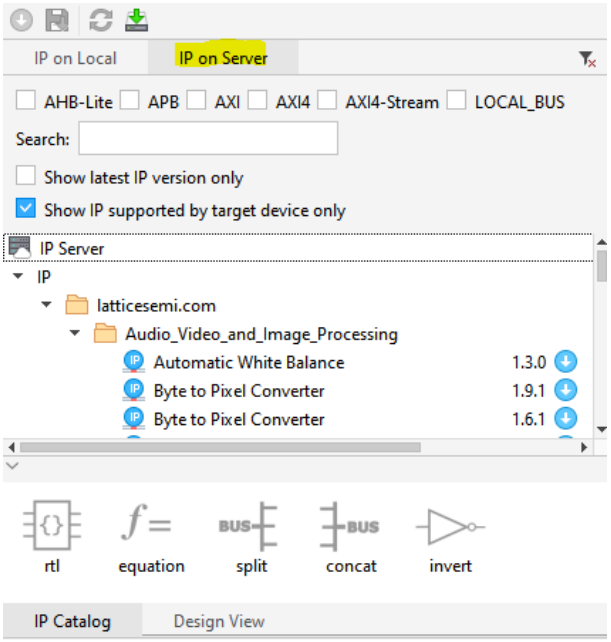


**Figure 7.5. Installing IPs from the IP Catalog using IP on Server Tab**

4. The ahbl2axi4s IP is a custom IP developed specifically for this reference design. To reconfigure this IP, **copy** the following IP source to **PropelIPLocal** directory:
   *<top>/misc/custom_ip/latticesemi.com_ip_ahbl2axi4s_bridge_1.0.1*

   Copy the entire folder as shown in the diagram below. By default, the **PropelIPLocal** directory is located at user's home directory.

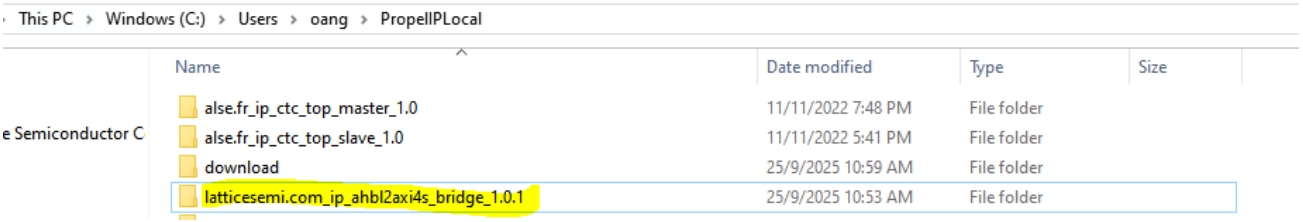


**Figure 7.6. Copying the ahbl2axi4s IP Source Folder to the PropelIPLocal Directory**

**Notes**:

- It is **NOT** recommended to configure this IP with different configurations, as it is developed for this reference design with limited validation.
- For latest version of the ahbl2axi4s custom IP, contact Lattice Sale or Tech Support. Refer to Technical Support Assistance.

### 7.2.2. Radiant IPs

Only two IPs are generated from Radiant in this reference design: the PLL IP and TSEMAC IP.

To reconfigure IPs generated from Radiant:

1. Open Radiant software and load the following Radiant project file (.rdf):
   *<top>/fpga_machxo5/radiant/riscv_rgmii.rdf*
2. Go to **File List** and double-click the desired IP for reconfiguration. As stated in Propel Builder IPs, IPs must be installed locally for configuration. Download and install missing IPs from **IP Catalog** > **IP on Server** tab.

## 7.3. Upgrading IPs

Lattice Propel Builder and Lattice Radiant can detect availability of newer IP versions during IP configuration and prompt user to use the upgraded IP version. The steps to upgrade specific IP are the same as section Reconfiguring IPs. The newer IPs version must be installed locally before performing IP upgrade.

# 8. Resource Utilization

This design is implemented in Verilog. When using this reference design in a different device, density, or speed grade, the performance and utilization can vary. Default settings are used during the design fitting.

**Table 8.1. Performance and Resource Utilization**

| Device Family | Speed Grade | $f_{MAX}$ (MHz) | Utilization | | | |
|---|---|---|---|---|---|---|
| | | | Registers (%) | LUTs (%) | EBR (%) | Others |
| MachXO5-65T | -9 | >125 | 6334 (11%) | 9181 (17%) | 26 (20%) | x1 PLL, x1 DCC, x1 DCS, x5 IDDRX1, x6 ODDRX1 |

**Note**: Performance and utilization characteristics were generated using LFMX05-65T-9BBG484I device with the Lattice Radiant software version 2025.1 and Synplify-Pro synthesis engine.

# References

- Tri-Speed Ethernet IP web page
- Tri-Speed Ethernet IP User Guide (FPGA-IPUG-02084)
- Tri-Speed Ethernet IP Release Notes (FPGA-RN-02036)
- RISC-V MC CPU IP User Guide (FPGA-IPUG-02252)
- System Memory Module User Guide (FPGA-IPUG-02073)
- System Memory Module IP Release Notes (FPGA-RN-02065)
- GPIO IP User Guide (FPGA-IPUG-02076)
- GPIO IP Release Notes (FPGA-RN-02026)
- UART IP User Guide (FPGA-IPUG-02105)
- UART IP Release Note (FPGA-RN-02023)
- PLL Module User Guide (FPGA-IPUG-02063)
- AHB-Lite Interconnect Module User Guide (FPGA-IPUG-02051)
- AHB-Lite Interconnect Module Release Notes (FPGA-RN-02044)
- AHB-Lite to APB Bridge Module User Guide (FPGA-IPUG-02053)
- APB Interconnect Module User Guide (FPGA-IPUG-02054)
- APB Interconnect Module Release Notes (FPGA-RN-02077)
- MachXO5-65T Development Board
- Wireshark software download web page
- Product web page
- Lattice Radiant FPGA design software
- Lattice Solutions Reference Designs web page
- Lattice Solutions IP Cores web page
- Lattice Propel Design Environment web page
- Lattice Propel SDK User Guide (FPGA-UG-02234)
- Lattice Radiant Software User Guide
- Lattice Insights for Lattice Semiconductor training courses and learning plans

# Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

# Revision History

**Revision 1.0, October 2025**

| Section | Change Summary |
|---|---|
| All | Initial release. |


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