Lattice Radiant 2025.2 Software Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant 2025.2 Software

- **Device Support:**
  - Certus™-NX (LFD2NX)
    - 9 (-7/-8/-9) 1.00V (COM/IND/AUTO) – CSFBGA121, CABGA196
  - Certus™-N2 (LN2-CT)
    - 20ES1 (-1/-2/-3) 0.82V (COM/IND) – CBG484
  - Lattice™ Avant (LAV-AT)
    - E70 (-1/-2/-3) 0.82V (COM/IND) – CBG484, CSG841, LFG1156, LFG676
  - MachXO4™ (LFMXO4) – This new family supports Reveal Debugger, Power Calculator, and bitstream capability.
    - 010HC (-5/-6) 2.5V/3.3V (COM/IND/AUTO) – TSG100, BSG132
    - 010HC (-5/-6) 2.5V/3.3V (COM/IND) – TSG144
    - 010HE (-5/-6) 1.2V (COM/IND/AUTO) – TSG100, BSG132
    - 010HE (-5/-6) 1.2V (COM/IND) – TSG144
    - 015HC (-5/-6) 2.5V/3.3V (COM/IND/AUTO) – TSG100, BSG132, BBG256
    - 015HC (-5/-6) 2.5V/3.3V (COM/IND) – TSG144, BFG256
    - 015HE (-5/-6) 1.2V (COM/IND/AUTO) – TSG100, BSG132, BBG256
    - 015HE (-5/-6) 1.2V (COM/IND) – UUG36, TSG144, BFG256
    - 025HC (-5/-6) 2.5V/3.3V (COM/IND/AUTO) – TSG100, BSG132, BBG256
    - 025HC (-5/-6) 2.5V/3.3V (COM/IND) – TSG144, BFG256
    - 025HE (-5/-6) 1.2V (COM/IND/AUTO) – TSG100, BSG132, BBG256
    - 025HE (-5/-6) 1.2V (COM/IND) – UUG49, TSG114, BFG256
    - 050HC (-5/-6) 2.5V/3.3V (COM/IND/AUTO) – BSG132, BBG256
    - 050HC (-5/-6) 2.5V/3.3V (COM/IND) – TSG144, BFG256, BBG400
    - 050HE (-5/-6) 1.2V (COM/IND/AUTO) – BSG132, TSG114, BBG256
    - 050HE (-5/-6) 1.2V (COM/IND) – UUG81, BFG256, BBG400

- 080HC (-5/-6) 2.5V/3.3V (COM/IND) – BBG256, BBG400
- 080HE (-5/-6) 1.2V (COM/IND) – BBG256, BBG400
- 110HC (-5/-6) 2.5V/3.3V (COM/IND) – BBG256, BBG400, BBG484
- 110HE (-5/-6) 1.2V (COM/IND) – BBG256, BBG400, BBG484

- **Tool and Other Enhancements:**
  - **Digital Signature Tab** – Support for digital signature has been added in Radiant executables for improve security and authentication.
  - **IP –** Various IP Cores are now bundled with Lattice Radiant Subscription license starting in Radiant 2025.2 release (i.e. PCIe, Ethernet, (10G & below), DDR4, LPDDR4). For complete list, please refer to the Product Bulletin FPGA-PB-02030 1.0 - Lattice Radiant Software & IP Licensing Updates.
  - **LSE –** The LSE top-module identification behavior has been updated. If top-module is not set in the LSE project file, LSE now issues a critical warning in the LSE report file.
  - **Reveal**
    - Reveal Analyzer waveforms have been improved.
    - Reveal SERDES kit now supports SERDES merge.
  - **Synplify Pro**
    - Synplify Pro now uses SLICE for register mapping instead of IOL by default.
    - The IO register is now set to “disabled” by default.
  - **Timing Analysis**
    - The “Overall Summary” section of the timing engine has been updated. Each timing corner now shows one to three lines, depending on the errors found.
    - Nexus Fast Corner STA default setting uses Vccmax for Hold time analysis. Previous releases used Vccmin by default.
  - **Timing Constraints** – A new Constraint Configuration dialog has been added to support using multiple constraint files. This feature allows users to add, remove, reorder, save, and manage individual constraint files. Only top-level constraint files are supported.

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, it may be necessary to re-create some IP, per the procedures described in the following table.

These procedures adapt the project for the changes in Radiant software.

Versions	IP Regeneration Procedures		
	Avant (LAV-AT)	**CrossLink-NX (LIFCL), Certus-N2 (LN2-CT-ES), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP), MachXO4 (LFMXO4), MachXO5-NX (LFMXO5)**	
2025.2	MPPHY	PLL	These IP used in designs created in Radiant 2025.1.1 or earlier must be re-generated in Radiant 2025.2.
	PLL	DDR_MEM	
	SEDC	MIPI_DPHY	
		MPCS	

Supported Devices

Lattice Radiant software can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
iCE40 UltraPlus (iCE40UP)	◀	◀
Lattice Avant (LAV-AT)		◀

Device Family	Free License	Subscription License
CertusPro™-NX (LFCPNX)	Evaluation Mode	◄
Certus-NX (LFD2NX)	◄	◄
Certus-N2 (LN2-CT-ES)		◄
MachXO4 (LFMXO4)	◄	◄
MachXO5-NX (LFMXO5-25)	◄	◄
MachXO5-NX (LFMXO5-100T)	Evaluation Mode	◄
MachXO5-NX (LFMXO5-35)	◄	◄
MachXO5-NX (LFMXO5-35T)	Evaluation Mode	◄
MachXO5-NX (LFMXO5-55TDQ)[1]		◄
MachXO5-NX (LFMXO5-65)	◄	◄
MachXO5-NX (LFMXO5-65T)	Evaluation Mode	◄
MachXO5-NX (LFMXO5-15D)[1]		◄
CrossLink-NX (LIFCL)	◄	◄
CrossLink-NX (LIFCL-33U)	Evaluation Mode	◄
Certus-NX-RT (UT24C)	Evaluation Mode	◄
CertusPro-NX-RT (UT24CP)	Evaluation Mode	◄

Note:

1. To enable this device, please submit a support ticket.

Support for Third-Party Synthesis and Simulator Tools

The Synopsys Synplify Pro® for Lattice synthesis tool and the Siemens QuestaSim® Lattice Edition simulator tools are included in the Radiant software.

- **Synopsys Synplify Pro FPGA synthesis software version W-2025.03LR-SP1**
  - Release Notes for Synplify Pro are located in ..\<*install_directory*>\radiant\2025.2\synpbase\doc\. The file name is release_notes.pdf.
  - A full set of documents for Synplify Pro are also located in \<*install_directory*>\radiant\2025.2\synpbase\doc\.
- **Siemens QuestaSim Lattice Edition 2025.2**
  - Release Notes for QuestaSim Lattice Edition are located in <install_directory>\radiant\2025.2\questasim\. The file names are RELEASE_NOTES.html or RELEASE_NOTES.txt.
  - A full set of documents for QuestaSim Lattice Edition are located in <install_directory>\radiant\2025.2\questasim\docs\pdfdocs.
- **Siemens Questa® 2022.3**
- **Cadence Xcelium® 24.03.003**
- **Synopsys VCS® U-2023.03-SP2**

Help Resources

- Online Help updated with CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP), and Lattice Avant (LAV-AT) content.
- To view the Online Help, start the Lattice Radiant software and select the 

"Getting Started" icon under Information Center.

  Note: The Firefox Snap install is not supported if you are using Ubuntu 20.04 or 18.04 to access the Radiant Help. This is a result of the snap install's inability to open local HTML pages. You may reinstall the latest version of Firefox using Apt install. For installation instructions, please refer to this guide.

System Requirements

The following shows the basic system requirements for Radiant software:

- Intel x86 64-bit or 64-bit-compatible PC
- OS Support:

64-bit OS	Radiant	Synplify Pro	QuestaSim
Windows 10	✓	✓	✓
Windows 11	✓	✓*	✓
Red Hat Enterprise Linux 8.10	✓	✓	✓
Ubuntu version 24.04 LTS	✓	✓*	✓*
Ubuntu version 22.04 LTS	✓	✓*	✓*

***Note**: The third-party tools have been tested by Lattice on the listed platforms, but the vendors do not officially support them.

- Approximately 50GB free disk space
- Computer Memory Requirement:
  - Nexus – 16GB
  - LAV-AT– 32GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.
- 1024 X 768 graphics display
- Network adapter for license and network connectivity
- A Web browser with JavaScript capability
- Acrobat Reader

Issues Fixed in this Release

The following known issues are fixed in this release. Their workarounds are no longer needed.

Security commands are not available for SSPI embedded programming.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-28999

Post-Synthesis fails due to invalid Clock and Multi-Cycle Path constraints when using “generate” keyword.

Devices affected: All devices

Bug number: DNG-28930

Place & Route (PAR) does not count gated clock correctly.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-28761

There is a mismatch when ECO editor initializes memory readback value.

Device affected: Lattice Avant (LAV-AT)

Bug number: DNG-27777

Timing Analysis for CDC paths may be incorrect if the following conditions are met:

- **PLL has a phase shifted clock**
- **User defined PLL output clock constraints**
- **There is a CDC path with the phase shifted PLL clock**

Device affected: All devices

Bug number: DNG-27414

Incorrect number of PIOs shown in the Device Selector Window for LFD2NX-35/65 CABGA400 packages.

The correct PIO count should be 307.

Devices affected: Certus-NX (LFD2NX-35, LFD2NX-65)

Bug number: DNG-27120

The MPP merge arbiter does not work for PMA registers.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-27079

Incorrect autogenerated clock constraints for PCIEx4 IP create_generated_clock must be used instead of create_clock.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-26433

The PLL dynamic phase adjustment is inaccurate when phase_dir = 1.

Device affected: Certus-NX (LFD2NX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-26281

Unsupported components may still pass synthesis when using both Synplify Pro and LSE.

SEDCA, UMXSPI, and UXSPI are not available for the E30ES device, but the synthesis step in Radiant project flow may still pass.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-24562

Synplify reports could not find binding for a variable.

Device affected: CrossLink-NX (LIFCL)

Bug number: DNG-21575

Using the Dynamic Clock Enable feature, re-enabled clocks do not start on falling edge of the associated clocks.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-15105

The CSI-2/DSI D-PHY Transmitter and Receiver Soft IP simulations fail when using Synopsys VCS as simulation tool.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-13225

Known Issues for Radiant 2025.2

The following are known issues for Radiant Software 2025.2. For assistance with these issues, please contact Lattice Technical support.

In Radiant 2025.2, the SHAREDEBRINIT=Disable setting for MachXO4 devices does not match Diamond's behavior for MachXO3 devices.

When disabled:

- Radiant writes EBR initialization data only once in the JEDEC file.
- Diamond writes the same EBR initialization data N times where N is the number of EBRs used for initialization.

There is no functional impact on device operation because both approaches correctly initialize EBR contents.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-30070

IBIS hardware data status is not available in the IBIS reports for all LFMXO4-080HE packages.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29994

Post-synthesis TCE does not infer the correct clock frequency from PLL.

Workaround: Use Pre-synthesis constraints editor to constrain the PLL output clocks.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29970

ECO memory initialization is not supported for LFMXO4 device.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29952

The IO mode in Physical Designer is not available for LFMXO4 devices.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29616

When the width of ROM data in a memory initialization file is wider than the defined ROM width, Radiant issues warnings and ignores the extra bits.

The synthesis engine treats these extra bits as don't-care values and ROM module may be optimized away during synthesis.
In contrast, Diamond enforces strict consistency between the ROM width and the initialization file width, resulting in an error instead of continuing.

Workaround:

- Ensure that the memory initialization file width matches the ROM width defined in your design.
- Treat Radiant warnings (e.g., CG1194, CG532, MO156) as critical and correct the file before synthesis.
- If strict error handling is required, add a manual check in your design flow to validate memory file widths.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29440

Incorrect Dual Boot Behaviour with Specific sysCONFIG Settings.

Radiant sysCONFIG settings allow you to configure CONFIGURATION, DUALBOOTGOLDEN, and MASTER_SPI_PORT to enable the Dual Boot feature. By applying specific settings, you can select the desired boot mode.

The issue occurs when the following settings are applied:

- CONFIGURATION = EXTERNAL
- DUALBOOTGOLDEN = INTERNAL
- MASTER_SPI_PORT = ENABLE

Under these settings, it is expected for the device to boot from external SPI flash first and, if configuration fails, attempt to boot from the golden image in internal flash. This fallback behavior is not supported.

Workaround: Use the supported Dual Boot mode (CFG_EXT), which boots from internal flash first and, if configuration fails, attempts to boot from the golden image in external SPI flash.

To enable this mode, set:

- CONFIGURATION = CFG
- DUALBOOTGOLDEN = EXTERNAL

- MASTER_SPI_PORT = ENABLE

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29393

IOs are missing in the Physical Designer Placement Mode.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29369

SEI Editor generates incorrect SEI information.

The SEI implementation for LFMXO4 is not yet available, which causes the GUI to display unrealistic values.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29364

The DCC and DCM resource utility in PAR report are missing.

You can still view the usage in the clock report area of the PAR report.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29345

Bitstream generation may error out when specifying custom idcode (MY_ASSP=ON).

When the “MY_ASSP” system configuration interface pin is enabled, the CUSTOM_IDCODE field becomes the device’s JTAG ID. This change leads to an issue during bitstream generation for LFMXO4 devices. The problem only occurs in designs where this field is set, not in all configurations.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29152

Internal device name is visible in DCE device part view.

Devices affected: MachXO4 (LFMXO4-015HE, LFMXO4-015HC, LFMXO4-050HC and LFMXO4-050HE) with specific packages (BFG256, BBG256 and BBG400)

Bug number: DNG-29144

Synplify Pro infers EBR blocks instead of LRAM for several clear-text designs.

Devices affected: MachXO5 (LFMXO5)

Bug number: DNG-30284

When launching Radiant using Ubuntu OS on remote sessions, the Radiant application may fail to start and display the following error: [fatal] unknown:0 - Could not initialize GLX. Aborted (core dumped).

This indicates an OpenGL/GLX initialization failure. Possible causes include:

- Missing or misconfigured GLX libraries.
- Incorrect X11 configuration for OpenGL/GLX.
- Graphics driver or hardware issues.

Workaround: Set the following environment variables before launching Radiant:

```
export QT_XCB_GL_INTEGRATION=none
export QT_QUICK_BACKEND=software
```

Devices affected: All devices

Bug number: DNG-30276

When using Structural Verilog (.vm) in the design flow, information about the synthesis attribute black_box_pad_pin “port_list” is not available in the online help.

Devices affected: All devices

Bug number: DNG-30152

When simulating certain IP cores (PCIe IP, MPCS IP, 10G MAC IP, SLVS-EC IP) using QuestaSim Lattice Edition, repeated warnings appear indicating that non-differential clock signals are being used.

The message typically states that the input signals (e.g., CLKP and CLKN) are not differential.
This warning can be ignored if the functionality is correct.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-30104

In Radiant 2025.2, the Place and Route (PAR) Design process completes successfully even though the PAR Utilization Summary reports more than 100% SLICE for LFD2NX-28.

Devices affected: Certus-NX (LFD2NX-28)

Bug number: DNG-30080

In Radiant 2025.2, the Programmer utility does not display the bitstream checksum value.

Workaround:

- There is no direct workaround in Radiant Programmer to display the embedded CRC.
- If checksum verification is required, use an external tool or script to extract and validate the 16-bit CRC from the bitstream file before programming.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG- 30013

In Radiant 2025.2, PAR ignores user location constraints for instantiated DCC and performs automatic placements of the instantiated DCCs.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-30001

Password may still show up even though the Hide/Show Password is checked/unchecked in the bitstream security settings GUI.

Devices affected: All devices

Bug number: DNG-29999

The VHDL testbench template generator utility in Radiant may fail to generate a testbench and flags errors. These errors are not caused by the user's design and should be ignored.

This only affects VHDL testbench generation. Verilog designs have no issues in generating testbenches.

Workaround:

- Users can download a patch from Lattice website that fixes this issue

Devices affected: All devices

Bug number: DNG-29978

Changing VCC in DCE and Standalone Timing Analyzer does not affect hold analysis. Hold Analysis always uses VCC Max for analysis.

Devices affected: All devices

Bug number: DNG-29957

Timing Analyzer ignores the Maximum Slack limit set by the user and displays all slacks. The display also has a mismatch in the units between Timing option setting and General information in the GUI.

This is a GUI issue and not a functional issue

Devices affected: All devices

Bug number: DNG-29930

Radiant may crash in very rare cases during implementation when Pre-synthesis Constraints Editor is open.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-29819

Standalone Physical Designer application fails to launch in Linux.

When launching Standalone Physical Designer (or the fpgae GUI) in Red Hat Enterprise Linux 8 OS, a dependency error prompt is shown in the terminal.

Workaround: Use the Radiant built-in Physical Designer.

Devices affected: All devices

Bug number: DNG-29701

LSE Synthesis may fail when CRC_Register attribute is used with an error:" CDC_Register chain cannot be fully determined for register…".

Devices affected: All devices

Bug number: DNG-29431

Post synthesis simulation may fail when top-level module is not specified in the project, and the design is compiled from the command-line using LSE synthesis engine in Linux OS.

Workaround:

- Always specify the top-level module when running LSE from the command line.
- Radiant now issues a **Critical warning** at the start of the LSE flow if no top-level module is provided, helping users correct the issue before proceeding.

Devices affected: MachXO5 (LFMXO5)

Bug number: DNG-29792

During LSE synthesis in Radiant 2025.2, the expected critical warning CRITICAL <35001747> – Bit(s) of a register stuck at '0' may not appear even when the condition exists.

This warning is intended to alert users about registers that are stuck at zero.
Workaround:

- Users should manually review synthesis reports and RTL logic for registers that may be optimized away or stuck at constant values.
- Consider using simulation or formal verification to confirm register behavior if this condition is suspected.

Devices affected: All devices

Bug number: DNG-29724

Inserting Reveal during pre-synthesis causes change in the hierarchy names when OSC IP is used. It results in timing constraints that use hierarchical objects to be dropped.

Workaround: Use Post-Synthesis Reveal debug flow.

Devices affected: All devices

Bug number: DNG-29637

Using Distributed RAM (DPRAM) for a shift-register path that feeds a Delay Element can cause the Delay Element output to behave incorrectly.

With syn_keep or syn_preserve applied to the shift array, simulation shows glitches, and Reveal capture shows unintended or corrupted data. The problem is observed in both pre-synthesis and post-synthesis Reveal.

Workaround:

- Avoid DPRAM for the shift chain feeding the Delay Element. Use EBR or PFU registers for the shift register resource.
    - In IP configuration, select EBR or Registers as the resource.
    - For inferred RTL, guide synthesis to map to block RAM or registers (e.g., set ramstyle to block RAM or registers in your synthesis attributes).
- If you must use DPRAM:
    - Keep the shift depth ≤ 32 where practical to reduce risk.
    - Remove syn_keep and syn_preserve on the internal shift array when not strictly required or apply them at module boundaries instead of the array element level.
- Reverify with simulation and Reveal after changing the resource selection. Designs using EBR or PFU registers do not show the issue.

Devices affected: Lattice Avant (LAV-AT-E70)

Bug number: DNG-29618

When a .fdc constraints file is used for synthesis, Synplify Pro issues an error message “Input file <file>.fdc does not end with .ldc. Please provide a valid file type”

Workaround: Use .sdc file for synthesis

Devices affected: All devices

Bug number: DNG-29306

Gate-level timing simulation may show an unexpected jitter for PLL.

This only affects the gate level timing simulation and HW behavior is unaffected.

Devices affected: Lattice Avant (LAV-AT-E70)

Bug number: DNG-29299

In Radiant 2025.2, when viewing timing paths in Netlist Viewer, the displayed paths may be incorrect or appear disconnected. This occurs when clicking on timing paths from the Timing Analysis report to cross-probe into the Netlist Viewer.

Workaround: Use the Timing Analysis report as the source of truth for timing paths and slack values.

Devices affected: All devices

Bug number: DNG-29138

LSE synthesis may fail without providing a clear error message if the design includes module instantiations that do not have instance names.

The same design may be compiled successfully with Synplify Pro but later fail during PAR.
Workaround:

- Always provide instance names for all module instantiations in your design.
- If the design fails without an error message, review the RTL for unnamed instances and update them accordingly.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-29029

LSE synthesis may fail with an error if the project path length is too long. This occurs because the synthesis engine has a limit on the maximum path length it can handle for project files and directories.

Workaround:

- Shorten the project path by:
    - Moving the project to a directory closer to the root (e.g., C:\RadiantProjects\).
    - Reducing folder name lengths.
- Avoid using excessively long directory structures for project files.

Devices affected: All devices

Bug number: DNG-28606

The bitstream hardware data status of LFD2NX-35/65 is missing.

The bitstream hardware data status is Preliminary.

Devices affected: Certus-NX (LFD2NX-35, LFD2NX-65)

Bug number: DNG-28463

Radiant may crash during implementation when DCE is open.

Workaround: Close DCE and run implementation.

Devices affected: Certus-NX (LFD2NX-35, LFD2NX-65)

Bug number: DNG-28678

When using Avant PLL IP configured with an LMMI interface, synthesis fails in Synplify Pro with an error. The issue occurs during synthesis and prevents successful compilation of the design.

Workaround:

- Use the PLL IP without the LMMI interface if possible.
- If LMMI functionality is required, consider alternative design approaches or contact Lattice support for guidance until a fix is available.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-27611

In Certus-NX LRAM IP simulation, when DPS is asserted high, lram_ready may remain high instead of going low.

This does not affect HW functionality and only affects simulation.
Expected behavior: Driving DPS high powers down LRAM, so lram_ready should be low.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-27555

When using Radiantc for ECO flows, the eco_config_memory command requires the design database to be initialized first. If des_read_udb is not executed before eco_config_memory, memory configuration will fail.

Workaround:

- Before running eco_config_memory in Radiantc, execute: des_read_udb
- This ensures the design database is loaded and memory initialization completes successfully

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-27493

Designs using nested VMs fail during post-synthesis.

Workaround: Do not use nested VMs. Instantiate VMs separately.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-27317

When using Synplify Pro, user-defined create_generated_clock constraints in the SDC file for PLL clock outputs may be overwritten by auto-generated PLL clock constraints if a Reveal Core is added to the design.

Without Reveal, user-defined constraints propagate correctly through synthesis and implementation. With Reveal present, the constraints are accepted during Constraint Propagation Engine (CPE) but fail to persist after synthesis.

Workaround:

- Define PLL clock constraints in the PDC file instead of SDC. PDC constraints are preserved even when Reveal is added.
- If SDC-based constraints are required, use post-synthesis Reveal debug flow.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-26270

Programming may fail when using compressed bitstreams.

Workaround: Use plain or uncompressed bitstream formats.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-26097

Radiant timing analysis for designs using LMMI_CLK / LMMI_CLKO may show:

- **A missing timing arc from OSCA to CONFIG_CLKRST_CORE on the LMMI clock path (this is a bug).**
- **A 0 ns net delay from CONFIG_CLKRST_CORE to CONFIG_LMMI (this is expected behavior per the current timing model).**

As a result, the report may present a direct path from the OSC IP to CONFIG_LMMI without explicitly reflecting the expected clock path delay from LMMI_CLK to LMMI_CLKO (i.e., OSCA → CONFIG_CLKRST_CORE).

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-27889

Standalone Timing Analyzer results may differ from RunSTA results even when using the same pdc file.

The results from RunSTA are correct.
Workaround: Avoid using Standalone Timing Analyzer and use RunSTA for debug.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-27523

Timing analysis and the Tcl command “sta_get_slack -worst” may return different worst slack values.

The command may return a slack value, but it might not be the worst-case slack. The returned slack is valid, but it corresponds to a path that does not represent the worst slack.

In addition, the detailed timing report may contain some arrival values that are incorrect. However, the path of the report, the delays of the connections and arcs along the path, the required value, the arrival value used for slack computation, and the slack of the path are all correct.

Device affected: All devices

Bug number: DNG-27408

The power file revision is shown as advanced in LFMXO5-35/35T/65/65T devices.

The power file revision should be Preliminary.

Devices affected: MachXO5-NX (LFMXO5-35, LFMXO5-35T, LFMXO5-65, LFMXO5-65T)

Bug number: DNG-26755

In PLL simulation, the phase stops moving when it goes over 360 degrees.

In a Phase-Locked Loop (PLL) simulation, the phase should not stop moving but only reset to stay within a specific range (such as 0°–360).

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-23458

Synplify Pro synthesis may fail if the .sdc file contains a user-defined constraint referencing a hierarchical object that includes a dot (.). Example: top.inst/out.

Workaround:

- Create the constraint in the .pdc file instead of .sdc file.
- Use LSE for synthesis.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-20134

Radiant may crash on version 2025.2 due to libbasct.dll.

Workaround: If you encounter this issue, try one of the following solutions:

1. Contact Lattice Technical Support to request for the unencrypted libbasct.dll.
2. Whitelist the specific dll in antivirus software (already documented in troubleshooting guide section).

Devices affected: MachXO5-NX (LFMXO5)

Bug number: DNG-27676

Synplify Pro Fails to Optimize Resource on pmi_fifo design if Reveal Core is inserted causing undesired toggling of the empty flag of the FIFO.

Workaround: Use Post-Synthesis Reveal Debug flow

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-24358

The des_report_flow_status command may show incomplete status after restoring a milestone with prj_open_milestone, because it relies on session history rather than the design database.

Workaround: After restoring a milestone with prj_open_milestone, run the appropriate flow stage again (such as synthesis or PAR) before calling des_report_flow_status. This refreshes the session history so the status reflects correctly.

Devices affected: All FPGAs

Bug number: DNG-29723

When opening the Place & Route Timing Analysis report in Radiant, the displayed content may appear truncated, preventing users from viewing the full report details. This is a display issue in the report viewer.

Workaround: Click on the contents to view the next section of the report.

Devices affected: All FPGAs

Bug number: DNG- 29808

When opening or double-clicking an .ipx file, the Module/IP Block Wizard window may appear too small, making its contents difficult to read or navigate. This is a GUI scaling issue and does not affect the functionality of the IP configuration.

Workaround: After the Module/IP Block Wizard window pop-up appears, manually enlarge the window by dragging its corners or edges to the desired size.

Devices affected: All FPGAs

Bug number: DNG-29827

On Avant devices, the FIFO empty signal may not match the synthesis or Place-and-Route (PAR) netlist behavior if the clear signal is asserted during the first clock cycle. This can lead to incorrect FIFO status reporting immediately after reset.

Workaround:

- Do not assert the clear signal during the first clock cycle.
- Apply the clear signal after at least one valid clock cycle has elapsed to ensure proper alignment of the FIFO empty signal.
- Verify FIFO behavior in simulation and hardware after applying this change.

Devices affected: Avant (LAV-AT)

Bug number: 24704