



XAUI IP

IP Version: v1.1.0

Release Notes

FPGA-RN-02104-1.0

December 2025

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Contents 3

1. Introduction 4

 XAUI IP v1.1.0 4

 XAUI IP Earlier Versions 4

References 5

Technical Support Assistance 6

1. Introduction

This document contains the Release Notes for the XAUI IP. For specific details about the IP, refer to the following:

- [XAUI IP User Guide \(FPGA-IPUG-02160\)](#)

XAUI IP v1.1.0

Software	Software Version	Summary of Changes
Lattice Radiant™	2025.2	<ul style="list-style-type: none">• Enabled Avant™-AT-G/X device support.• Removed MDIO interface.• Enabled SDC flow and updated timing constraints for easier integration by replacing set_clock_groups with set_false_paths.

XAUI IP Earlier Versions

IP Version	Summary of Changes
1.0.1	Updated the license string.
1.0.0	Initial release.

References

- [XAUI IP User Guide \(FPGA-IPUG-02160\)](#)
- [XAUI 10G Ethernet Attachment Unit Interface IP Core](#) web page
- [CertusPro-NX FPGA](#) web page
- [Avant-G](#) web page
- [Avant-X](#) web page
- [Lattice Radiant Software](#) web page
- [Lattice Propel Design Environment](#) web page
- [Lattice Solutions IP Cores](#) web page
- [Lattice Solutions Reference Designs](#) web page
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.



www.latticesemi.com