Lattice Radiant 2025.1.1 Software Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant 2025.1.1 Software

- **Device Support:**
  - Certus™-NX (LFD2NX)
    - The BBG400 package for LFMXO5-35/65 and LFD2NX-35/65, as well as the CABGA256 package for LFD2NX-25, have been changed from 'generally available' to 'controlled access.'
    - To request for a license, you may raise a ticket to the Submit Support Ticket page.
  - Lattice Avant™-NX (LAV-AT)
    - E50 (-1/-2/-3) 0.82V (COM/IND) – CSG841
  - MachXO5™-NX (LFMXO5)
    - 35T (-7/-8/-9) 1.00V (COM/IND) – BBG256
    - 65T (-7/-8/-9) 1.00V (COM/IND) – BBG256

- **Tool and Other Enhancements:**
  - **Device**
    - The license string for -7 speed grade has been removed for LIFCL-17 UWG72 package.

      Note: This is now supported with Radiant free license.
    - The status of the following LAV-AT-E70 packages has been changed from "Advanced" to Preliminary":
      - LFG676
      - CSG841
      - CBG484
  - **Design Tcl Commands** – Design commands now support the des_get_ram_cells and des_get_ram_style.
    - des_get_ram_cells retrieves memory cells that are implemented as either distributed RAM or block RAM.
    - des_get_ram_style returns the memory style of a specified RAM cell.

- **Programmer** – Status check code after reboot has been removed. This avoids failure when the device exits user mode while STAPL is still trying to read the status register.

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, it may be necessary to re-create some IP, per the procedures described in the following table.

These procedures adapt the project for the changes in Radiant software.

Versions	IP Regeneration Procedures		
	Avant (LAV-AT)	**CrossLink-NX (LIFCL), Certus-N2 (LN2-CT-20ES), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP), MachXO5-NX (LFMXO5)**	
2025.1.1	MPPHY	PLL	These IP used in designs created in Radiant 2025.1 or earlier must be re-generated in Radiant 2025.1.1.
	PLL	DDR_MEM	
	SEDC	MIPI_DPHY	
		MPCS	

Supported Devices

Lattice Radiant software can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
iCE40 UltraPlus (iCE40UP)	◀	

Device Family	Free License	Subscription License
Lattice Avant (LAV-AT)		◄
CertusPro™-NX (LFCPNX)	Evaluation Mode	◄
Certus-NX (LFD2NX)	◄	
Certus-N2 (LN2-CT-20ES)		◄
MachXO5-NX (LFMXO5-25)	◄	
MachXO5-NX (LFMXO5-100T)	Evaluation Mode	◄
MachXO5-NX (LFMXO5-35)	◄	
MachXO5-NX (LFMXO5-35T)	Evaluation Mode	◄
MachXO5-NX (LFMXO5-65)	◄	
MachXO5-NX (LFMXO5-65T)	Evaluation Mode	◄
MachXO5-NX (LFMXO5-15D)[1]		◄
CrossLink-NX (LIFCL)	◄	
CrossLink-NX (LIFCL-33U)	Evaluation Mode	◄

Note:

1. To enable this device, please submit a support ticket.

Support for Third-Party Synthesis and Simulator Tools

The Synopsys Synplify Pro® for Lattice synthesis tool and the Siemens QuestaSim® Lattice Edition simulator tools are included in the Radiant software.

- **Synopsys Synplify Pro FPGA synthesis software version V-2023.09LR-3**
  - Release Notes for Synplify Pro are located in ..\<*install_directory*>\radiant\2025.1\synpbase\doc\. The file name is release_notes.pdf.
  - A full set of documents for Synplify Pro are also located in \<*install_directory*>\radiant\2025.1\synpbase\doc\.
- **Siemens QuestaSim Lattice Edition 2024.2**
  - Release Notes for QuestaSim Lattice Edition are located in <install_directory>\radiant\2025.1\questasim\. The file names are RELEASE_NOTES.html or RELEASE_NOTES.txt.
  - A full set of documents for QuestaSim Lattice Edition are located in <install_directory>\radiant\2025.1\questasim\docs\pdfdocs.
- **Siemens Questa® 2022.3**
- **Cadence Xcelium® 23.03.003**
- **Synopsys VCS® U-2023.03-SP2**

Help Resources

- Online Help updated with CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP), and Lattice Avant (LAV-AT) content.
- To view the Online Help, start the Lattice Radiant software and select the 

"Getting Started" icon under Information Center.

  Note: The Firefox Snap install is not supported if you are using Ubuntu 20.04 or 18.04 to access the Radiant Help. This is a result of the snap install's inability to open local HTML pages. You may reinstall the latest version of Firefox using Apt install. For installation instructions, please refer to this guide.

System Requirements

The following shows the basic system requirements for Radiant software:

- Intel x86 64-bit or 64-bit-compatible PC

- OS Support:

64-bit OS	Radiant	Synplify Pro	QuestaSim
Windows 10	✓	✓	✓
Windows 11	✓	✓*	✓*
Red Hat Enterprise Linux 7.9	✓	✓	✓
Red Hat Enterprise Linux 8.10	✓	✓	✓
Ubuntu version 20.04 LTS	✓	✓*	✓*
Ubuntu version 22.04 LTS	✓	✓*	✓*

***Note**: The third-party tools have been tested by Lattice on the listed platforms, but the vendors do not officially support them.

- Approximately 50GB free disk space
- Computer Memory Requirement:
  - Nexus – 16GB
  - LAV-AT– 32GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.
- 1024 X 768 graphics display
- Network adapter for license and network connectivity
- A Web browser with JavaScript capability
- Acrobat Reader

Issues Fixed in this Release

The following known issues are fixed in this release. Their workarounds are no longer needed.

Pinout file for LAV-AT-E70-3CBG484C in Radiant 2025.1 is outdated.

Device affected: Lattice Avant (LAV-AT)

Bug number: DNG-28440

MPP merge utility to check phy_tx_mpll_sel setting instead of DATA_RATE when determining PLLA/PLLB usage.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-26386

There is a discrepancy between the pinout files in the web version and the Radiant version.

Radiant pinout files are outdated.

Devices affected: Certus-NX (LFD2NX-15)

Bug number: DNG-28408

When using Reveal, Synplify Pro may issue an error: "ERROR <2019992> - Error in encrypted block" related to the generated Reveal verilog file.

Workaround: Contact Lattice technical support.

Devices affected: All devices

Bug number: DNG-27465

Setting the FIFO DC “Controller Implementation” parameter to “Area-Optimized (HW)” is not functional due to an issue in the E70ES1 device.

Device affected: Lattice Avant (LAV-AT-ES1)

Bug number: DNG-27444

MPPHY IP pma_rx*_blk_lock_o status port toggles using Near End Parallel Loopback.

Device affected: Lattice Avant (LAV-AT)

Bug number: DNG-27445

For Avant designs when placing CE and SR with different polarities on the same SLICE, placement may fail.

Workaround: Modify the design to eliminate the use of register control signals with both positive and negative polarities. For instance, generate a new signal to inverse the polarity and use that signal.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-25568

When trying to synthesize a SEDC design from the SEDC IP, an error occurs that says the FAKE_SEDC_CRAM_FRM_ERRLOC parameter is set to an invalid value.

Device affected: Lattice Avant (LAV-AT)

Bug number: DNG-23841

Reveal Power-on Reset (POR) Debug function does not work when using LSE with only one Trigger Unit (TU).

Workaround: Add another Trigger Unit (TU) that can be unrelated to POR Debug.

Devices affected: All devices except iCE40UP

Bug number: DNG-13901

Known Issues for Radiant 2025.1.1

The following are known issues for Radiant Software 2025.1.1. For assistance with these issues, please contact Lattice Technical support.

Avant CRE simulation may fail to complete due to a fatal error encountered during execution.

Workaround: You can use Radiant 2024.2.1.330.0

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-29026

Certain programming operations using compressed bitstream (RBT format) are currently not functional due to a known software limitation.

Workaround: Use plain or uncompressed bitstream formats.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-26097

Post-Synthesis fails due to invalid Clock and Multi-Cycle Path constraints when using “generate” keyword.

When using Synplify Pro, synthesis may fail during the post-synthesis stage due to invalid clock or multi-cycle path constraints. This issue typically occurs when the user design includes the "generate" keyword in module declarations, especially in clock divider modules. In such cases, the tool may generate invalid constraints, leading to post-synthesis errors.

Workaround: If you encounter this issue, try one of the following solutions:

1. Modify the Design – Remove the “generate” keyword from module or instance names involved in clock divider logic to prevent constraint generation issues.
2. Manual Constraint Cleanup – After synthesis, open the “*_impl_1.ldc” file located in the impl_1 directory. Manually delete the invalid constraint commands. Then, click the Synthesis button to resume the flow from the post-synthesis stage

Devices affected: All devices

Bug number: DNG-28930

Place & Route (PAR) does not count gated clock correctly.

In Radiant 2023.2.1, PAR only counts gated clocks driven by PFU. If clocks with other drivers also use gated clock resources, clock placement may fail.

Workaround: Remove the signals from PCLK selection using the following constraint:

- ldc_set_attribute USE_PRIMARY=FALSE [get_nets {signal_name}]

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-28761

The bitstream hardware data status of LFD2NX-35/65 is missing.

The bitstream hardware data status is Preliminary.

Devices affected: Certus-NX (LFD2NX-35, LFD2NX-65)

Bug number: DNG-28463

Missing Timing Arc: OSCA to CONFIG_CLKRST_CORE for LMMI_CLK clock path.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-27889

Timing Analysis for CDC paths may be incorrect if the following conditions are met:

- **PLL has a phase shifted clock**
- **User defined PLL output clock constraints**
- **There is a CDC path with the phase shifted PLL clock**

Device affected: All devices

Bug number: DNG-27414

Incorrect number of PIOs shown in the Device Selector Window for LFD2NX-35/65 CABGA400 packages.

The correct PIO count should be 307.

Devices affected: Certus-NX (LFD2NX-35, LFD2NX-65)

Bug number: DNG-27120

Incorrect Autogenerated Clock constraints for PCIEx4 IP create_generated_clock must be used instead of create_clock.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-26433

Synplify reports could not find binding for a variable.

Device affected: CrossLink-NX (LIFCL)

Bug number: DNG-21575

Standalone Timing Analyzer results may differ from RunSTA results, even when using the same pdc file.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-27523

The PLL dynamic phase adjustment is inaccurate when phaase_dir = 1.

Device affected: Certus-NX (LFD2NX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-26281

Timing analysis and the Tcl command “sta_get_slack -worst” may return different worst slack values.

The command may return a slack value, but it might not be the worst-case slack. The returned slack is valid, but it corresponds to a path that does not represent the worst slack.

In addition, the detailed timing report may contain some arrival values that are incorrect. However, the path of the report, the delays of the connections and arcs along the path, the required value, the arrival value used for slack computation, and the slack of the path are all correct.

Device affected: All devices

Bug number: DNG-27408

The MPP merge arbiter does not work for PMA registers.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-27079

The power file revision is shown as advanced in LFMXO5-35/35T/65/65T devices.

The power file revision should be Preliminary.

Devices affected: MachXO5-NX (LFMXO5-35, LFMXO5-35T, LFMXO5-65, LFMXO5-65T)

Bug number: DNG-26755

The location for a secured component (Hard DPHY) cannot be changed.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-24746

Unsupported components may still pass synthesis when using both Synplify Pro and LSE.

SEDCA, UMXSPI, and UXSPI are not available for the E30ES device, but the synthesis step in Radiant project flow may still pass.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-24562

CONFIG_LMMIE and CONFIG_LMMIB RTL simulation fails.

Devices affected: MachXO5-NX (LFMXO5)

Bug number: DNG-22187

The clock, using pclk routing and connected only to fabric registers, has a lower clock MPW at the higher speed grade (-8).

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-21315

The CSI-2/DSI D-PHY Transmitter and Receiver Soft IP simulations fail when using Synopsys VCS as simulation tool.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-13225