DDR Pin Planner Tool

User Guide

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Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
CK	Clock
DDR	Double Data Rate
DDR3	Double Data Rate 3
DDR3L	DDR3 Low Voltage
DQ	Data Signal
DQS	Data Strobe
FPGA	Field Programmable Gate Array
GUI	Graphical User Interface
IP	Intellectual Property
LPDDR	Low Power DDR
LPDDR4	Low Power DDR 4
PCIe	Peripheral Component Interconnect Express
PDC	Post-Synthesis Constraint
SDRAM	Synchronous Dynamic Random Access Memory

1. Introduction

Determining pinouts for Double Data Rate (DDR) or Low Power Double Data Rate (LPDDR) memory interfaces is a complex process that requires careful consideration of high-speed I/O pinout generation rules. This includes dedicated data strobe (DQS), data byte grouping (DQ), clock signals (CK), address, command, and control signals.

The DDR Pin Planner Tool simplifies this process by generating proposed pinouts for DDR3, DDR3L, or LPDDR4 external memory interfaces on Lattice Nexus™ and Lattice Avant™ FPGAs.

1.1. Overview of the DDR Pin Planner Tool

The DDR Pin Planner Tool is an Excel-based Graphical User Interface (GUI) tool designed to specify either a target FPGA device and memory interface configuration or a supported Lattice Development Kit.

Based on the selected inputs, the tool generates a set of recommended pinouts, which can be added to an existing Post-Synthesis Constraint (.pdc) file within a Lattice Radiant project.

The generated pinouts can be used for final implementation if the Place & Route process completes successfully during project compilation.

Note: The generated pinouts serve as an example of valid pin assignments that follow typical configurations and assignment rules. However, they should not be considered as the only valid set of pinouts.

2. Getting Started

2.1. System Requirements

To run the Lattice DDR Pin Planner Tool, the following system requirements must be met:

- Microsoft Windows 10 or Windows 11 operating system
- Microsoft Excel 2016 or later (Office 365 recommended)

Note: The GUI is not compatible with Excel Online or mobile versions.

2.2. Setting Up & Enabling Macros

When launching the DDR Pin Planner Tool for the first time, a security risk message may appear as an indicator that the DDR Pin Planner Excel File has not been marked as a trusted file.

Figure 2.1. Disabled Macros Security Risk Message

To ensure full functionality of the macro-based GUI:

1. Close the DDR Pin Planner Tool if it is already open.
2. To disable the Microsoft Security setting for the DDR Pin Planner Tool, right-click the Excel file and select **Properties**.
3. Check the **Unblock** option under **General** tab in the **Properties**.
4. Click **Apply** and **OK**.

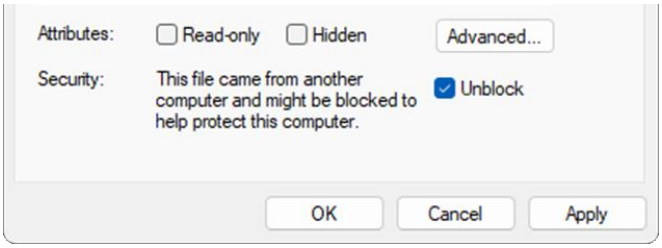

Figure 2.2. Unblocking DDR Pin Planner Tool Macros

After reopening the file, Excel may display a security warning indicating that macros are disabled. Click **Enable Content** to allow the macros to run.

Figure 2.3. Disabled Macros Security Warning Message

3. Running the DDR Pin Planner Tool

The DDR Pin Planner Tool provides a user-friendly interface for determining valid pinouts for DDR and LPDDR memory interfaces on Lattice Nexus and Lattice Avant FPGAs.

To launch the interface, select **DDR Pin Planner** from the introduction page shown in Figure 3.1. Running DDR Pin Planner Tool.

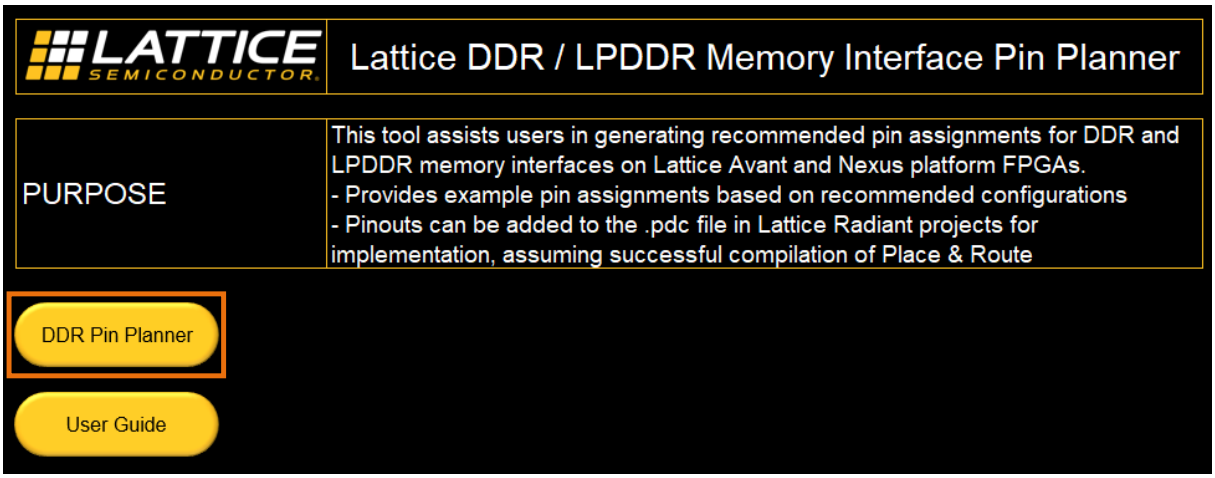

Figure 3.1. Running DDR Pin Planner Tool

A new window opens with two tabs: **General** and **Board**.

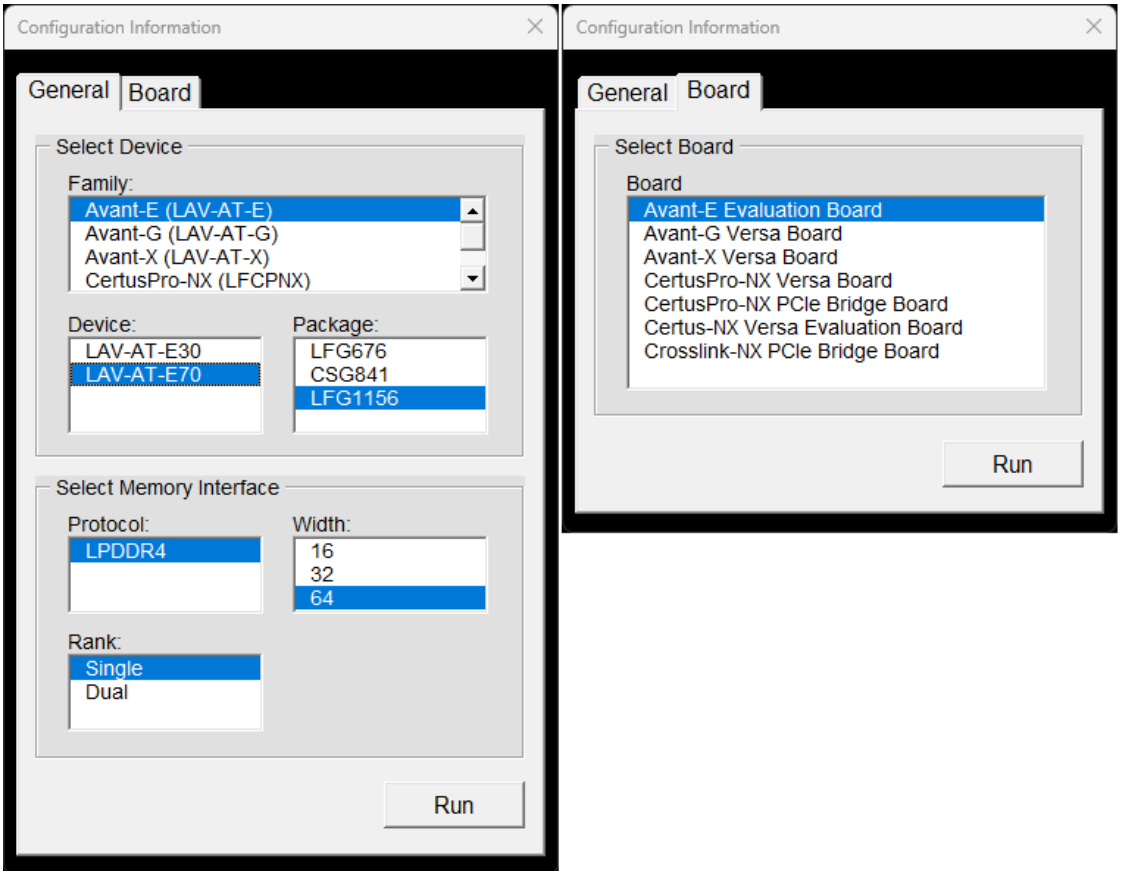

Figure 3.2. Configuration Information: General and Board Tabs

3.1. General Tab

Use the **General** tab when starting from scratch or targeting a custom board. This tab includes the following fields:

- Under Select Device:
  - Family
  - Device
  - Package
- Under Memory Interface:
  - Protocol: DDR3, DDR3L, or LPDDR4
  - Bus Width: 16, 32, or 64
  - Number of Ranks: Single or Dual

For a complete list of supported memory controller IPs, devices, and configurations, refer to Table 3.1. Memory IPs, Devices, and DDR or LPDDR Support Summary.

Table 3.1. Memory IPs, Devices, and DDR or LPDDR Support Summary

IP Core Name	Device	DDR/LPDDR Interface[1]
DDR Memory Controller IP Core	Avant-E/G/X	• LPDDR4 • x16, x32, or x64 • Single or Dual Rank
LPDDR4 Memory Controller IP Core for Nexus Devices	CertusPro™-NX	• LPDDR4 • x16 or x32 • Single or Dual Rank
DDR3 SDRAM Controller IP Core for Nexus Devices	• Certus™-NX • CrossLink™-NX • CertusPro-NX	• DDR3 or DDR3L • x8, x16, x24, or x32 • Single Rank

Note:

1. Not all device or package combinations can support all the listed bus widths or ranks.

After selecting an FPGA device, package, and memory configuration, click **Run**. This triggers the tool to generate an example set of pinouts to accelerate the design process and illustrate typical pinout configurations.

3.2. Board Tab

Use the **Board** tab when working with a Lattice Development Kit that contains DDR3, DDR3L or LPDDR4 external memory support.

When a board is selected, the tool automatically apply board-specific settings, including memory protocol, bus width, and number of ranks. For a complete list of supported boards and their memory configurations, refer to Table 3.2. Development Kit & DDR/LPDDR Support Summary.

Table 3.2. Development Kit & DDR/LPDDR Support Summary

Board Name	Featured DDR/LPDDR Memory Configuration
Avant-E Evaluation Board	LPDDR4 (x32, Single Rank)
Avant-G Versa Board	LPDDR4 (x32, Single Rank)
Avant-X Versa Board	LPDDR4 (x32, Single Rank)
CertusPro-NX Versa Board	LPDDR4 (x32, Single Rank)
CertusPro-NX PCIe Bridge Board	LPDDR4 (x32, Single Rank)
Certus-NX Versa Evaluation Board	DDR3/DDR3L (x16, Single Rank)
CrossLink-NX PCIe Bridge Board	DDR3/DDR3L (x16, Single Rank)

After selecting a board, click **Run**. This trigger the tool to generate a set of validated pin assignments to accelerate the design process and provide insight into typical pinout configurations.

Note: The generated pinouts serve as an example of valid pin assignments that follow typical configurations and assignment rules. However, they should not be considered as the only valid set of pinouts.

4. Results

After clicking **Run**, the tool generates pin assignments and displays the pinouts in the **Result** sheet, as shown in Figure 4.1. Generated Pin Assignments Result Sheet.

Note: The signal names in the generated output follow the naming conventions used in the example designs of the memory controller IPs. If the top-level memory interface signals use different names, the generated pinout signal names in Post-Synthesis Constraint (.pdc) file must be updated before compilation.

Figure 4.1. Generated Pin Assignments Result Sheet

Above the generated pin assignments, three buttons are available:

- Copy to Clipboard
- Append to .pdc
- Clear Pinouts

4.1. Copy to Clipboard

Click **Copy to Clipboard** to copy the generated pinouts for manual pasting into a .pdc file.

4.2. Append to .pdc

Click **Append to .pdc** to insert the generated pinouts into an existing .pdc file. A **Confirm Overwrite** dialog box appears, warning that any previously generated pinouts will be overwritten.

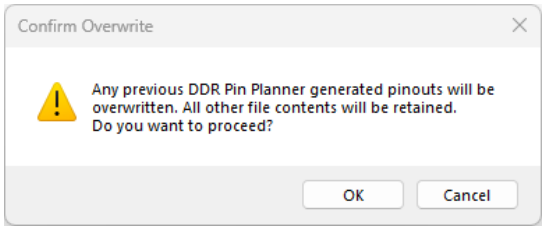

Figure 4.2. Confirm Overwrite Alert

Any content inserted between previously generated pinouts will be overwritten. Specifically, all text between the header and footer will be replaced in the .pdc file. Below shows an example of the generated header and footer in the .pdc file.

```
Header: #The following pinouts are auto-generated by the Lattice DDR Pin Planner
.
.
.
Footer: #End of generated pinouts
```

It is recommended to review the .pdc file contents before proceeding with the append operation. After clicking **OK** in the **Confirm Overwrite** dialog box, a **Select a .pdc file** window open. Choose the file to update with the generated pinouts.

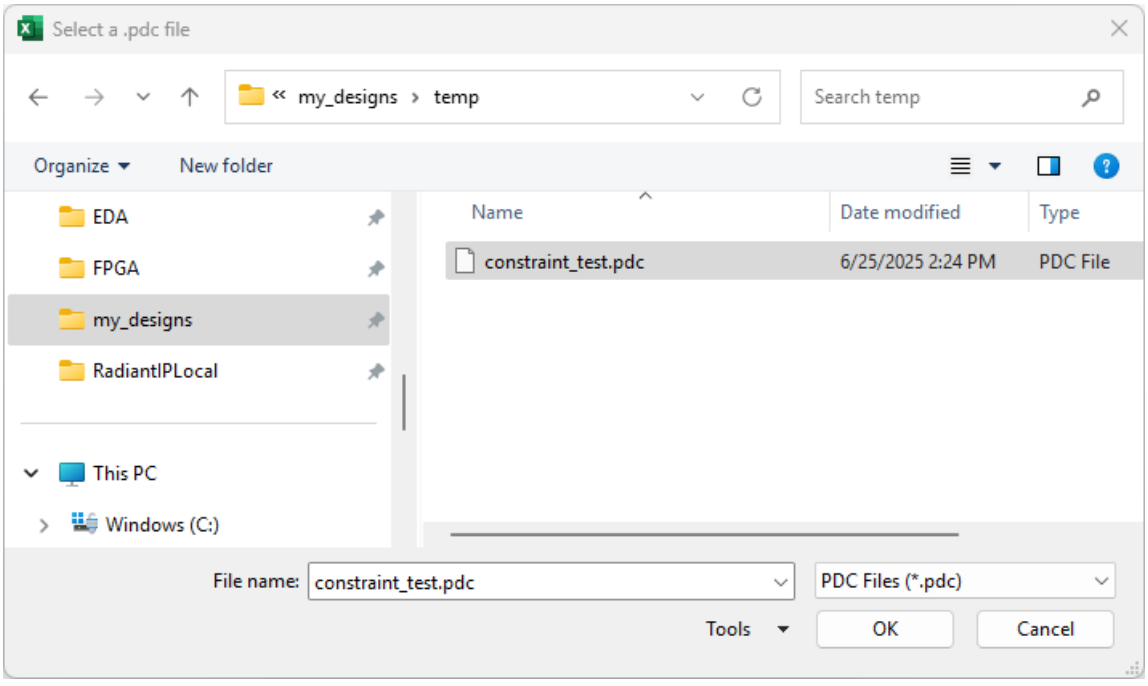

Figure 4.3. Select a PDC File Dialog Box

After selecting a .pdc file, click **OK**. If the update is successful, a confirmation dialog box appears indicating that the .pdc file has been updated successfully.

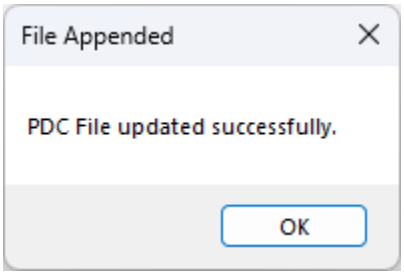

Figure 4.4. Successful File Appended Notification

4.3. Clear Pinouts

Click **Clear Pinouts** to remove all generated pin assignments from the **Result** sheet.

References

- DDR Memory Controller IP (FPGA-IPUG-02208)
- DDR3 SDRAM Memory Controller IP Core for Nexus Devices (FPGA-IPUG-02086)
- LPDDR4 Memory Controller IP Core for Nexus Devices (FPGA-IPUG-02127)
- Avant-E Evaluation Board
- Avant-G Versa Board
- Avant-X Versa Board
- CertusPro-NX Versa Board
- CertusPro-NX PCIe Bridge Board
- Certus-NX Versa Evaluation Board
- CrossLink-NX PCIe Bridge Board

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, August 2025

Section	Change Summary
All	Initial release.

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