SLVS-EC to MIPI CSI-2 with CertusPro-NX Devices

Reference Design

FPGA-RD-02251-1.1

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
APB	Advanced Peripheral Bus
AXI4	Advanced eXtensible Interface Version 4
CMOS	Complementary Metal-Oxide-Semiconductor
CRC	Cyclic Redundancy Check
CSI-2	Camera Serial Interface 2
D-PHY	Physical Layer
DPI	Display Pixel Interface
DSI	Display Serial Interface
DT	Data Type
EBR	Embedded Block RAM
ECC	Error Correction Code
EoT	End of Transmission
EoTp	End of Transmission Packet
FF	Flip-Flop
GPLL	General Purpose PLL
HDL	Hardware Description Language
HS	High Speed
IP	Intellectual Property
LSB	Least Significant Bit
LP	Low Power
LUT	Look Up Table
LVDS	Low-Voltage Differential Signaling
LVCMOS	Low-Voltage Complementary Metal-Oxide-Semiconductor
MIPI	Mobile Industry Processor Interface
MSB	Most Significant Bit
P2B	Pixel2Byte
PLL	Phase Locked Loop
PMA	Physical Medium Attachment
RX	Receiver
SLVS-EC	Scalable Low Voltage Signaling with Embedded Clock
TX	Transmitter
VC	Virtual Channel
WC	Word Count

1. Introduction

The Mobile Industry Processor Interface (MIPI®) D-PHY is developed primarily to support camera and display interconnections in mobile devices, and it has become the industry's primary high-speed PHY solution for these applications in smartphones. It is used in conjunction with MIPI camera serial interface-2 (CSI-2) and MIPI display serial interface (DSI) protocol specifications. It meets the demanding requirements of low power, low noise generation, and high noise immunity that mobile phone designs demand.

MIPI D-PHY is a practical PHY for the typical camera, display applications and designed to replace traditional parallel buses based on low-voltage complementary metal-oxide-semiconductor (LVCMOS) or low-voltage differential signaling (LVDS). However, many processors and displays/cameras still use RGB, complementary metal-oxide-semiconductor (CMOS), or MIPI display pixel interface (DPI) as an interface.

The scalable low voltage signaling with embedded clock (SLVS-EC) to MIPI reference design allows the quick interface to receive serial data from CMOS Image Sensors and convert the incoming serial data to MIPI CSI-2 data format. The Lattice Semiconductor SLVS-EC to MIPI D-PHY Interface reference design provides this conversion for Lattice Semiconductor CertusPro™-NX devices. This is useful for wearable, tablet, human-machine interfacing, medical equipment, and many other applications.

The reference design is available on the SLVS-EC to MIPI CSI-2 with CertusPro-NX web page.

1.1. Supported Device and IP

This reference design supports the following devices with IP versions.

Table 1.1. Supported Device and IP

Device Family	Part Number	Compatible IP
CertusPro-NX	LFCPNX-100-9LFG672I	SLVS-EC Receiver IP version 1.2.3 Pixel-to-Byte Converter IP version 1.9.1 D-PHY Transmitter IP version 2.3.0

The IPs above are supported by the Lattice Radiant™ software version 2025.1 or later.

1.2. Features List

The key features of the SLVS-EC to MIPI Reference Design are:

- Compliant with SLVS-EC Protocol specification v2.0
- Back compatibility with SLVS-EC Protocol specification v1.2
- Compliant with MIPI D-PHY v1.2, and MIPI CSI-2 v1.2 Specifications
- Supports MIPI CSI-2 interfacing up to 5 Gb/s for SLVS-EC and 6 Gb/s for Soft TX D-PHY
- Supports 1, 2, or 4 data lanes
- Supports 1, 2, or 4 MIPI TX D-PHY data lanes
- Supports low-power (LP) mode during the vertical and horizontal blanking
- Supports common MIPI CSI-2 compatible video formats (RAW8, RAW10, RAW12, or RAW16)

1.3. Block Diagram

Figure 1.1 shows the block level diagram of the SLVS-EC to MIPI Reference Design.

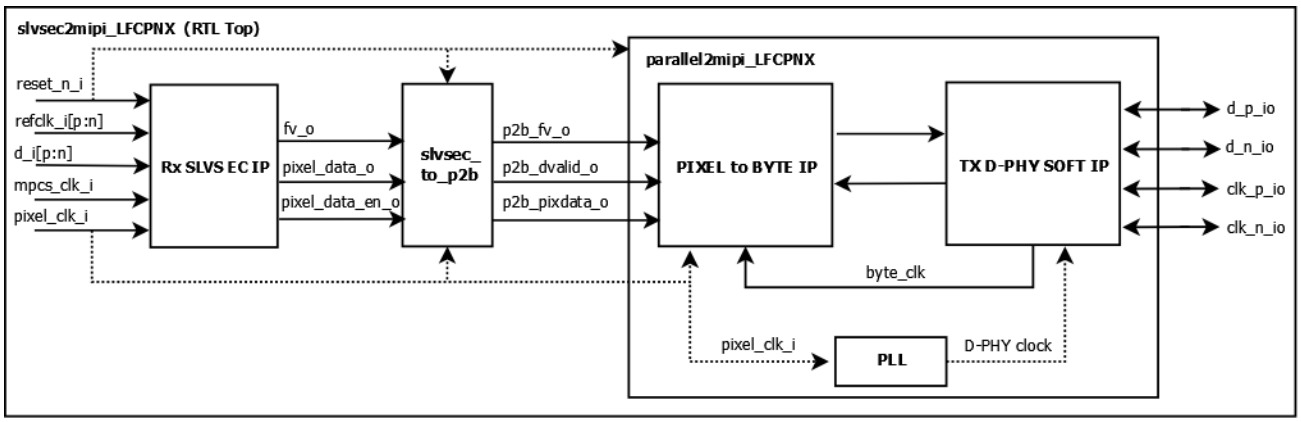

Figure 1.1. SLVS-EC to MIPI Reference Design Block Diagram

As shown in Figure 1.1, the block level diagram of the SLVS-EC to MIPI reference design mainly consists of the SLVS-EC IP, Pixel to Byte IP, and TX D-PHY IP. The pixel data output from SLVS EC IP given is to slvsec_to_p2b module that provides support to feed pixel data to Pixel to Byte IP as per its Byte data output extraction format. In CertusPro-NX devices, TX D-PHY IP uses Soft D-PHY, which requires input clocks that matches with the targeted D-PHY clock frequency, and general purpose PLL (GPLL) used is to create an appropriate TX D-PHY clock frequency.

1.4. Functional Description

The SLVS-EC to MIPI D-PHY Reference Design converts incoming serial video data from the CMOS image sensor back into MIPI CSI-2 serial data format. The SLVS-EC receiver interface consists of two clock lanes and a configurable number of data lanes and as per the configured data type RAW10, provides frame valid, line valid, and parallel pixel data. The design converts this parallel output further from Pixel to byte and transmits the serial data over MIPI D-PHY lanes using TX-DPHY IP.

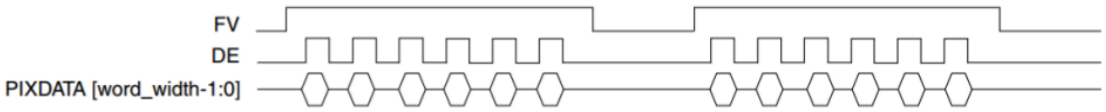

Figure 1.2. Camera Sensor Parallel Input Bus Waveform

This serial bus in Figure 1.2 is converted to the appropriate CSI-2 output format. The CSI-2 output serializes HS (High Speed) data, controls LP (Low Power) data, and transfers them through MIPI D-PHY IP. MIPI D-PHY also has a maximum of 5 lanes per channel. It consists of one clock lane and up to 4 data lanes. The maximum D-PHY data rate per lane is 1.5 Gb/s by TX Soft D-PHY IP.

1.5. Conventions

1.5.1. Nomenclature

The nomenclature used in this document is based on Verilog Hardware Description Language (HDL). This includes radix indications and logical operators.

1.5.2. Data Ordering and Data Types

The highest bit within a data bus is the most significant bit. 10-bit parallel data is serialized to a 1-bit data stream on each MIPI D-PHY data lane where bit 0 is the first transmitted bit.

Table 1.2 lists pixel data order coming from core module.

Table 1.2. Pixel Data Order

Data Type	Format
RAW	RAW [MSB: 0]

1.5.3. Signal Names

Signal names that end with:

- _n are active low
- _i are input signals
  - Some signals are declared as bidirectional (I/O) but are only used as input. Hence, _i identifier is used.
- _o are output signals
  - Some signals are declared as bidirectional (I/O) but are only used as output. Hence, _o identifier is used.
- _io are bidirectional signals

2. Parameters and Port List

There are two directive files for this reference design:

- synthesis_directives.v – used for design synthesis by the Lattice Radiant software and simulation
- simulation_directives.sv – used for simulation

These directives can be modified according to the required configuration. The settings in these files must match SLVS-EC IP, Pixel to Byte IP, and TX D-PHY IP settings created by the Lattice Radiant software.

2.1. Synthesis Directives

Table 2.1 shows the synthesis directives that affect this reference design. They are used for both synthesis and simulation. Some restricted parameter selections are by other parameter settings as shown in Table 2.1 and Table 2.2.

Table 2.1. Synthesis Directives

Category	Directive	Remarks
Number of RX Lane	NUM_RX_LANE_1	Only one of these directives must be selected as per SLVS-EC lanes configuration.
	NUM_RX_LANE_2	
	NUM_RX_LANE_4	
Number of Bits per Pixel lane	BIT_PER_PIXEL {value}	Number of Bits per Pixel lane for SLVS EC, Set value {n} for Raw{n} data type.
Pixel count per line	LINE_LENGTH {value}	Number of pixels count in SLVS-EC, Set to 1920.
Baud Grade	BAUD_GRADE_1	Only one of these directives must be selected as per SLVS-EC baud grade configuration.
	BAUD_GRADE_2	
	BAUD_GRADE_3	
D-PHY Type	TX_CSI2	SLVS-EC supports only CSI-2. Hence, CSI-2 is always used for transmission.
Video Data Type	RAW8	Type of video data to convert from Serial to Pixel for SLVS-EC and from pixel format to byte format for Pixel to Byte converter. Must match with SLVS-EC configuration.
	RAW10	
	RAW12	
	RAW14	
	RAW16	
Number of TX Lane	NUM_TX_LANE_1	Only one of these directives must be selected as per TX DPHY lanes configuration.
	NUM_TX_LANE_2	
	NUM_TX_LANE_4	
Number of Pixels Per Pixel Clock	NUM_PIX_LANE_1	Only one of these four directives must be defined, Number of pixels per pixel clock used for the input to the Pixel to Byte converter.
	NUM_PIX_LANE_2	
	NUM_PIX_LANE_4	
TX D-PHY Clock Gear	TX_GEAR_8	TX D-PHY Clock Gear is always Gear 8.
Miscellaneous	TX_CSI2	Enables internal signals monitored by test-bench. Always ON.
Number of Pixels	NUM_PIXELS {value}	Number of active Pixels per Line, set to 1920.
Clock Mode	TX_CLK_MODE_HS_ONLY	TX D-PHY Clock mode, only one of these two directives must be defined.
	TX_CLK_MODE_HS_LP	
Use GPLL	USE_GPLL	Always defined to generate D-PHY clock frequency for TX D-PHY.

Note: HS_LP mode means *non-continuous clock mode* and HS_ONLY means *continuous clock mode* for the TX D-PHY.

2.2. Simulation Directives

Table 2.2 shows the simulation directives for this reference design.

Table 2.2. Simulation Directives

Category	Directive	Remarks
Pixel clock period	PIX_CLK {value}	Pixel clock period in ns
Number of video frames	NUM_FRAMES {value}	Number of video frames to be transmitted
Number of lines per frame	NUM_LINES {value}	Number of active lines per frame
Horizontal Front Porch	HFRONT {value}	Number of blanking cycles before HSYNC signal is asserted
Horizontal Back Porch	HBACK {value}	Number of blanking cycles after HSYNC signal is de-asserted
Vertical Front Porch	VFRONT {value}	Number of blanking lines before VSYNC signal is asserted
Vertical Back Porch	VBACK {value}	Number of blanking lines after VSYNC signal is de-asserted

2.3. Top-Level I/O

Table 2.3 shows the top-level I/O of this reference design. Actual I/O depends on your configurations and compiler directives automatically declare all necessary I/O ports.

Table 2.3. SLVS-EC to MIPI Top Level I/O

Port Name	Direction	Description
Clocks and Reset		
pixel_clk_i[1]	I	Pixel clock input.
reset_n_i	I	Active low asynchronous reset.
refclk_p_i	I	Differential Reference Clock, CLK+.
refclk_n_i	I	Differential Reference Clock, CLK-.
mpcs_clkin_i	I	Clock source for physical medium attachment (PMA) in SLVS-EC IP, use 125 MHz.
mpcs_pwrdn_i	I	PHY power down. 2'b00: Operational. 2'b10: Low-power state. Rx CDRPLL is powered-down. The PHY starts in this low-power mode to perform calibration. 2'b11: Deep low-power state. TX driver is in electrical Idle II (static low). All PLLs are powered down and clock shutdown.
Primary I/O		
d_p_i	I	Differential Reference Clock, CLK+.
d_n_i	I	Differential Reference Clock, CLK-.
setup_i	I	Active high setup signal from Client-side interface to commence start-up for SLVS-EC.
APB Interface		
apb_pclk_i	I	APB clock, Use 125 MHz.
apb_preset_n_i	I	APB active low reset.
apb_paddr_i	I	Address signal.
apb_psel_i	I	Select signal. This indicates that the completer device is selected and a data transfer is required.
apb_penable_i	I	Enable signal. Indicates the second and subsequent cycles of an APB transfer.
apb_pwdata_i	I	Write data signal.
apb_pwrite_i	I	Direction signal, Write = 1, Read = 0.
apb_pready_o	O	Ready signal shows transfer completion. The completer uses this signal to extend an APB transfer.
apb_prdata_o	O	Read data signal.
MIPI DPHY TX Interface		
d_p_io[NUM_TX_LANE -1:0][2]	I/O	Positive differential TX D-PHY data lanes.
d_n_io[NUM_TX_LANE -1:0][2]	I/O	Negative differential TX D-PHY data lanes.
clk_p_io	I/O	Positive differential TX D-PHY clock lane.

Port Name	Direction	Description
clk_n_io	I/O	Negative differential TX D-PHY clock lane.
Miscellaneous		
pll_lock_o	O	GPLL lock output.

Notes:

1. Available only if Native interface is enabled in SLVS-EC IP
2. NUM_TX_LANE = Number of TX D-PHY Lanes: 1, 2, 4 (available on user interface)

3. Design and Module Description

The top-level design (slvsec2mipi_LFCPNX.v) consists of the following modules:

- rx_slvs_ec
- slvsec_to_p2b
- p2b
- tx_dphy
- int_pll

The design uses external PLL support on defining USE_GPLL according to Soft TX D-PHY configuration.

Figure 3.1 shows the timing diagram for the D-PHY TX Input Bus for Long Packet Transmission in CSI-2 Interface.

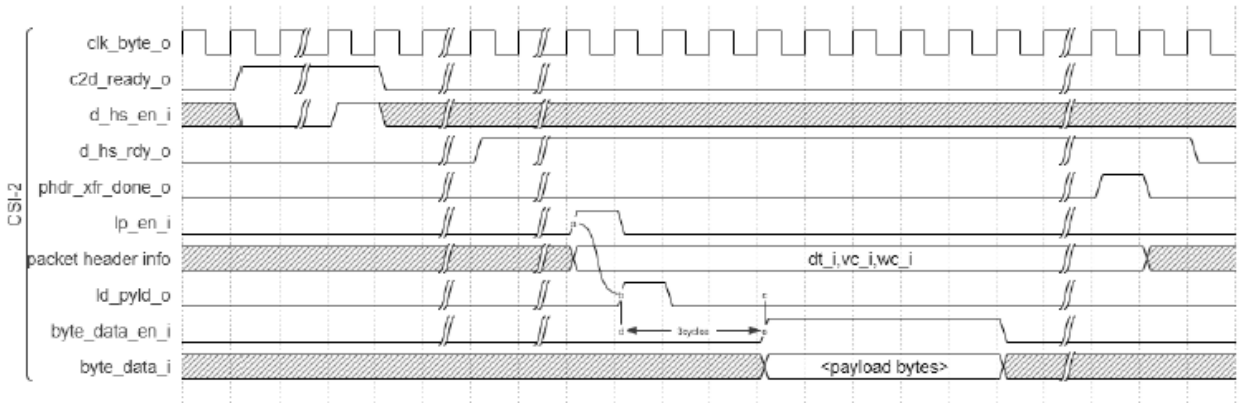

Figure 3.1. D-PHY Tx Input Bus for Long Packet Transmission in CSI-2 Interface

When the protocol type ‘CSI-2’ selected, there is no internal buffer to save the incoming payload data before the creation of the header packet. Because of this, the D-PHY TX IP requires 3 cycles from the assertion of the ld_pyld_o to the arrival of the valid payload data. The ld_pyld_o asserts the next cycle after the detection of the lp_en_i. Hence, little glue logic is added in the top-level design to take care of this timing requirement for the required signals for the D-PHY TX IP as shown in Figure 3.1.

3.1. rx_slvs_ec

Create this module to receive serial data from the CMOS image sensor and convert it into parallel pixel data output according to configurations, such as RX lanes, Data Type, Baud grade, and others. Figure 3.2 shows an example of IP GUI interface settings in the Lattice Radiant software for the RX SLVS-EC IP. Refer to the SLVS-EC Receiver IP User Guide (FPGA-IPUG-02125) for details.

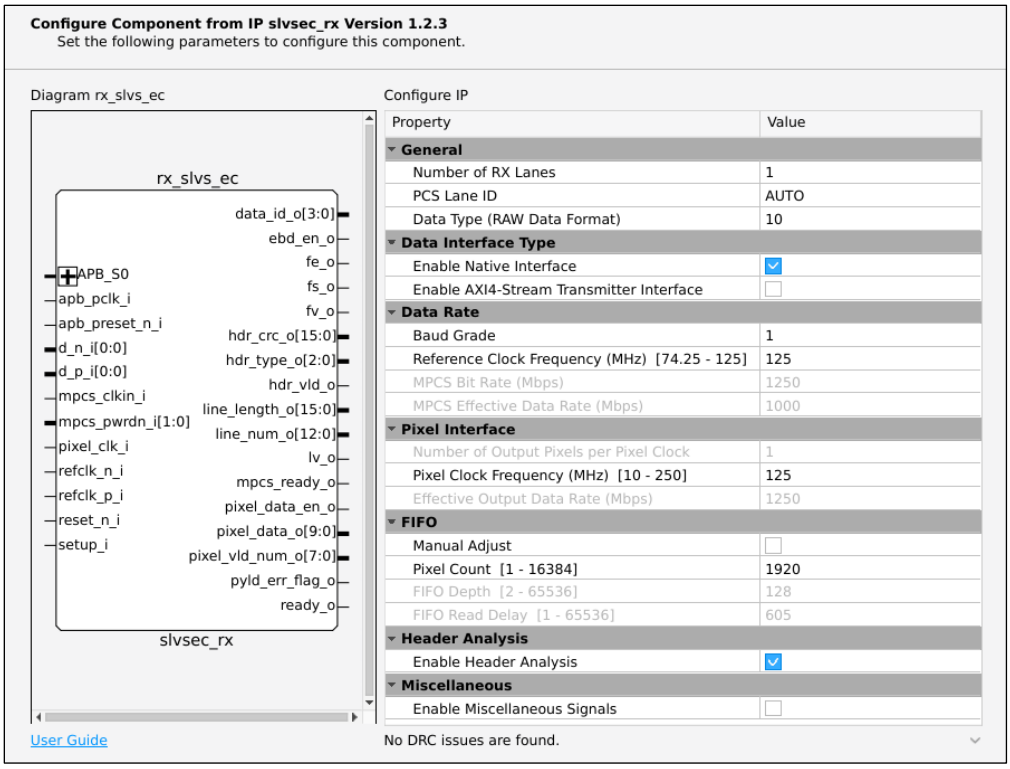

Figure 3.2. rx_slvs_ec IP Creation in Lattice Radiant Software

The following shows the guidelines and the required parameter settings for this reference design:

- Number of RX Lanes – Select 1,2,4,6 or 8 as per configuration.
- PCS Lane ID – Always use AUTO.
- Data Type – Select as 8,10,12,14 or 16 as per configuration. These indicate RAW data types.
- Enable Native Interface – Always enabled (checked).
- Enable AXI4-Stream Transmitter Interface – Always disabled (unchecked).
- Baud grade – Select as 1,2 or 3 as per configuration.
- Pixel Clock Frequency – Recommended by IP is always 125 MHz. Value changes as per Baud grade selection.
- Pixel count – Set as 1920.
- Enable Header Analysis – Always enabled (checked).
- Enable Miscellaneous signals – Always disabled (unchecked).

Note: RXSLVS-EC IP supports only MIPI CSI-2 DPHY type data transfer. Hence, the D-PHY interface type in Pixel to Byte and TX D-PHY IPs also should be always set as CSI-2 only.

The .ipx file is included in the projects (rx_slvs_ec/rx_slvs_ec.ipx) to reconfigure the IP as per the user configuration requirements. If this IP is required to create from scratch, recommended is to set the design name to *rx_slvs_ec* so that it is not required to modify the instance name of this IP in the top-level design as well in the simulation setup file.

3.2. p2b

Create this module to convert Pixel data into Byte data output according to configurations, such as TX Interface, Data Type, number of TX Lanes, and others. Figure 3.3 shows an example of IP GUI interface settings in the Lattice Radiant software for the Pixel to Byte IP. Refer to the Pixel-to-Byte Converter IP User Guide (FPGA-IPUG-02094) for details.

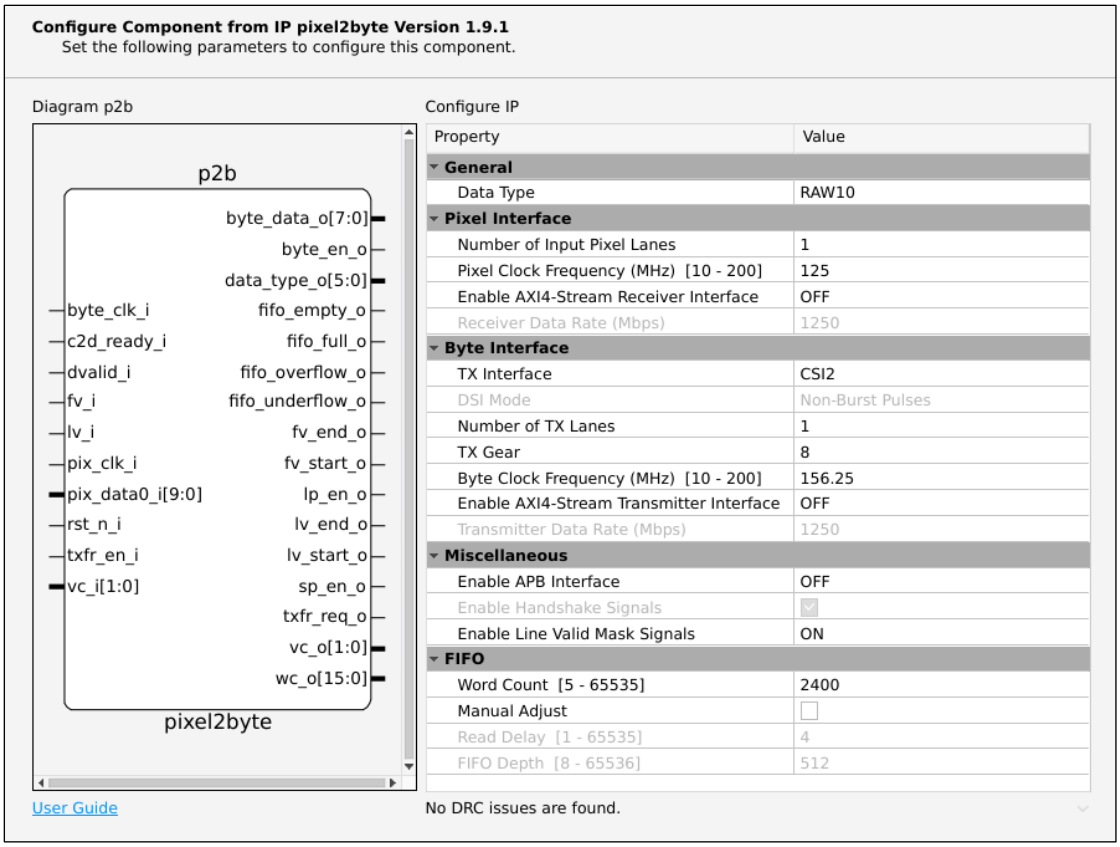

Figure 3.3. p2b IP Creation in Lattice Radiant Software

The following shows the guidelines and the required parameter settings for this reference design:

- TX Interface – Always select CSI-2.
- Data Type – Select RAW8, RAW10, RAW12, or RAW16 for CSI-2, others are not supported in this reference design.
- Number of TX Lanes – Select 1, 2, or 4. Set the same value as TX D-PHY IP.
- Number of Input Pixel Lanes – Match the configuration with the rx_slvs_ec *Number of output pixel per clock*.
- TX Gear – Always select 8.
- Word Count – Must be set according to the number of pixels per line and number of bits per pixel. The equation is NUM_PIXELS × BITS_PER_PIXEL / 8.
- Manual Adjust – Unselect the checkbox.
- Enable miscellaneous status signals – Select the checkbox to enable (checked).

The Pixel-to-Byte Converter IP converts the standard pixel data format to the D-PHY CSI-2 standard-based byte data stream. The .ipx file is included in the projects (p2b/p2b.ipx) to reconfigure the IP as per the user configuration requirements. If this IP is required to create from scratch, recommended is to set the design name to *p2b* so that it is not required to modify the instance name of this IP in the top-level design as well as in the simulation setup file.

3.3. slvsec_to_p2b

This module works as a bridge between SLVS EC IP and Pixel to Byte IP to avoid any data mismatch in the design. The design assumes that the packetized input byte data from the SLVS-EC sensor is sent without change over the MIPI DPHY transmitter. The SLVS-EC Receiver IP unpacks the byte data into pixel data differently compared to the Pixel-to-Byte Converter IP, thus we need to remap them accordingly. The Pixel-to-Byte Converter IP are packetizing the pixel data into the byte data format according the defined MIPI CSI-2 specification. The remapping is only required for the data types that are not byte-aligned. For example, 1 pixel does not correspond to a multiple of 8 bits.

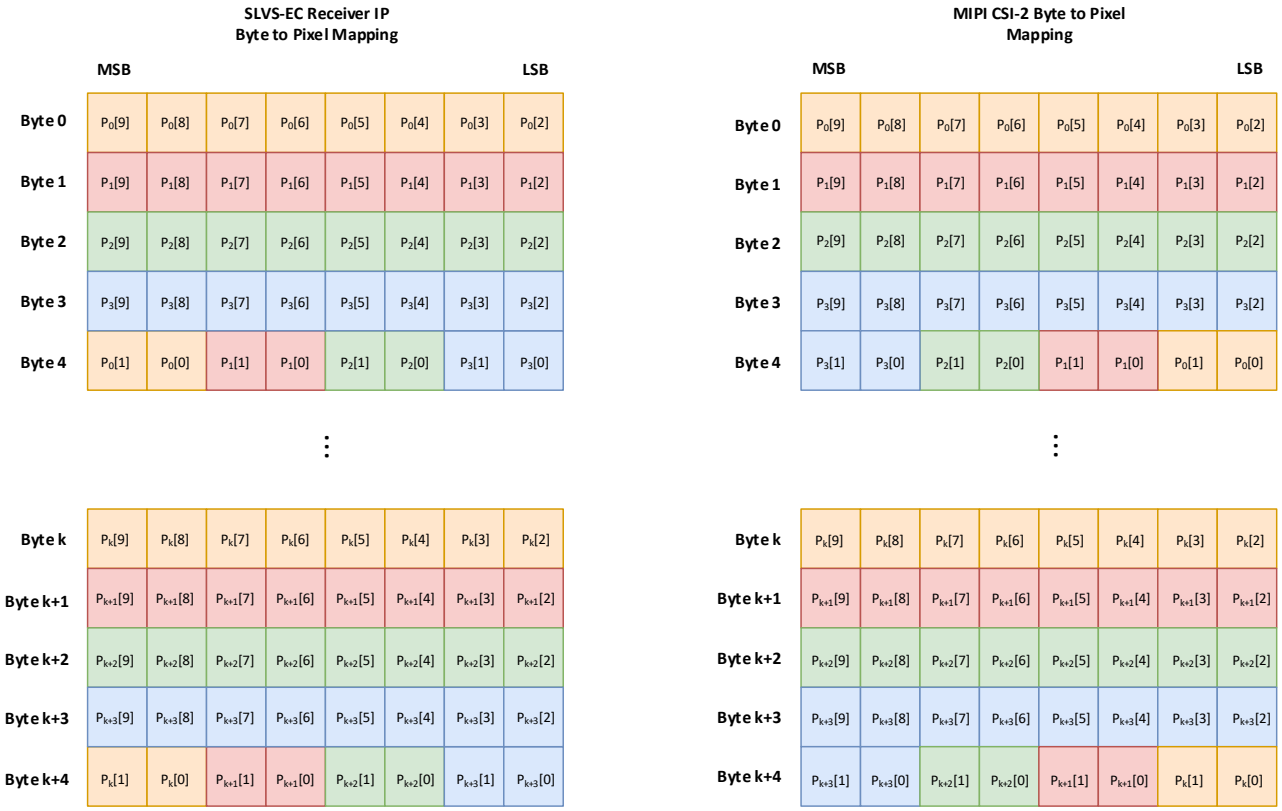

Figure 3.4. RAW10 Byte to Pixel Mapping

Figure 3.4 shows the RAW10 byte to pixel mapping. In the RAW10 format, pixel data is distributed across bytes in groups of five. The first four bytes in each group (Byte 0 to Byte 3) are mapped identically between the SLVS-EC Receiver IP output and MIPI CSI-2 protocols, each carrying the 8 most significant bits (MSBs) of four consecutive pixels. However, the fifth byte (Byte 4) in each group contains the 2 least significant bits (LSBs) of those four pixels, and this is where the two protocols differ. The bit arrangement within Byte 4 varies between the SLVS-EC Receiver IP and MIPI CSI-2, requiring a bit-level rearrangement.

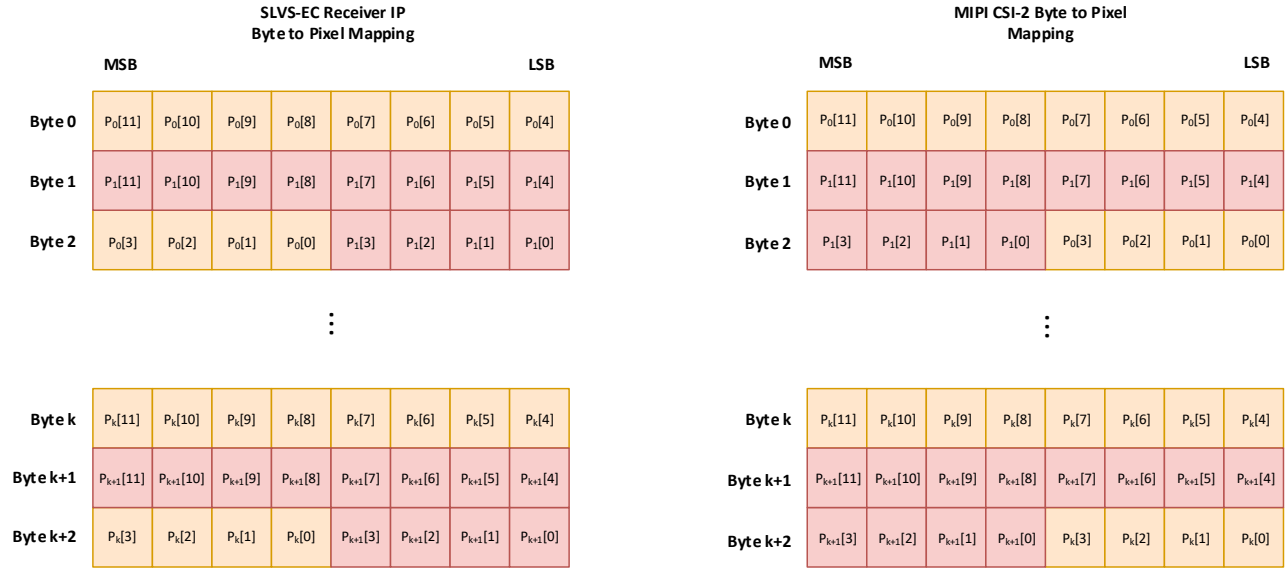

Figure 3.5. RAW12 Byte to Pixel Mapping

Figure 3.5 shows the RAW12 byte to pixel mapping. In the RAW12 format, each pixel is represented using 12 bits, which are split across multiple bytes. The mapping of these bytes is largely consistent between the SLVS-EC Receiver IP and MIPI CSI-2 protocols for the first two bytes in each 3-byte group. These bytes carry the upper 8 bits (P[11:4]) of each pixel and are aligned similarly in both the SLVS-EC Receiver IP output and MIPI CSI-2 protocol. However, the third byte in each group (every third byte) contains the remaining 4 least significant bits (P[3:0]) of multiple pixels. This byte is formatted differently between the SLVS-EC Receiver IP and MIPI CSI-2, requiring a bit-level rearrangement.

This module performs pixel generation for all supported combinations of this reference design as shown in the Known Limitations section.

3.4. tx_dphy

Create this module according to the channel conditions, such as the number of lanes, bandwidth, and others. Figure 3.6 shows an example IP GUI interface setting in the Lattice Radiant software for the CSI-2 D-PHY Transmitter IP. Refer to the CSI-2/DSI D-PHY Tx IP User Guide (FPGA-IPUG-02080) for details.

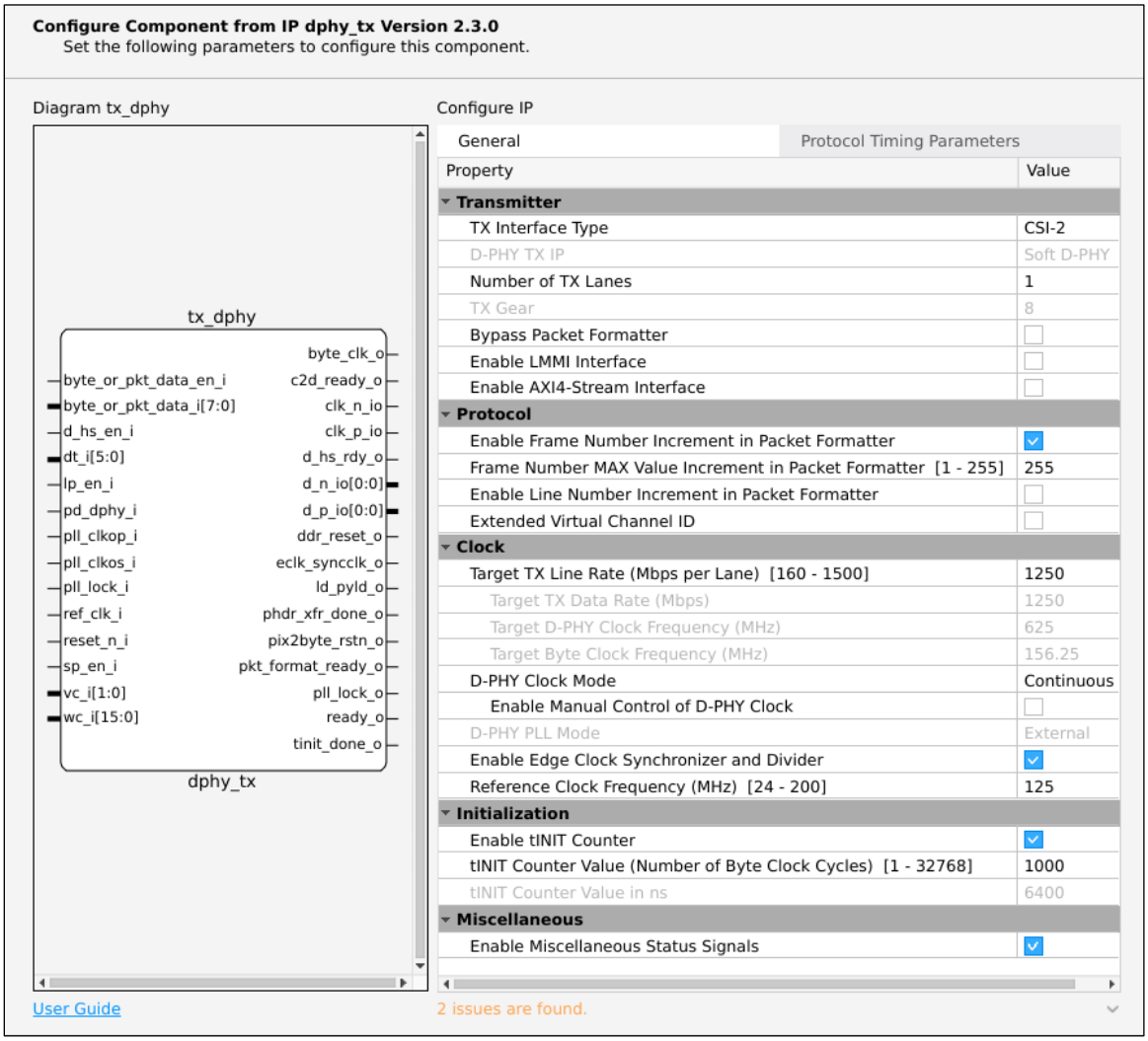

Figure 3.6. tx_dphy IP Creation in Lattice Radiant Software

The following shows the guidelines and required parameter settings for this reference design:

- TX Interface Type – Always select CSI-2.
- D-PHY TX IP – CertusPro-NX by default supports only Soft DPHY type.
- Number of TX Lanes – Select 1, 2, or 4 according to the required configuration.

- TX Gear – Always 8, since the D-PHY type supported by the device is Soft D-PHY only. The Lattice Radiant software automatically selects TX Gear 8 when the lane bandwidth is less than 1500 Mbps, which means the TX byte clock could be ~187.5 MHz.
- Bypass Packet Formatter – Always disabled (unchecked).
- Enable Frame Number Increment in Packet Formatter – Select checkbox to enable (checked), only for CSI-2.
- Frame Number MAX Value Increment in Packet Formatter [1 - 255] – Numerical value between 1 to 255, only for CSI-2.
- Enable Line Number Increment in Packet Formatter – Select checkbox to enable (checked), only for CSI-2.
- Enable LMMI Interface – Always disabled (unchecked).
- Enable AXI4-Stream Interface – Always disabled (unchecked).
- TX Line Rate per Lane (Mbps) [160 – 1500] (Soft D-PHY) – Set according to the required configuration.
- D-PHY Clock Mode – Set Continuous or Non-continuous according to the required configuration.
- Reference Clock Frequency (MHz) [24 – 200] – Set the same value as pixel clock frequency.
- tINIT Counter – Always enabled (checked) and use 1000 as the counter value.
- Enable Miscellaneous Status Signals – Always enable (checked).

The default values are recommended in the Protocol Timing Parameters window of this IP. This module takes the byte data and outputs CSI-2 data after serialization in CSI-2 High-Speed mode. The .ipx file is included in the project (tx_dphy/tx_dphy.ipx) to reconfigure the IP as per the user configuration requirements. If this IP is required to create from scratch, it recommended is to set the design name to *tx_dphy* so that it is not required to modify the instance name of this IP in the top-level design as well as a simulation setup file.

3.5. int_pll

Create this module to generate the required TX D-PHY clock frequency (clkop_o) for Soft TX D-PHY IP as per the equation mentioned below. Figure 3.7 shows an example IP GUI interface setting in the Lattice Radiant software for the PLL IP. Refer to the PLL Module User Guide (FPGA-IPUG-02063) for details.

TX D-PHY clock frequency = (TX D-PHY Line rate / 2) MHz

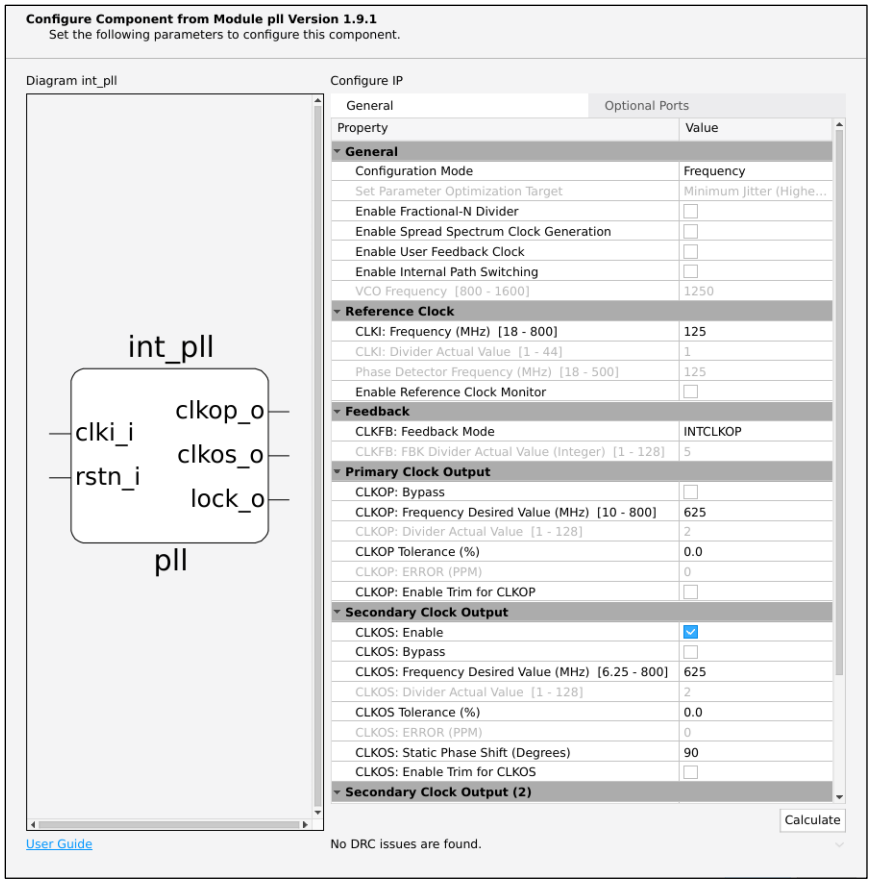

Figure 3.7. int_pll IP Creation in Lattice Radiant Software

Modify the reference clock, clkop_o, and clkos_o frequency as per the required configurations. clkop_o frequency needs to be the same as *Target D-PHY Clock Frequency* of the tx_dphy IP with 0-degree phase shift, while clkos_o frequency needs to be the same as *Target D-PHY Clock Frequency* of the tx_dphy IP with 90-degree phase shift. The .ipx file is included in this project (int_pll/int_pll.ipx) to reconfigure the IP as per the user configuration requirements. If this IP is required to create from scratch, recommended is to set the design name to int_pll so that it is not required to modify the instance names of IPs in the top-design file.

4. Design and File Modifications

This reference design uses SLVS EC IP v1.2.3, Pixel2Byte IP v1.9.1, and TX D-PHY IP v2.3.0. Some modifications are required depending on user configuration in addition to two directive files (synthesis_directives.v and simulation_directives.v).

4.1. Top-level RTL

The current top-level file (slvsec2mipi_LFCPNX.v) integrates all the above-mentioned design IPs required for this reference design. The GPLL setting in the current sub-level file (parallel2mipi_LFCPNX.v) corresponds to the configuration selected for this reference design. According to the configuration, modify the GPLL instantiation as described in the int_pll section. In addition, modify the instance names of RX SLVS-EC (rx_slvs_ec), Pixel to Byte (p2b), TX D-PHY (tx_dphy) and internal GPLL (int_pll) if this IP(s) is created with different name(s).

5. Design Simulation

The script file (sim/run_sim.do) and testbench folder are provided to run the functional simulation using QuestaSim. Follow the naming recommendations regarding design name and instance name when the required IPs are created by the Lattice Radiant software. To run the simulation, follow these steps:

1. Launch QuestaSim using the Lattice Radiant software.
2. Execute the following command in the QuestaSim terminal:

```
cd ../sim
source run_sim.do
```

Modify the simulation_directives.v according to the required configuration (refer to Simulation Directives for details). By executing the script in QuestaSim, compilation and simulation execute automatically. The test-bench slvsec2mipi_LFCPNX_tb.v instantiates the top-level design module, generates the stimulus video data, and does the data comparison between the expected data and output data from the RD, including Frame Number, EoT Packet check, CRC check, EoTp (Long Packet and Short Packet), ECC, and timing parameters of TX D-PHY. Figure 5.1 shows the following statements when the simulation is completed.

```
#    Time: 659982 ns  Iteration: 0  Instance: /slvsec2mipi_LFCPNX_tb
#              659982   ---------------------------------------------
#              659982   ##### DATA COMPARING IS STARTED #####
#              659982   ---------------------------------------------
#              659982   ***PASS : EOT PACKET CHECK***
#              659982   ***PASS : SYNC CHECK
#              659982   ***PASS : ECC
#              659982   ***PASS : FRAME NO
#              659982   ***PASS : CRC***
#              659982   Test fail count : 0
#
#              659982  ------------------------------------------------------
#              659982  ----------------- SIMULATION PASSED -----------------
#              659982  ------------------------------------------------------
#              664982   TEST END
#
#
# ========================================
# Simulation Done
# ========================================
```

Figure 5.1. Simulation Done Statement

The test-bench generates other debug files during simulation like *input_data.log*, *output_data.log,* and *dphy_checker_timing.log* for debugging purposes. The *input_data.log* file stores the data transmitted by the test-bench to RX SLVS-EC. The *output_data.log* file stores the data received to the test bench from TX D-PHY. The testbench compares both of these files. The *dphy_checker_timing.log* file stores all the timing parameters (such as LP-11, TLPX, HS-prepare, HS-0, and HS-Trail) and gives an error if any timing parameter fails. The same file also saves timing of Header Packet received and Header Packet values like DT, VC, WC, and ECC.

Figure 5.2 shows the SLVS EC simulation waveform of the full view of two lines and two frames for the CSI-2 interface. Figure 5.3 shows the zoom view of the simulation waveform shown in Figure 5.2 for the CSI-2 interface.

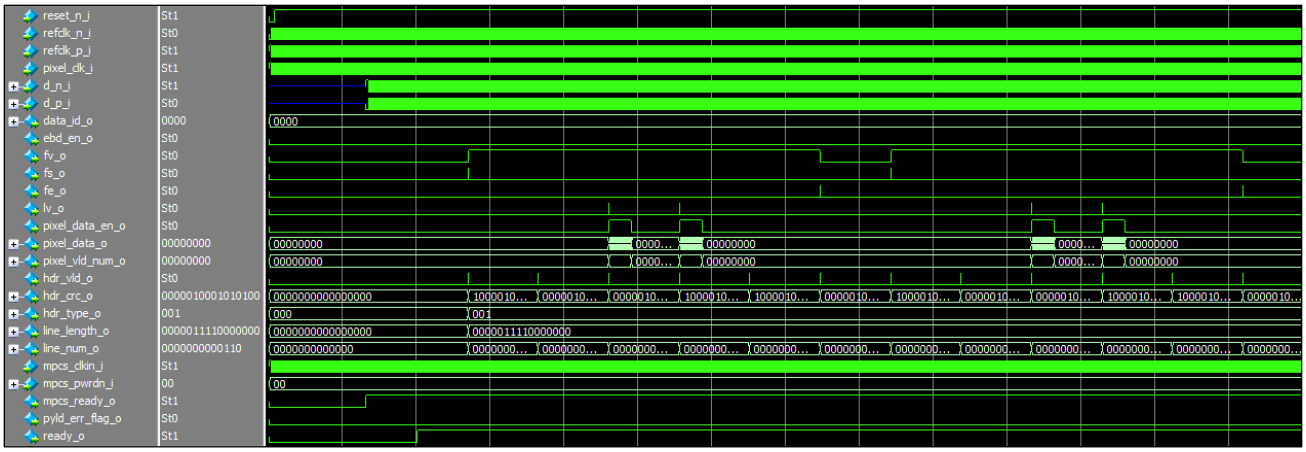

Figure 5.2. Simulation Waveform for CSI-2 (1/2)

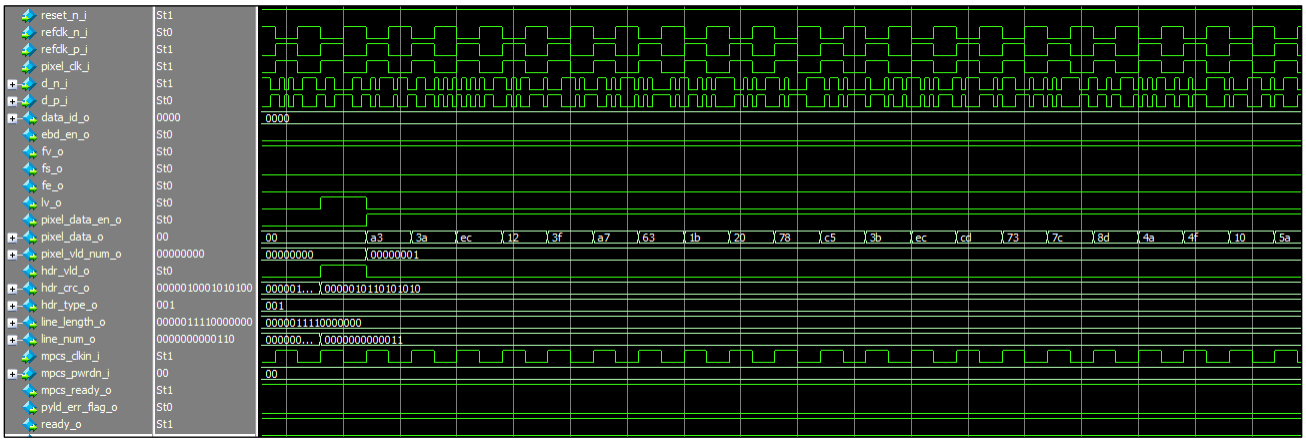

Figure 5.3. Simulation Waveform for CSI-2 (2/2)

The simulation waveform can be by opening the vsim.wlf file in the QuestaSim from the simulation directory. More signals can be added from different modules to the waveform as required.

6. Known Limitations

The following are the limitations of this reference design:

- For RAW10 and RAW12, the SLVS-EC Receiver IP maps pixel LSBs differently from the standard MIPI CSI-2 format. This design assumes identical byte-formatted pixel data between SLVS-EC and MIPI DPHY, hence a remapping module is included.
- RX SLVS-EC supports only the MIPI CSI-2 D-PHY interface.

Table 6.1 shows the combinations of RX SLVS-EC data type and pixel per clock supported by this design.

Table 6.1. Combinations of RX SLVS EC Data Type

Data type	Pixel Per Clock
RAW8	1, 2, 4
RAW10	1, 2, 4
RAW12	1, 2
RAW16	1

7. Design Package and Project Setup

Figure 7.1 shows the directory structure. The targeted design is for LFCPNX-100-7LFG672I. synthesis_directives.v and simulation_directives.v are set to configure the design with the following configuration:

- RX : CSI-2, 1-lane, RAW10 with 1 pixel/clock
- TX: CSI-2, 1-lane, Gear 8 with Soft D-PHY in continuous clock mode

```
├── radiant                  # Contains Lattice Radiant project files
│   └── src
│       ├── constraints      # Contains physical design constrains (.pdc) file
│       ├── ip               # Contains generated IPs from Lattice Radiant
│       │   ├── int_pll
│       │   ├── p2b
│       │   ├── rx_slvs_ec
│       │   └── tx_dphy
│       ├── rtl              # Contains the RTLs used in the reference design
│       └── testbench        # Contains testbench files used in the reference design
└── sim                      # Contains QuestaSim .do file for RTL simulation
```

Figure 7.1. Directory Structure

Figure 7.2 shows the design files used in the Lattice Radiant project. Including PLL, the Lattice Radiant software creates four .ipx files. By specifying slvsec2mipi_LFCPNX as a top-level design, the tool ignores all unnecessary files. Constraint file (slvsec_to_mipi_LFCPNX.pdc) is also included in the project for reference.

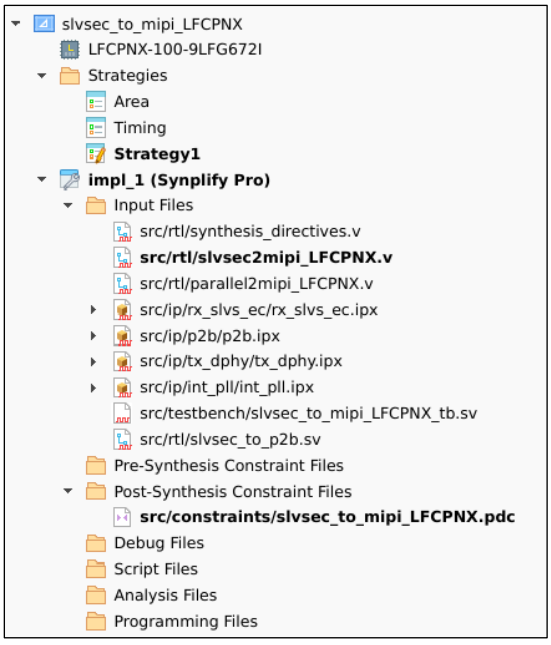

Figure 7.2. Project Files

8. Resource Utilization

Resource utilization depends on the configuration used. Table 8.1 shows resource utilization examples under certain configurations targeting LFCPNX-100. This is just a reference and actual usage varies.

Table 8.1. Resource Utilization Examples

Configuration	LUT (Utilization/Total)	FF (Utilization/Total)	EBR (Utilization/Total)
RAW10, 1 SLVS-EC Rx lane, 1 Pixel/clock, Baud grade 1, 1 MIPI D-PHY Tx lane	4460/79872	2199/79872	3/208
RAW10, 1 SLVS-EC Rx lane, 4 Pixel/clock, Baud grade 3, 4 MIPI D-PHY Tx lane	6749/79872	3655/79872	10/208
RAW16, 1 SLVS-EC Rx lane, 1 Pixel/clock, Baud grade 1, 4 MIPI D-PHY Tx lane	4823/79872	2606/79872	12/208
RAW8, 4 SLVS-EC Rx lane, 1 Pixel/clock, Baud grade 1, 4 MIPI D-PHY Tx lane	9263/79872	4311/79872	9/208
RAW10, 1 SLVS-EC Rx lane, 2 Pixel/clock, Baud grade 2, 2 MIPI D-PHY Tx lane	5628/79872	2717/79872	6/208
RAW12, 1 SLVS-EC Rx lane, 1 Pixel/clock, Baud grade 1, 1 MIPI D-PHY Tx lane	4411/79872	2193/79872	5/208
RAW12, 2 SLVS-EC Rx lane, 2 Pixel/clock, Baud grade 1, 2 MIPI D-PHY Tx lane	6477/79872	3023/79872	6/208

References

- MIPI Alliance web page for D-PHY Version 1.2 and Camera Serial Interface 2 (CSI-2) Version 1.2
- SLVS-EC Receiver IP User Guide (FPGA-IPUG-02125)
- Pixel-to-Byte Converter IP User Guide (FPGA-IPUG-02094)
- CSI-2/DSI D-PHY Tx IP User Guide (FPGA-IPUG-02080)
- PLL Module User Guide (FPGA-IPUG-02063)
- SLVS-EC to MIPI CSI-2 with CertusPro-NX web page
- CertusPro-NX web page
- Lattice Radiant Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.1, July 2025

Section	Change Summary
All	• Renamed document from SLVS EC to MIPI CSI-2 with CertusPro-NX to SLVS-EC to MIPI CSI-2 with CertusPro-NX Devices. • Changed instances of *slave* to *completer*. • Performed minor formatting and editorial edits.
Disclaimers	Updated disclaimers.
Inclusive Language	Added inclusive language boilerplate.
Acronyms in This Document	Added definition for APB, AXI4, CMOS, DPI, EoT, EoTp, FF, HDL, LSB, LVDS, LVCMOS, and PMA.
Supported Device and IP	Updated device part number and IP and software versions, and moved to section 1.1 Supported Device and IP.
Introduction	• Added the link to the reference design in the Introduction section. • Added the Supported Device and IP section. • Updated data lanes and common MIPI CSI-2 compatible video formats support in the Features List section. • Updated the description on the TX D-PHY IP in the Block Diagram section.
Parameters and Port List	• Updated the simulation_directives.sv in the Parameters and Port List section. • Updated *Baud Grade*, *Video Data Type* and *Number of Pixels Per Pixel Clock* in Table 2.1. Synthesis Directives.

Design and Module Description	• Updated the following figures:
	  • Figure 3.2. rx_slvs_ec IP Creation in Lattice Radiant Software
	  • Figure 3.3. p2b IP Creation in Lattice Radiant Software
	  • Figure 3.6. tx_dphy IP Creation in Lattice Radiant Software
	  • Figure 3.7. int_pll IP Creation in Lattice Radiant Software
	• Updated the rx_slvs_ec section as follows:
	  • Corrected the reference.
	  • Replaced *Enable AXI4-Stream Transmitter Interface* with *Enable AXI4-Stream Transmitter Interface*.
	• Updated the p2b section as follows:
	  • Updated the *Data Type* and *Number of Input Pixel Lanes* parameters.
	  • Added the *Word Count* and *Manual Adjust* parameters.
	• Updated the slvsec_to_p2b section.
	• Updated the tx_dphy section as follows:
	  • Removed figure: *tx_dphy IP Creation in Lattice Radiant (2/2)*.
	  • Updated the description of *tINIT Counter*.
	• Added description on clkop_o and clkos_o frequency in the int_pll section.

Design and File Modifications	Updated the IP versions in the Design and File Modifications section.

Design Simulation	• Updated the script file path.
	• Changed ModelSim to QuestaSim.
	• Updated the steps to run the simulation.
	• Removed the following figures:
	  • *Script Modification #1*
	  • *Script Modification #2*

Known Limitations	• Added limitations for RAW10 and RAW12 data types. • Updated Table 6.1. Combinations of RX SLVS EC Data Type.

Design Package and Project Setup	• Updated the configuration example for RX and TX.
	• Updated the following figures:
	  • Figure 7.1. Directory Structure
	  • Figure 7.2. Project Files

Section	Change Summary
Resource Utilization	Updated section.
References	Updated references.
Technical Support Assistance	Added link to the Lattice Answer Database.

Revision 1.0, March 2022

Section	Change Summary
All	Initial release.

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