User Manual
Motion Control Board

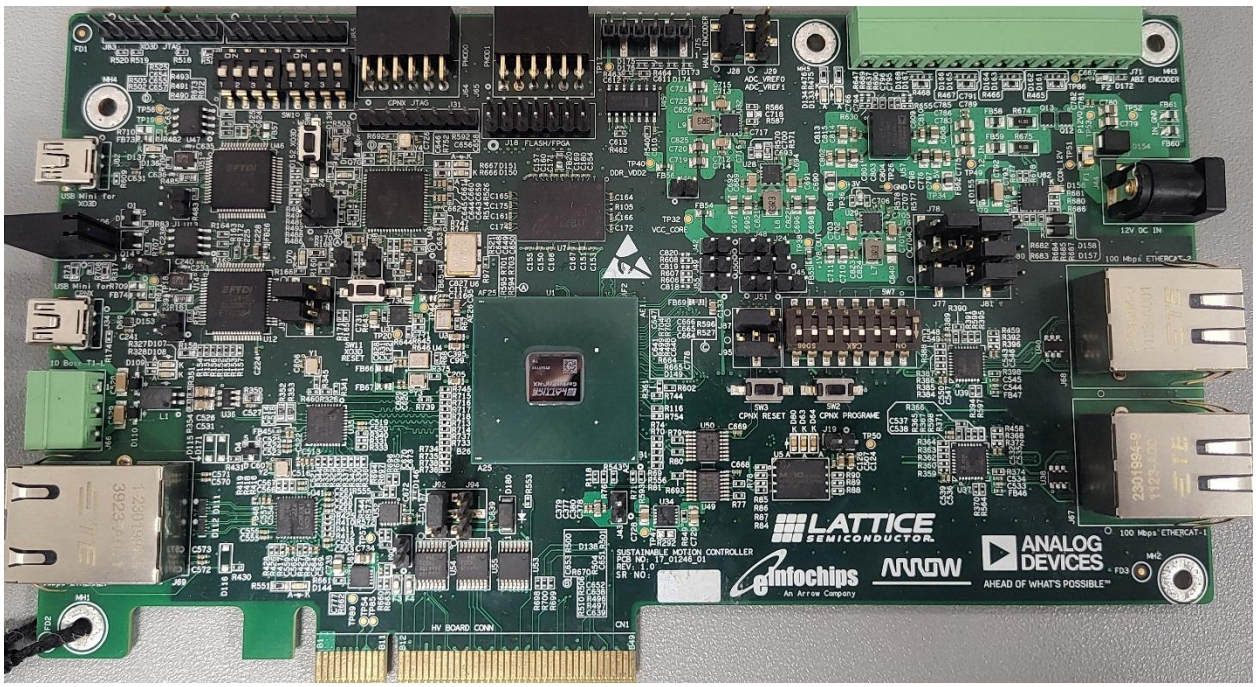

Figure 1 Motion Control Board

Version	1.0
Status	Baseline
Date	15-Oct-2024

Confidentiality Notice

CONTENTS

FIGURES

TABLES

1 DOCUMENTATION DETAILS

1.1 Document History

Version	Author		Reviewer		Approver	
	Name	**Date (DD-MM-YYYY)**	**Name**	**Date (DD-MMM-YYYY)**	**Name**	**Date (DD-MM-YYYY)**
Draft 0.1	Shrey Bechara	31-Jan-24	Ziyauddin Dhukka	3-March-24	Ashish Agarwal	01-Oct-24
Baseline 1.0	Ziyauddin Dhukka	15-Oct-24	Ashish Agarwal	15-Oct-24	Kalpesh Balar	16-Oct-24

Version	Description of Change
Draft 0.1	Initial draft version created.
Baseline 1.0	Internal reviewed and approved.

Table 1: Document History

1.2 Definition, Acronyms and Abbreviations

Definition/Acronym/Abbreviation	Description
AC/DC	Alternating Current and Direct Current
ADC	Analog Digital Converter
caBGA	Chip Array Ball Grid Array
CMOS	Complementary Metal-Oxide Semiconductor
CSI	Camera Serial Interface
DDR	Double Data Rate
DRAM	Dynamic Random Access Memory
DIP	Dual Inline Package
ESD	Electro Static Discharge
FD-SOI	Fully Depleted Silicon On Insulator
FPGA	Field Programmable Logic Array
FTDI	Future Technology Devices International
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LPDDR	Low Power Double Data Rate
LVDS	Low-Voltage Differential Signaling
MIPI	Mobile Industry Processor Interface
PC	Personal Computer
PCIe	Peripheral Component Interconnect Express
PHY	Physical Layer Device
PMOD	Peripheral Module
RGMII	Reduced Gigabit Media Independent Interface
SerDes	Serializer/Deserializer
SFP	Small Form-Factor Pluggable Transceiver
SGMII	Serial Gigabit Media Independent Interface
SMA	Sub-Miniature A Connector
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus

Table 2: Definition, Acronyms and Abbreviations

1.3 References

No.	Document	Version	Remarks
1	Versa board user manual	FPGA-EB-02053-1.2	

Table 3: References

2 INTRODUCTION

Motion Control Board based on Lattice CertusPro-NX with ADI PHYs allows designers to investigate and experiment with the features of the CertusPro-NX Field Programmable Gate Array (FPGA) and motor control features. The features of the Motion Control Board can assist engineers with the rapid prototyping and testing of their specific designs. This guide is intended to be referenced to demonstrate the Motion Control Board based on Lattice CertusPro-NX with ADI PHY and introduce board resources.

2.1 Motion Control Board

The Motion Control Board based on Lattice CertusPro-NX with ADI PHYs features the CertusPro-NX FPGA in the LFG672 package which is built on Lattice Nexus™ FPGA platform using low power 28 nm FD-SOI technology. The board has the ability to expand the usability of the CertusPro-NX FPGA with 3xRJ45, 1xPCI connector, 2xPMOD connectors, ADI PHYs such as 1xADIN1100 over RGMII, 2xADIN1200 over MII, 1xADIN1300 over RGMII interface. Easy-to-use board resources of the jumper, LED indicator, push button and switch are available for user-defined applications.

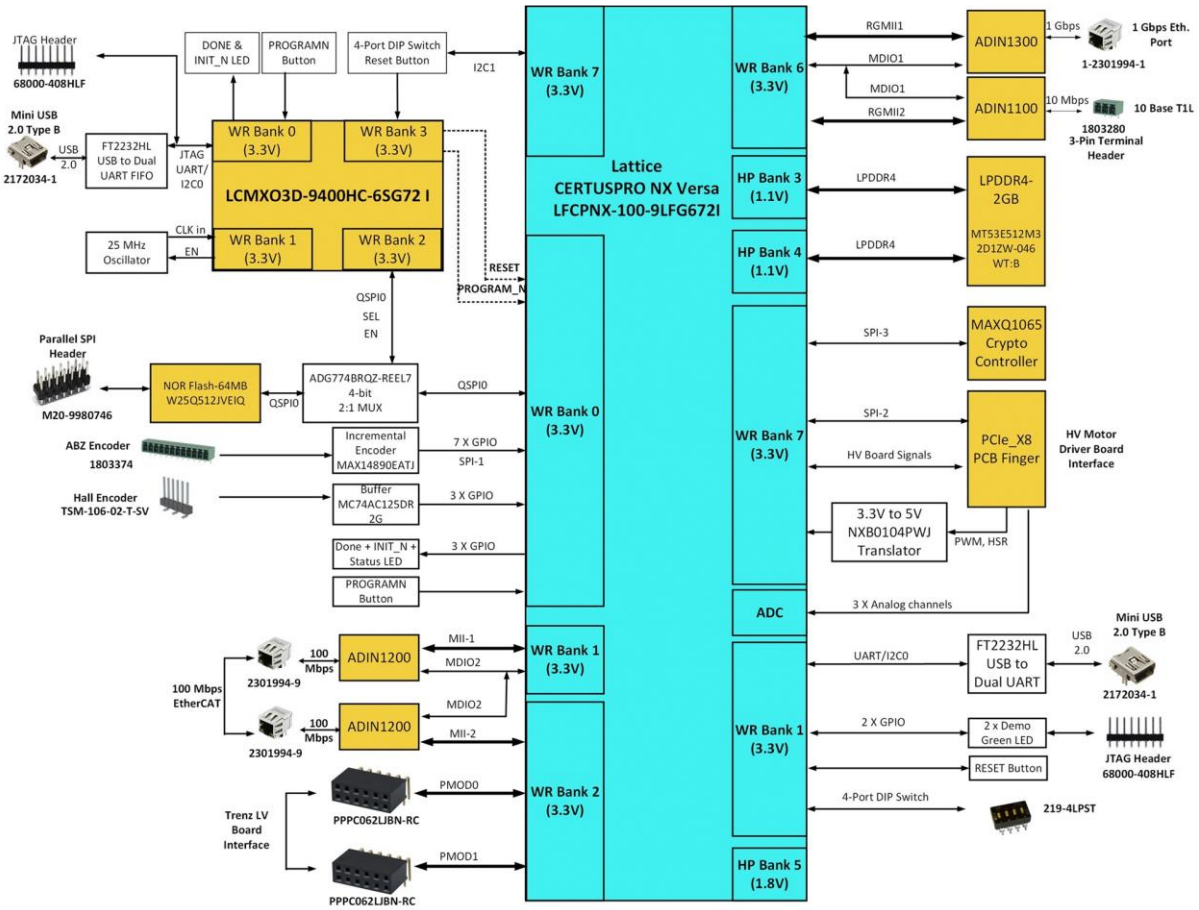

Figure 2 Block Diagram of Motion Control Board

2.2 Features

The Motion Control Board based on Lattice CertusPro-NX with ADI PHY includes the following features:

- CertusPro-NX FPGA (LFCPNX-100-9LFG672I)
- Root port configuration
- 2×RJ45 100 Mbps EtherCAT (ADIN1200 PHY)
- 1×RJ45 1Gbps RGMII (ADIN1300 PHY)
- 1×10 Base T1-L 10Mbps (ADIN1100 PHY)
- LPDDR4 DRAM Memory

• On-board Boot Flash – 128 Mb Serial Peripheral Interface (SPI) Flash, with Quad read feature
• USB-B connection for CPNX device programming and Inter-Integrated Circuit Bus (I2C) utility
• USB-B connection for MACHXO3D device programming and Inter-Integrated Circuit Bus (I2C) utility
• 2 x PMOD Connector
• 4 input DIP switches for CPNX & 4 input DIP switches for MACHXO3D, 4 push buttons, 2 status LEDs for CPNX & 2 status LEDs for MACHXO3D.
• MAXQ1065 Cryptographic controller
• Lattice Radiant® software programming support
• Multiple reference clock sources
• ADI Compatible HV Board.
• ABZ and HALL Encoder
• Motor Control Driver IC Compatible

Caution: The CertusPro-NX Motion Control Board contains ESD-sensitive components. ESD safe practices should be followed while handling and using the development board.

2.3 CertusPro-NX Device

The Motion Control Board based on Lattice CertusPro-NX with ADI PHY features the CertusPro-NX device in an LFG672 package, also referred to as LFCPNX-100-9LFG672I. The low-power general purpose FPGA can be used in a wide range of applications across multiple markets and is optimized for bridging and processing needs in edge applications. For more information on the capabilities of CertusPro-NX device, see CertusPro-NX Family Data Sheet (FPGA-DS-02086).

2.4 Applying power to the board

The Motion Control Board based on Lattice CertusPro-NX with ADI PHY comes ready to power up. The board can power up using a 12 V DC power source input. The power supply can be connected with the right-angle DC power input jack J44, which is fused with a surface mounted fuse F1, as shown in Figure 2 and Table 4. The fuse can prevent the crashed current from flowing into the internal circuits and cause serious damage. Power LEDs light after applying 12 V DC power to the CertusPro-NX Evaluation Board to indicate that the board is functioning.

Figure 3 12 V DC Power Supply

Table 4 Board Power Supply

Part Designator	Description
J44	12 V DC Input Supply Jack
F1	12 V DC Input Supply Fuse
SW6	—

3 JUMPER DEFINITIONS

Table 5 Jumper Details

Header Ref. Des.	Header Type	No. of pins	Function
J1	1 X 2	2	MachXO3D FTDI Chip RESET
J3	1 X 2	2	Set MachXO3D pins to JTAG
J4	1 X 2	2	Connect / disconnect VCCAUXSDQ0 from 1.8V
J5	1 X 2	2	MachXO3D Programming
J7	1 X 2	2	Connect / disconnect VCCAUXSDQ1 from 1.8V
J14	1 X 2	2	Connect / disconnect VCCSD from 1V
J18	2 X 7	14	QSPI Pin Header
J19	1 X 2	2	Certus-Pro Programming
J24	1 X 2	2	Connect / disconnect VCCADC18 from 1.8V
J28	1 X 3	3	Short 1-2-> 1.8V to ADC_REF0 Short 2-3-> External Voltage to ADC_REF0
J29	1 X 3	3	Short 1-2-> 1.8V to ADC_REF1 Short 2-3-> External Voltage to ADC_REF1
J30	1 X 2	2	Connect / disconnect FTDI Reset to GND
J31	1 X 8	8	Certus-Pro FTDI Chip JTAG
J32	1 X 3	3	Short 1-2-> FTDI to Certus-pro through UART Short 2-3-> FTDI to Certus-pro through I2C
J33	1 X 3	3	Short 1-2-> FTDI to Certus-pro through UART Short 2-3-> FTDI to Certus-pro through I2C
J34	USB 2.0 Mini Connector		USB 2.0 Mini Connector for Certus-Pro FTDI.
J42	1 X 2	2	Connect / disconnect VCCCORE Power rail.
J43	1 X 2	2	Connect / disconnect 1.8V to VCCAUXA
J44	DC Power Jack		DC Power Jack for 12V supply.
J45	1 X 2	2	Connect / disconnect 1.8V to VCCAUX
J46	1 X 2	2	Connect / disconnect 1.1V to VCCIO3 & VCCIO4
J47	1 X 2	2	Connect / disconnect 1.8V to VCCIO5
J48	1 X 2	2	Connect / disconnect 3.3V to VCCIO6
J49	1 X 2	2	Connect / disconnect 3.3V to VCCIO2
J50	1 X 2	2	Connect / disconnect 3.3V to VCCIO7
J51	1 X 2	2	Connect / disconnect 3.3V to VCCIO1
J55	1 X 2	2	Connect / disconnect 3.3V to VCCIO0
J60	1 X 2	2	Connect / disconnect 12 MHz clock to
J64	2 x 6	12	PMOD0 Connector
J65	2 x 6	12	PMOD1 Connector
J66	10Base T1-L Ethernet connector		10Base T1-L Ethernet connector
J67	RJ45 with magnetics for 100Mbps		RJ45 with magnetics for 100Mbps
J68	RJ45 with magnetics for 100Mbps		RJ45 with magnetics for 100Mbps
J69	RJ45 with magnetics for 1Gbps		RJ45 with magnetics for 1Gbps
J71	1 x 12	12	ABZ Encoder
J75	1 x 6	6	Hall Encoder

J76	1 X 3	3	Short 1-2-> HITH/CSn_SPI connect to VCC_VL Short 2-3-> HITH/CSn_SPI connect to GND
J77	1 X 3	3	Short 1-2-> SNGL/CLK connect to VCC_VL Short 2-3-> SNGL/CLK connect to GND
J78	1 X 3	3	Short 1-2-> TTL/SDI connect to VCC_VL Short 2-3-> TTL/SDI connect to GND
J79	1 X 3	3	Short 1-2-> DI_DTTLY connect to VCC_VL Short 2-3-> DI_DTTLY connect to GND
J80	1 X 3	3	Short 1-2-> DI_TTL2 connect to VCC_VL Short 2-3-> DI_TTL2 connect to GND
J81	1 X 3	3	Short 1-2-> DI_TTL3 connect to VCC_VL Short 2-3-> DI_TTL3 connect to GND
J82	USB 2.0 Mini Connector		USB 2.0 Mini Connector for MachXO3D FTDI.
J83	1 X 8	8	MachXO3D FTDI Chip JTAG
J85	1 X 8	8	MachXO3D Debug GPIO
J87	1 X 3	3	Short 1-2-> QSPI Flash connect to Certus-pro Short 2-3-> Mux-Demux In pin control to MachXO3D
J88	1 X 2	2	Connect / disconnect MachXO3D Programn pin
J89	1 X 2	2	Connect / disconnect MachXO3D Reset out to certus_pro reset
J90	1 X 2	2	Connect / disconnect crypto Reset out to certus_pro reset
J92	1 X 3	3	Short 1-2-> External battery for MAXQ1065 Short 2-3-> Onboard 3.3V for MAXQ1065
J94	1 X 3	3	Pin no. 1 -> External Battery +ve Pin no. 2 -> External Battery -ve Pin no. 3 -> TAMPER_IN Input
J95	1 X 3	3	Short 1-2-> QSPI Flash connect to Certus-pro Short 2-3-> Mux-Demux En pin control to MachXO3D

4 PROGRAMMING AND I2C

The JTAG/SPI programming architecture and I2C interface of the Motion Control Board based on Lattice CertusPro-NX with ADI PHY are shown in Figure 3.

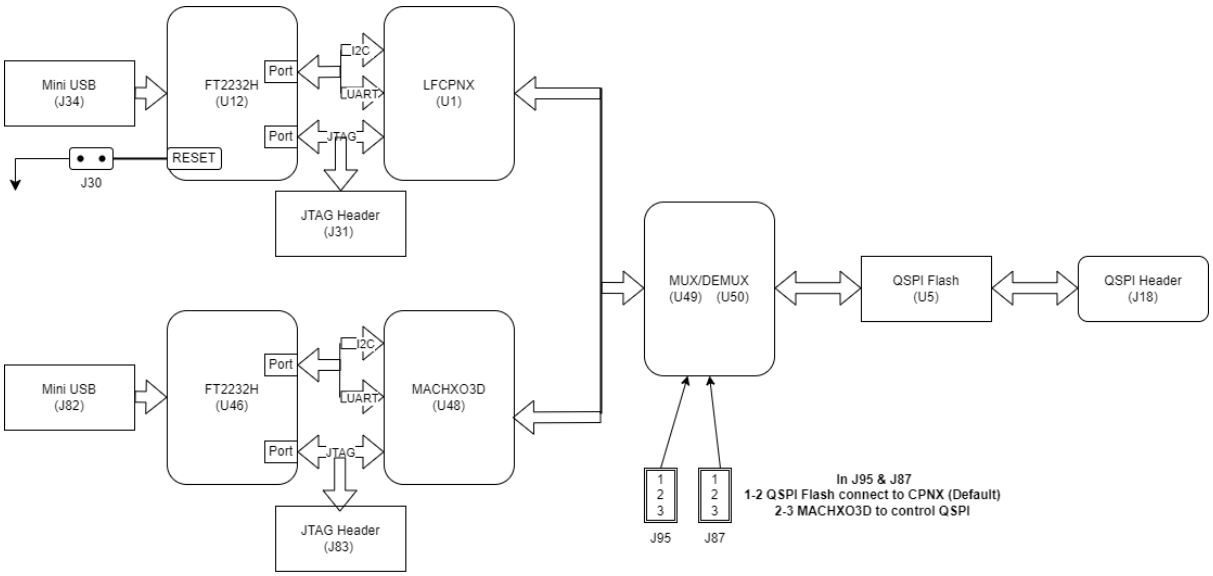

Figure 4 Configuration Architecture

4.1 JTAG Download Interface.

The Motion Control Board based on Lattice CertusPro-NX with ADI PHY has a built-in download controller for programming the CertusPro-NX device. It uses an FT2232H Future Technology Devices International (FTDI) part to convert USB to JTAG. To use the built-in download cable, connect the USB cable from a PC with Radiant Programmer tool installed to the mini-USB connector J34 on the board. The USB hub on the PC detects the cable of the USB function on Port 0, making the built-in cable available for use with the Radiant programming software.

4.2 Alternate JTAG Download Interface

J31 is an 8-pin standalone JTAG header used with an external Lattice download cable that is available separately, when the FTDI part is disabled from the JTAG chain after resetting FTDI. A USB download cable can be attached to the board using this JTAG Header to interface with the CertusPro-NX device. For details on the connection between the USB download cable and J82, refer to Programming Cables User Guide (FPGA-UG-02042).

JTAG Header can also be used as test point when USB to JTAG is working. The JTAG connection is shown in Table 6.

Table 6 JTAG Connection

J31 Pin Number	Signal Name	CertusPro-NX Pin
1	3V3_OUT	—
2	TDO	M8
3	TDI	L9
4	—	—
5	—	—
6	TMS	L7
7	GND	—

8	TCK	M5

4.3 Other FPGA Configuration Pins

The Motion Control Board based on Lattice CertusPro-NX with ADI PHY provides test points for other FPGA configuration pins as shown in Table 7.

Table 7 Other JTAG Signals

Signal Name	CertusPro-NX Ball Location	Test Point	Push Button
PROGRAMN	G4	—	SW2
INITN	G2	TP59	—
DONE	G5	TP58	—

- INITN: Open drain pin. This signal is driven to LOW when configuration sequence is started, indicating the device is in initialization state. At this moment, the LED (D80) is lighted with red color. This signal is released after initialization is completed, and the configuration download starts.
- DONE: Open drain pin. This signal is driven to LOW during configuration time. This signal releasing indicates the device has completed configuration. At this moment, the LED (D106-1) is lighted with green color.

For more information on Certus-NX JTAG and SPI programming, refer to sysCONFIG Usage Guide for Nexus Platform (FPGA-TN-02099).

4.4 JTAG to MSPI Pass-through Interface

The download controller can also access the JTAG to MSPI pass-through circuit that allows the slave SPI Flash to be erased, programmed, and read with Radiant Programmer.

4.5 SPI Flash Device Selection in Programmer

The Flash device on this board is a Winbond W25Q512JVEIQ which is powered by default to 3.3 V. Flash device programming is discussed in more detail in sysCONFIG Usage Guide for Nexus Platform (FPGA-TN-02099).

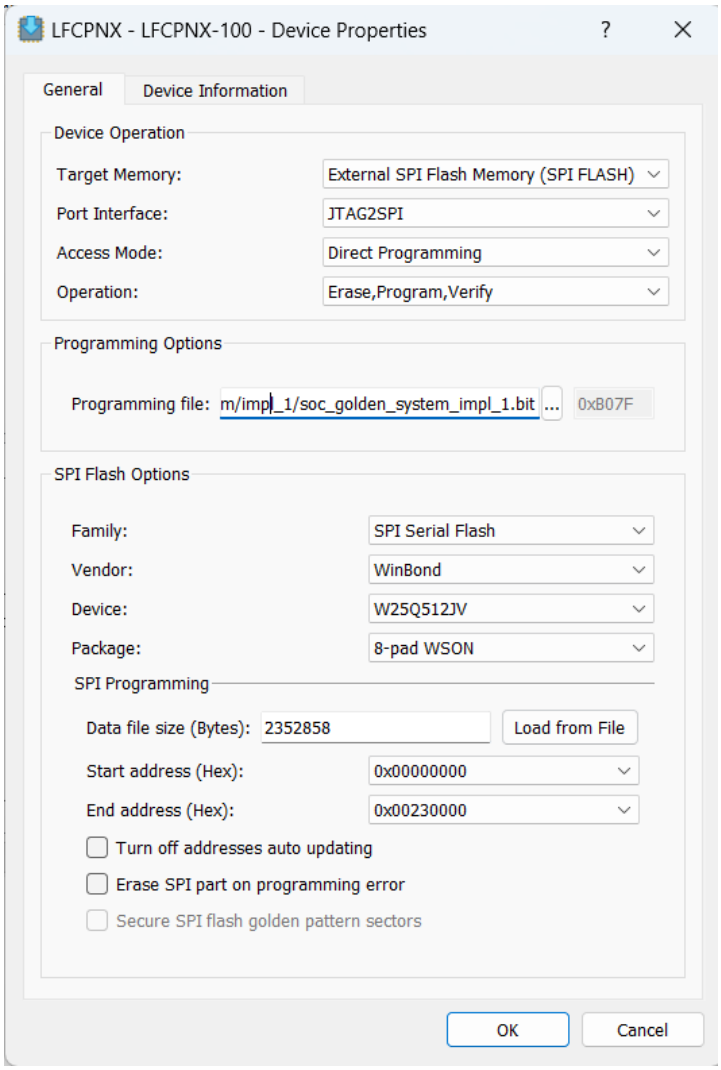

Figure 5 SPI Flash Operation Dialog

4.6 Programming the FPGA

This section guides you through the process of uploading the bit file in SPI Flash. Follow the instructions below.

Note: The software programs are available at [FPGA Design Software | Lattice Semiconductor](). The software programs are available for download only if you log into your account at this website.

1. Connect the 12 V power adapter to the J44 connector of the CertusPro-NX Motion Control Board.
2. Connect the USB Cable to the J34 connector of the CertusPro-NX Motion Control Board.
3. If the Radiant project is already opened in Lattice Radiant software, click the Radiant Programmer icon from the toolbar. If the project is not opened, click the **Windows Start** menu and choose **Radiant Programmer** to open the stand-alone Radiant Programmer. The **Radiant Programmer - Getting Started** dialog pops up (Figure 5). The default project name is **Untitled**. Enter a desired project name and browse to choose the project location from the **Project Location** area. Click OK.

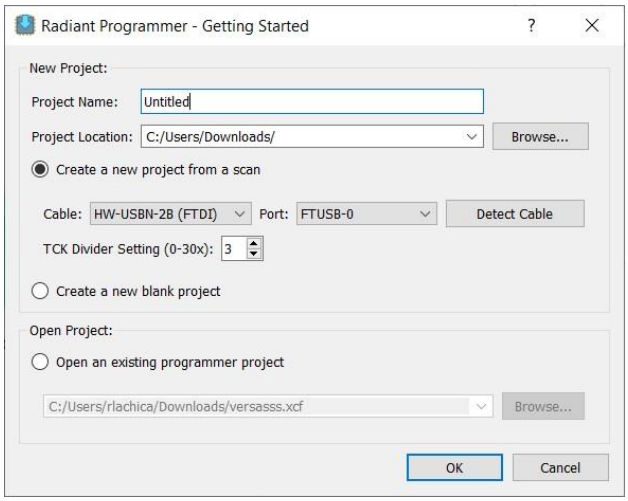

Figure 6 Stand-alone Radiant Programmer Opened from Windows Start Menu

4. You can see the selected project opened in the Programmer (Figure 6).

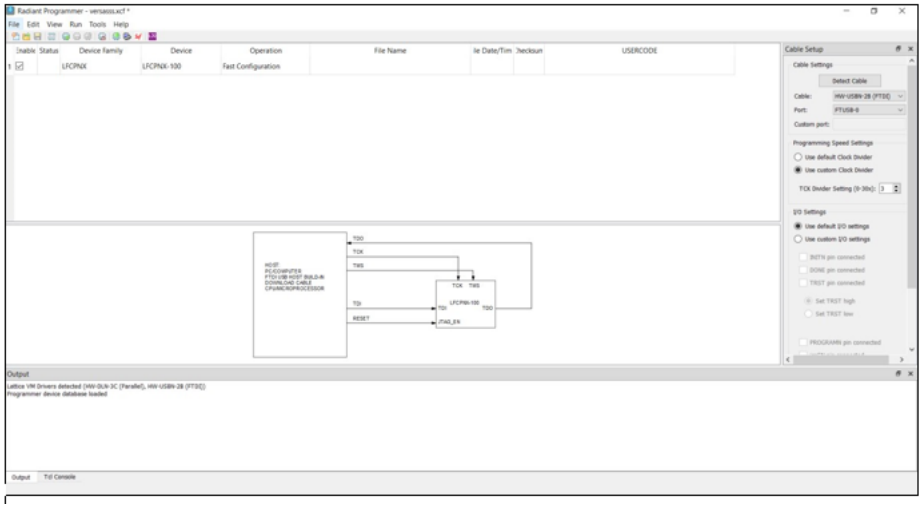

Figure 7 Radiant Programmer Opened from Windows Start Menu

5. If the settings you see are not the same as those shown in Figure 7, manually make changes and make settings (device family, device, and so on) the same as those shown in Figure 7.

Figure 8 FPGA Device Setting

6. Click on **Fast Configuration** from the **Operation** column (Figure 8). The **Device Properties** dialog pops up (Figure 8). Change the **Target Memory** settings using the drop-down menu, and then you can see the device properties settings exactly as those shown in Figure 8.

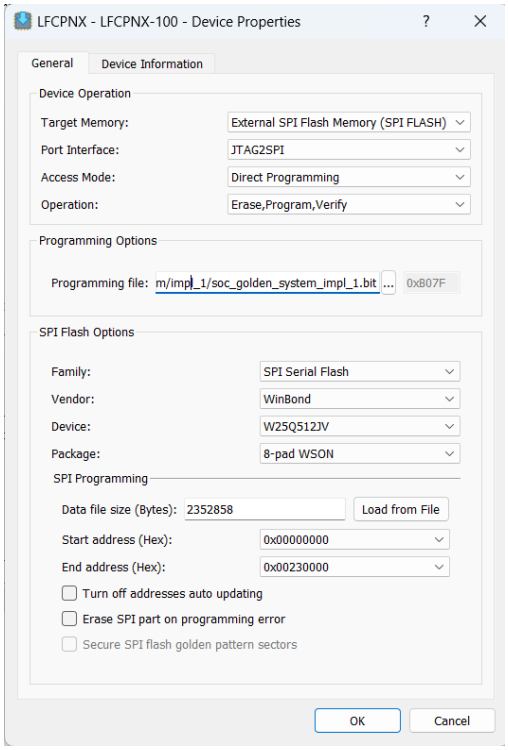

Figure 9 Device Properties Dialog for SPI Flash Programming Setting

6. Browse to choose the programming file “soc_golden_system_impl_1’.bit (Figure 9).
7. Click **OK**.
8. Click the **Program Device con.**

Figure 10 Programmer Toolbar

9. Check the Output console for the status of the programming. You should see **Operation: Successful**, as shown in Figure 10.

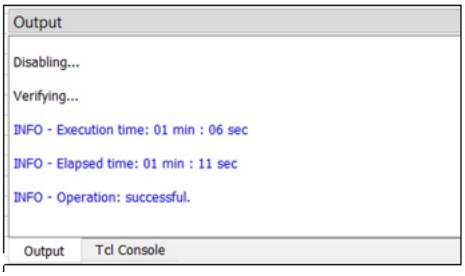

Figure 11 Programmer Output Window

11. If there is any issue or problem, refer to the Troubleshooting section for more details.
12. After programming, do power cycle the board.

4.7 Troubleshooting

This section guides you through the troubleshooting process while testing the design.

- If you get verification error while dumping the .bit file, try changing the TCK frequency to be greater than 4. The TCK Divider setting option can be found from the right-click menu of the Radiant Programmer Window (Figure 11). Restart programming by clicking the **Program Device icon.**

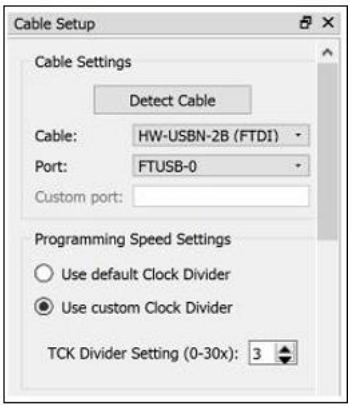

Figure 12 TCK Frequency Setting

• If the device is not detected on port FTUSB-0, click on **Detect Cable** and select the port FTUSB-1 (Figure 12).

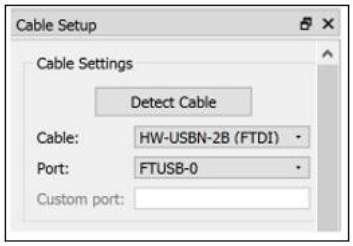

Figure 13 Port Selecting

5 CERTUSPRO-NX CLOCK SOURCES

The Motion Control Board based on Lattice CertusPro-NX with ADI PHY has three clock sources for the CertusPro-NX FPGA. Refer to Table 8 and Figure 13 for more details regarding the clock sources.

Table 8 Clock Sources

Clock Frequency	Signal Name	Clock Sources	CertusPro-NX Ball	Type
125 MHz	F_CLKIN_125Mhz	U4	P24	Single Ended
100 MHz	F_DDR_100Mhz_P F_DDR_100Mhz_N	U6	AB19 AB18	Differential
25 MHz	F_MII_CLKIN_25MHz	Y3	N23	Single Ended
125 MHz	F_125Mhz_P F_125Mhz_N	U3	W24 W23	Differential

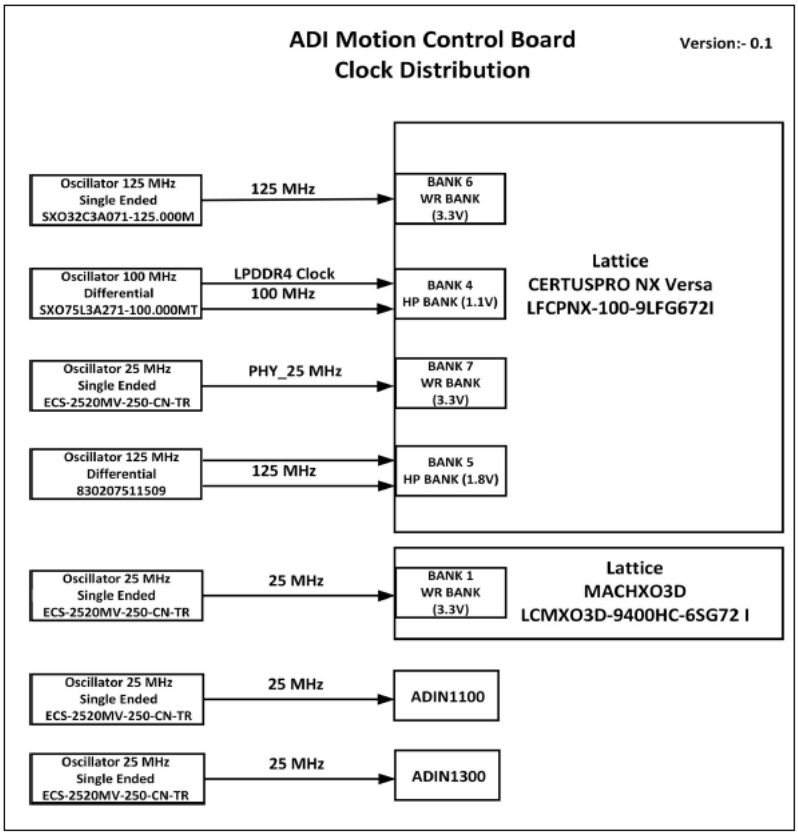

Figure 14 Clock Scheme

6 POWER SCHEME

The Motion Control Board based on Lattice CertusPro-NX with ADI PHY has most of the on-board regulators powered by an external 12 V power. Refer to Appendix A. CertusPro-NX Motion Control Board Schematics to see the details of these power supply options. Figure 14 shows the high-level power supply architecture of the board. Table 9 shows the voltage options available for various VCCIO supplies.

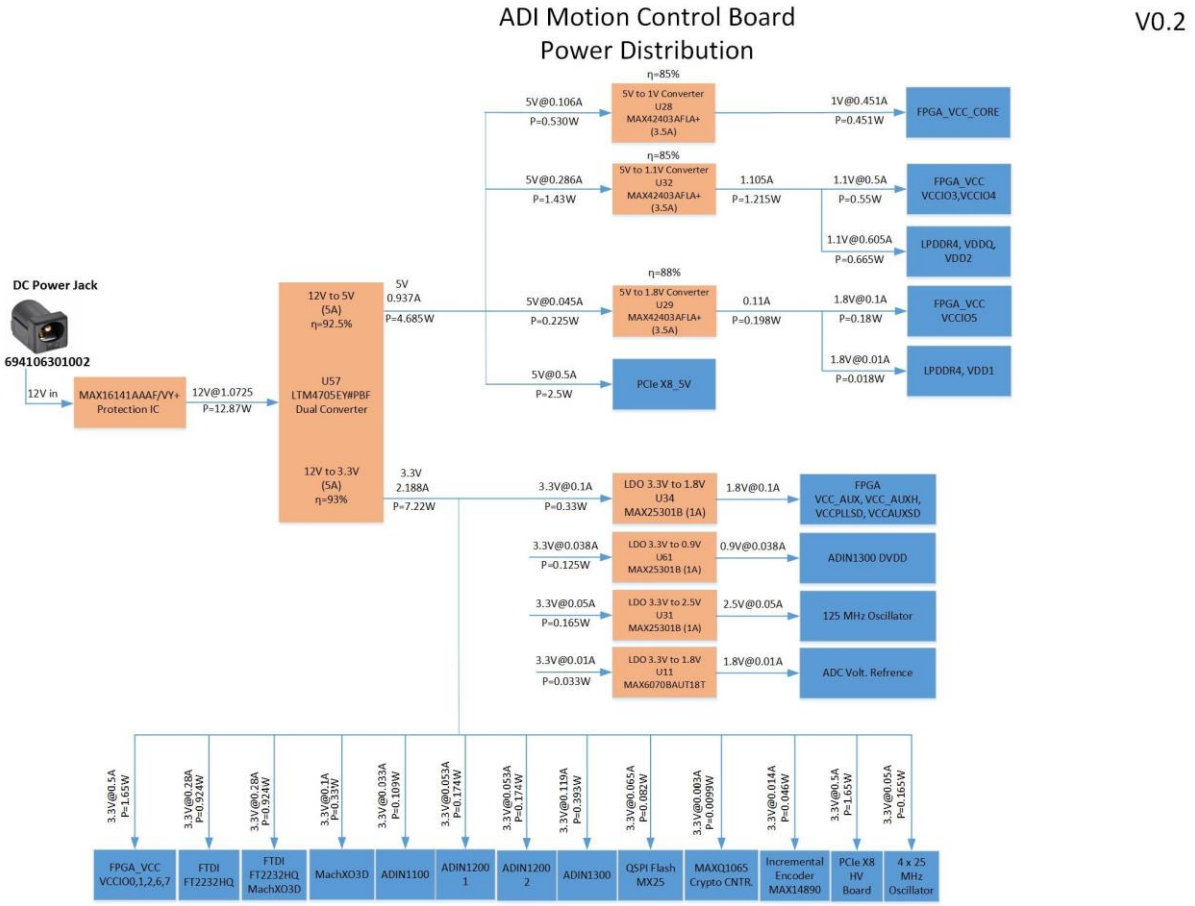

Figure 15 Power Scheme

Table 9 VCCIO Supply Options

VCCIO Bank	3.3 V	2.5 V	1.8 V	1.5 V	1.2 V	1.1 V
VCCIO0	Fixed	—	—	—	—	—
VCCIO1	Fixed	—	—	—	—	—
VCCIO2	Fixed	—	—	—	—	—
VCCIO3	—	—	—	—	—	Fixed
VCCIO4	—	—	—	—	—	Fixed
VCCIO5	—	—	Fixed	—	—	—
VCCIO6	Fixed	—	—	—	—	—
VCCIO7	Fixed	—	—	—	—	—

The Motion Control Board based on Lattice CertusPro-NX with ADI PHY provide status LEDs to provide a visual indication of power status (Table 10).

Table 10 Power Status LED Definition

REFDES	LED Name	Color	LED status	Function
D106-2	Power LED	Green	On	12V to 5V Power Supply is healthy
D136	Power LED	Green	On	Power in from USB 2.0 Mini for MachXO3D FTDI
D144	Power LED	Green	On	HV board Power is healthy
D145	Power LED	Green	On	5V to 1V_VCC_CORE Power Supply is healthy
D147	Power LED	Green	On	5V to 1.8V Power Supply is healthy
D148	Power LED	Green	On	5V to 1.1V Power Supply is healthy
D153	Power LED	Green	On	Power in from USB 2.0 Mini for Certus-Pro FTDI
D70	Status LED	Green	On	Status LED for FTDI chip of Certus-pro
D106-3	Status LED	Green	On	Status LED for Certus-Pro

7 CONTROL BUSES – I2C, UART, AND SPI

This section describes the topology of the various configuration and communication buses.

7.1 I²C topology

The Motion Control Board based on Lattice CertusPro-NX with ADI PHY uses the I²C bus to support CertusPro-NX configuration. The I²C bus has the signal names FTDI_I2C_SCL and FTDI_I2C_SDA. When the jumpers (J32, J33) are closed, the I²C bus is connected to a dedicated CertusPro-NX GPIO bank 1. I²C and UART share the same output port B on FTDI chip. The I²C connections are summarized in Table 11.

Table 11 I²C Bus Connections

Signal Name	CertusPro-NX Ball Location	FTDI Chip Ball Location	Jumper
FTDI_I2C_SCL	M7	38	J32
FTDI_I2C_SDA	M6	39&40	J33

7.2 UART topology

The board provides one UART communication interface by providing a flexible connection between the CertusPro-NX device and FTDI chip. Close the two jumpers, J32 and J33, to connect to two general-purpose I/O in Bank 1, as shown in Table 12. This UART is an alternative with I²C bus by setting FTDI configuration.

Table 12 UART Bus Communications

Signal Name	CertusPro-NX Ball Location	FTDI Chip Ball Location	Jumper
FTDI_UART_TXD	L8	38	J32
FTDI_UART_RXD	M9	39	J33

Note: The signal name and ball location refer to the FTDI chip perspective. When assigning the pins in Radiant, make sure the UART soft IP TX signal is connected to pin M9 (FTDI_UART_RXD). Repeat the same process for the RX signal.

7.3 SPI topology

One of the major functions of SPI connections on the board is to support CertusPro-NX configuration from the SPI Flash or the Parallel Configuration Header (J18), as shown in Table 13. The CertusPro-NX Motion Control Board can support both Master SPI (MSPI) and Slave SPI (SSPI) modes for CertusPro-NX configuration.

Table 13 SPI Bus Communications

Signal Name	CertusPro-NX Ball	Parallel Configuration Header Pin
CONN_FLASH_MCLK	G6	12
CONN_FLASH _MOSI	H7	5
CONN_FLASH _MISO	H6	7
CONN_FLASH_CS	G7	2
CONN_FLASH_DQ2	K5	11
CONN_FLASH_DQ3	H4	9
MCSNO	H3	3

8 LEDS AND SWITCHES

This section describes the Motion Control Board based on Lattice CertusPro-NX with ADI PHY LEDs and switches that can be used in demo and customer designs.

8.1 DIP Switch

Four CertusPro-NX pins are connected to the DIP switch (SW1) to allow manual actuating input to the FPGA. One side of each switch is connected to GPIOs within bank 5 and is pulled up through 4.7 kΩ resistors. The other side is grounded. The designated pins are connected as shown in Table 14.

Table 14 DIP Switch Signals

Signal Name	CertusPro-NX Ball Location	CertusPro-NX Bank
SWITCH1	U8	1
SWITCH2	R7	1
SWITCH3	T7	1
SWITCH4	P8	1

8.2 Push Buttons

The Motion Control Board based on Lattice CertusPro-NX with ADI PHY provides four push button switches, SW2, SW3, SW8, SW11 for demo and user applications. One of the buttons is a pre-defined functional pin, and the other three are generic pins. Pressing these buttons drives a logic level “0” to the corresponding I/O pins. The designated pins are connected as shown in Table 15.

Table 15 Push Button Switch Signals

Signal Name	CertusPro-NX Ball Location	Push Button Reference	Logic Level at Button Pressed
PROGRAMN	G4	SW2	0
SW_F_RESETn	N9	SW3	0
X03D_ PROGRAMN	61	SW8	0
XO3D_SW_RSTn	14	SW11	0

For more information on PROGRAMN, refer to sysCONFIG Usage Guide for Nexus Platform (FPGA-TN-02099).

8.3 Debug LEDs

The Motion Control Board based on Lattice CertusPro-NX with ADI PHY provides two LEDs that are connected to I/O within Bank 1. The LEDs are lighted with green color when the output is driven LOW. The designated pins are connected as shown in Table 16.

Table 16 Debug LED Signals

Signal Name	CertusPro-NX Ball Location	CertusPro-NX Bank/Color
LED0	R5	1/Green
LED1	R4	1/Green

9 HEADERS/CONNECTORS AND CERTUSPRO-NX DEVICE BALL MAPPING

This section describes the Motion Control Board based on Lattice CertusPro-NX with ADI PHY headers/connectors and ball mapping.

9.1 External Flash Configuration Header

Table 17 SPI Flash Configuration Header Pin Connections

J18 Pin Number	Signal Name	CertusPro-NX Ball Location
1	CONN_PROGRAMN	G4
2	CONN_FLASH_CS#	G7
3	MCSNO	H3
4	DONE	G5
5	CONN_FLASH_MOSI	H7
6	CONN_INITN	G2
7	CONN_FLASH_MISO	H6
8	-	-
9	CONN_FLASH_DQ3	H4
10	VCCIO0	-
11	CONN_FLASH_DQ2	K5
12	CONN_FLASH_MCLK	G6
13	GND	-
14	GND	-

Note:

1. These connections are possible if 0 Ω resistors are installed.

9.2 PMOD Header

J64 and J65 headers can be used as GPIO or as a connector to PMOD interface.

Table 18 PMOD Header Pin Details

Pin Name		Signal Name	CertusPro-NX Ball Location
J64	1	PMOD0_1_ADC_CH	T3
	2	PMOD0_2_ADC_SCK	T2
	3	PMOD0_3_ADC_CS	U1
	4	PMOD0_4_SENSOR_FAULT	AA2
	7	PMOD0_7_ADC0_DO	V2
	8	PMOD0_8_ADC1_DO	W1
	9	PMOD0_9_ADC2_DO	W3

	10	PMOD0_10_ADC3_DO	AB1
J65	1	PMOD1_1_PWM_CH0	T1
	2	PMOD1_2_PWM_CH1	Y2
	3	PMOD1_3_PWM_CH2	U3
	4	PMOD1_4	V1
	7	PMOD1_7_EN_CH0	V3
	8	PMOD1_8_EN_CH1	W2
	9	PMOD1_9_EN_CH2	Y1
	10	PMOD1_10	AA1

9.3 PCIe edge connector

Table 19 PCIe Edge Connector Pin Details

CN1 Pin Num	Signal Name	CertusPro-NX Ball	CN1 Pin Name	Signal Name	CertusPro-NX Ball
A1	VCC_HV_24V_IN	-	B1	VCC_HV_24V_IN	-
A2	VCC_HV_24V_IN	-	B2	VCC_HV_24V_IN	-
A3	VCC_HV_24V_IN	-	B3	VCC_HV_24V_IN	-
A4	GND_24V	-	B4	GND_24V	-
A5	GND_24V	-	B5	GND_24V	-
A6	GND_24V	-	B6	GND_24V	-
A7	GND_ISO	-	B7	GND_ISO	-
A8	VCC_HV_5V_ISO	-	B8	VCC_HV_5V_ISO	-
A9	VCC_HV_5V_ISO	-	B9	VCC_HV_5V_ISO	-
A10	GND_ISO	-	B10	GND_ISO	-
A11	VCC_HV_5V	-	B11	VCC_HV_5V	-
A12	GND	-	B12	HV_PGOOD	J19
A13	HV_MCLKOUT	J20	B13	GND	-
A14	VCC_HV_3V3	-	B14	HV_MDAT01	K25
A15	GND	-	B15	HV_MDAT03_V	N21
A16	HV_MDAT02_W	N22	B16	GND	-
A17	HV_MDAT04_U	N20	B17	HV_GPIO_3	L21
A18	GND	-	B18	GND	-
A19	HV_GPIO_0	J26	B19	PWM_U_UP	K26
A20	GND	-	B20	PWM_U_LO	L26
A21	HSR_U_UP	L20	B21	GND	-
A22	HSR_U_LO	L19	B22	GND	-

A23	GND	-	B23	PWM_V_UP	L25
A24	GND	-	B24	PWM_V_LO	L24
A25	HSR_V_UP	M26	B25	GND	-
A26	HSR_V_LO	N26	B26	GND	-
A27	GND	-	B27	PWM_W_UP	L23
A28	GND	-	B28	PWM_W_LO	L22
A29	HSR_W_UP	N25	B29	GND	-
A30	HSR_W_LO	N24	B30	GND	-
A31	GND	-	B31	HV_STO_ACK_B	K20
A32	HV_GPIO_1	J25	B32	GND	-
A33	No Connection	-	B33	HV_A_CH0	-
A34	GND	-	B34	HV_A_CH1	-
A35	HV_A_CH2	-	B35	GND	-
A36	No Connection	-	B36	GND	-
A37	HV_CSn	J21	B37	HV_SDI	K21
A38	HV_GPIO_2	J22	B38	HV_SDO	K19
A39	HV_SCLK	K18	B39	GND	-
A40	VCC_HV_3V3	-	B40	GND	-
A41	GND	-	B41	HV_CMD_0	N19
A42	GND	-	B42	HV_CMD_1_LS	P18
A43	HV_CMD_2	P19	B43	GND	-
A44	HV_CLK_TD	P20	B44	GND	-
A45	HV_EN_TR_LS	K24	B45	HV_GPIO_4	P26
A46	GND	-	B46	HV_GPIO_5	R9
A47	No Connection	-	B47	GND	-
A48	No Connection	-	B48	No Connection	-
A49	GND	-		GND	-

Note:

1. Connects to CPNX if Endpoint PCIe selected.

9.4 ADIN1100 10baseT1L Interface

Table 20 ADIN1100 10baseT1L Interface Pin Details

Signal Name	CertusPro-NX Ball
RGMII2_RESET_N	P23
RGMII2_INT_N	P21
RGMII2_RXC	R20
RGMII2_RX_CTL	R21
RGMII2_RXD3	T22
RGMII2_TXC	R25
RGMII2_TX_CTL	R26

RGMII2_RXD0	T25
RGMII2_RXD1	T24
RGMII2_RXD2	T23
RGMII2_TXD3	V18
RGMII2_TXD2	V19
RGMII2_TXD1	V20
RGMII2_TXD0	V21

9.5 ADIN1200 EtherCAT1 Interface

Table 21 ADIN1200 EtherCAT1 Interface Pin Details

Signal Name	CertusPro-NX Ball
CLKOUT25_MII1	T6
MII1_LINK_ST	T8
MII1_RX_CLK	R8
MII1_TX_CLK	R6
MII1_RX_ER	P9
MII1_RX_DV	N8
MII1_RXD2	N6
MII1_RXD3	N7
MII1_RXD0	N4
MII1_RXD1	N5
MII1_RESET_N	N2
MII1_TX_ER	N3
MII1_TXD3	M1
MII1_TX_EN	N1
MII1_TXD1	M3
MII1_TXD2	M2
MII1_TXD0	M4
MII1_INT_N	L6
MII_MDC	L3
MII_MDIO	L1

9.6 ADIN1200 EtherCAT2 Interface

Table 22 ADIN1200 EtherCAT2 Interface Pin Details

Signal Name	CertusPro-NX Ball
MII2_INT_N	AB3
MII2_RESET_N	AB2
MII2_TX_EN	Y4
MII2_TX_ER	AA4
MII2_TXD1	W5
MII2_TXD0	W4
MII2_TXD3	W7
MII2_TXD2	W6
MII2_RXD0	V5
MII2_RXD1	V6
MII2_RX_DV	V4
MII2_RXD3	V8
MII2_RXD2	V7
MII2_TX_CLK	U6
MII2_RX_ER	U7
MII2_RX_CLK	U2
CLKOUT25_MII2	T5
MII2_LINK_ST	T4

9.7 ADIN1300 1Gbps Ethernet Interface

Table 23 ADIN1300 1Gbps Ethernet Interface Pin Details

Signal Name	CertusPro-NX Ball
RGMII1_RX_CTL	P25
RGMII1_RXC	P22
RGMII1_RESET_N	R22
RGMII1_INT_N	T26
RGMII1_TXD3	T21
RGMII1_TXD2	T20
RGMII1_TXD1	T19
RGMII1_TXD0	T18
RGMII1_TXC	U19
RGMII1_TX_CTL	U18

RGMII1_RXD0	U22
RGMII1_RXD1	U23
RGMII1_RXD2	U24
RGMII1_RXD3	U25

9.8 ABZ Encoder

Table 24 ABZ Encoder Pin Details

Signal Name	CertusPro-NX Ball
LS_ENC1_A	K6
LS_ENC1_B	K7
LS_ENC1_Z	K8
LS_ENC1_Y	J7
ENC1_SCLK	J6
ENC1_CS	J5
ENC1_MISO	J3
ENC1_MOSI	J2
ENC1_IRQB	J1
LS_ENC1_LO3	H1
LS_ENC1_LO2	H2

9.9 HALL Encoder

Table 25 HALL Encoder Pin Details

Signal Name	CertusPro-NX Ball
HALL_U_LS_ENC2_A	K2
HALL_V_LS_ENC2_B	K3
HALL_W_LS_ENC2_C	K4

10 SOFTWARE REQUIREMENTS

The following software versions are required to develop designs for the Motion Control Board based on Lattice CertusPro-NX with ADI PHY:

- Lattice Radiant Software 2023.2 or later
- Lattice Radiant Programmer 2023.2 or later.

11 STORAGE AND HANDLING

Static electricity can shorten the life span of electronic components. Observe these tips to prevent damage that can occur from electrostatic discharge:

- Use antistatic precautions such as operating on an antistatic mat and wearing an antistatic wristband.
- Store the development board in the provided packaging.
- Touch a metal USB housing to equalize voltage potential between you and the board.

12 ORDERING INFORMATION

- Please go through Arrow Electronics for ordering inquiry.

APPENDIX A. MOTION CONTROL BOARD BASED ON LATTICE CERTUSPRO-NX WITH ADI PHY SCHEMATICS

https://github.com/ArrowElectronics/ADI-Lattice-MotionControlBoard/blob/main/HW_Package/Schematic/eIC_MCB_SCH_16_01246_01.pdf

APPENDIX B. MOTION CONTROL BOARD BASED ON LATTICE CERTUSPRO-NX WITH ADI PHY BILL OF MATERIALS

https://github.com/ArrowElectronics/ADI-Lattice-MotionControlBoard/blob/main/HW_Package/BOM/eIC_MCB_BOM_18_01246_01.xlsx

TECHNICAL SUPPORT ASSISTANCE

- For technical support, please go through Arrow Electronics and raise the ticket.