Lattice Radiant 2025.1 Software Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant 2025.1 Software

- **Device Support:**
  - Certus™-N2 (LN2-CT-20ES)
    - 22 (-1/-2/-3) 0.82V (COM/IND) – ASG410
  - Certus™-NX (LFD2NX)
    - 9 (-7/-8/-9) 1.00V (COM/IND) – CSFBGA121, CABGA196
    - 15 (-7/-8/-9) 1.00V (COM/IND) – CABGA256, CABGA400
    - 17 (-7/-8/-9) 1.00V (COM/IND/AUTO) – CSFBGA121, CABGA196
    - 25 (-7/-8/-9) 1.00V (COM/IND) – CABGA256, CABGA400
    - 35 (-7/-8/-9) 1.00V (COM/IND) – CABGA400, CABGA484
    - 65 (-7/-8/-9) 1.00V (COM/IND) – CABGA400, CABGA484
  - MachXO5™-NX (LFMXO5)
    - 35 (-7/-8/-9) 1.00V (COM/IND) – BBG400
    - 35T (-7/-8/-9) 1.00V (COM/IND) – BBG484
    - 65 (-7/-8/-9) 1.00V (COM/IND) – BBG400
    - 65T (-7/-8/-9) 1.00V (COM/IND) – BBG484

- **Tool and Other Enhancements:**
  - **Command Line** – The "sspi_cmd" command has been added to run SSPI commands for Nexus and Avant devices.
  - **Lattice Synthesis Engine (LSE)** – LSE now supports inference of byte write enable True Dual-Port RAM.
  - **License** – The license support has been updated for various MachXO5-NX devices. Refer to the **Supported Devices** table on page 3 for more information.
  - **Low Power Support** – Dynamic Clock Control (DCC) has been added to support low power reduction in the LSE tool and MAP. This functionality is currently available as a Beta feature in this release.
  - **Power Calculator** – The "(DPM)" text has been added in the Power Summary tab to support the table title Dynamic Power Multiplier.

- **Physical Designer** – The "Resource Usage Count" and "Selected Resource Usage Count" sections are now in the Create GROUP dialog box of Physical Designer, showing the total resource count for all instances.
- **Place and Route (PAR)**
  - The Physical Synthesis option has been integrated into Place and Route flow. This functionality is currently available as a Beta feature in this release.
  - The QoR improvement option “nexus_extreme” has been added to the PAR command line for Nexus devices. When enabled, the placement engine switches from Simulated Annealing (SA) to Analytical Placer (AP). AP can run faster with better timing results. This option is currently available as a Beta feature in this release.
- **Reports**
  - The "Parameter Settings" section has been added to Synthesis Reports, displaying parameters for each instance when the design includes entities with parameters. This feature is available only for LSE.
  - The “Stage Execution Time Summary” section has been added to the Project Summary.
  - The resource usage percentage has been added to the Report Summary.
- **Reveal**
  - Support for incremental flow has been added to the post-par Reveal stage.
  - The interface for setting up virtual switch/LED signals has been enhanced for ordering and color coding.
  - A captured waveform can now be saved as an RVA file and reloaded when Reveal Analyzer is reopened.
  - Support for memory controller debug for Avant devices has been added to diagnose and resolve DDR interface issues.
- **Strategies**
  - The “Set VIRTUAL IO on all ports” strategy has been added to strategy settings. This option adds virtual IO information to MAP reports when enabled.
  - The “Use DCC Insertion” option has been added to LSE options to support low power reduction.
- **TCL Console**
  - The Radiant TCL console (radiantc) now supports argument handling.

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, it may be necessary to re-create some IP, per the procedures described in the following table.

These procedures adapt the project for the changes in Radiant software.

Versions	IP Regeneration Procedures		
	Avant (LAV-AT)	**CrossLink-NX (LIFCL), Certus-N2 (LN2-CT-ES), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP), MachXO5-NX (LFMXO5)**	
2025.1	MPPHY	PLL	These IP used in designs created in Radiant 2024.2.1 or earlier must be re-generated in Radiant 2025.1.
	PLL	DDR_MEM	
	SEDC	MIPI_DPHY	
		MPCS	

Supported Devices

Lattice Radiant software can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
iCE40 UltraPlus (iCE40UP)	◀	
Lattice Avant (LAV-AT)		◀

Device Family	Free License	Subscription License
CertusPro™-NX (LFCPNX)	Evaluation Mode	◄
Certus-NX (LFD2NX)	◄	
Certus-N2 (LN2-CT-ES)		◄
MachXO5-NX (LFMXO5-25)	◄	
MachXO5-NX (LFMXO5-100T)	Evaluation Mode	◄
MachXO5-NX (LFMXO5-35)	◄	
MachXO5-NX (LFMXO5-35T)	Evaluation Mode	◄
MachXO5-NX (LFMXO5-65)	◄	
MachXO5-NX (LFMXO5-65T)	Evaluation Mode	◄
MachXO5-NX (LFMXO5-15D)[1]		◄
CrossLink-NX (LIFCL)	◄	
CrossLink-NX (LIFCL-33U)	Evaluation Mode	◄
Certus™-NX-RT (UT24C)		◄
CertusPro™-NX-RT (UT24CP)		◄

Note:

1. To enable this device, please submit a support ticket.

Support for Third-Party Synthesis and Simulator Tools

The Synopsys Synplify Pro® for Lattice synthesis tool and the Siemens QuestaSim® Lattice Edition simulator tools are included in the Radiant software.

- **Synopsys Synplify Pro FPGA synthesis software version V-2023.09LR-3**
  - Release Notes for Synplify Pro are located in ..\<*install_directory*>\radiant\2025.1\synpbase\doc\. The file name is release_notes.pdf.
  - A full set of documents for Synplify Pro are also located in \<*install_directory*>\radiant\2025.1\synpbase\doc\.
- **Siemens QuestaSim Lattice Edition 2024.2**
  - Release Notes for QuestaSim Lattice Edition are located in <install_directory>\radiant\2025.1\questasim\. The file names are RELEASE_NOTES.html or RELEASE_NOTES.txt.
  - A full set of documents for QuestaSim Lattice Edition are located in <install_directory>\radiant\2025.1\questasim\docs\pdfdocs.
- **Siemens Questa® 2022.3**
- **Cadence Xcelium® 23.03.003**
- **Synopsys VCS® U-2023.03-SP2**

Help Resources

- Online Help updated with CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP), and Lattice Avant (LAV-AT) content.
- To view the Online Help, start the Lattice Radiant software and select the 

"Getting Started" icon under Information Center.

  Note: The Firefox Snap install is not supported if you are using Ubuntu 20.04 or 18.04 to access the Radiant Help. This is a result of the snap install's inability to open local HTML pages. You may reinstall the latest version of Firefox using Apt install. For installation instructions, please refer to this guide.

System Requirements

The following shows the basic system requirements for Radiant software:

- Intel x86 64-bit or 64-bit-compatible PC
- OS Support:

64-bit OS	Radiant	Synplify Pro	QuestaSim
Windows 10	✓	✓	✓
Windows 11	✓	✓*	✓*
Red Hat Enterprise Linux 7.9	✓	✓	✓
Red Hat Enterprise Linux 8.10	✓	✓	✓
Ubuntu version 20.04 LTS	✓	✓*	✓*
Ubuntu version 22.04 LTS	✓	✓*	✓*

***Note**: The third-party tools have been tested by Lattice on the listed platforms, but the vendors do not officially support them.

- Approximately 50GB free disk space
- Computer Memory Requirement:
  - Nexus – 16GB
  - LAV-AT– 32GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.
- 1024 X 768 graphics display
- Network adapter for license and network connectivity
- A Web browser with JavaScript capability
- Acrobat Reader

Issues Fixed in this Release

The following known issues are fixed in this release. Their workarounds are no longer needed.

Place & Route error occurs when two MIPI_DPHY Tx are instantiated on the same bank.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-26196

Place & Route fails to complete PGROUP placement when instance is located in macro region.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-25945

The VOLTAGE_ALARM_EN feature is not currently displayed in the "feature row" readback within the Programmer tool.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-25737

Place & Route issue with SW version 2024.2 causing hardware failure in iCE40UP devices.

Devices affected: iCE40 UltraPlus (iCE40UP)

Bug number: DNG-25165

Potential Synplify synthesis crash in Avant projects that include LPDDR4.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-24791

The datasheet link for the Certus-N2 device is incorrect.

Devices affected: Certus-N2 (LN2-CT)

Bug number: DNG-24786

The expected behavior of Write Enable in a FIFO/EBR for Avant Simulation models was not captured with the WrEn assertion.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-24347

The DDRPHY64D, DDRPHY64E, and DDRPHY72D primitives are incompatible with the LN2-CT-20 device.

Devices affected: Certus-N2 (LN2-CT)

Bug number: DNG-24598

Synplify Pro incorrectly removes virtual wire signals that were preserved using the "syn_rvl_debug" attribute.

Devices affected: All devices

Bug number: DNG-21236

Synplify Pro fails in FSM with initial value case and reports an error instead of a warning.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-24118

Synplify Pro does not report an error or warning for clocks that are driven by logic.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-21048

The PDPSC32K primitive does not have an output path despite outreg being used.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20772

When using Synplify Pro, you may encounter the following error during macro reuse: “Synthesis exit by 9. Child process exited abnormally. Done: error code 1.”

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20116

IBIS reports I/O models of some sysCONFIG pins even if they are used as GPIO.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19646

Cannot assign input ports as MIPI_DPHY type for Avant.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19199

Known Issues for Radiant 2025.1

The following are known issues for Radiant Software 2025.1. For assistance with these issues, please contact Lattice Technical support.

Standalone Timing Analyzer results may differ from RunSTA results, even when using the same pdc file.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-27523

Avant designs using DDR may fail routing with the error: "ERROR <71001187> - netcheck: Signal <signal> partially routed under the following conditions.

- **One ECLK is driving many GDDR IOs that require more two IO banks**
- **User specifies a placement constraint such as ldc_set_location -bank {4} [get_ports clk_i]**

Workaround: Manually lockdown the driver to the clock pin in the bank instead of using "bank" constraint (e.g.: ldc_set_location -site AF6 [get_ports clk_i]).

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-27454

When using Reveal, Synplify Pro may issue an error: "ERROR <2019992> - Error in encrypted block" related to the generated Reveal verilog file.

Workaround: Contact Lattice technical support.

Devices affected: All devices

Bug number: DNG-27465

For Avant designs when placing CE and SR with different polarities on the same SLICE, placement may fail.

Workaround: Modify the design to eliminate the use of register control signals with both positive and negative polarities. For instance, generate a new signal to inverse the polarity and use that signal.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-25568

Timing Analysis for CDC paths may be incorrect if the following conditions are met:

- **PLL has a phase shifted clock**
- **User defined PLL output clock constraints**
- **There is a CDC path with the phase shifted PLL clock**

Workaround: Let the timing engine define the generated clock of the PLL's phase shifted clocks.

Device affected: All devices

Bug number: DNG-27414

Timing analysis and the Tcl command “sta_get_slack -worst” may return different worst slack values.

The command may return a slack value, but it might not be the worst-case slack. The returned slack is valid, but it corresponds to a path that does not represent the worst slack.

In addition, the detailed timing report may contain some arrival values that are incorrect. However, the path of the report, the delays of the connections and arcs along the path, the required value, the arrival value used for slack computation, and the slack of the path are all correct.

Device affected: All devices

Bug number: DNG-27408

Setting the FIFO DC “Controller Implementation” parameter to “Area-Optimized (HW)” is not functional due to an issue in the E70ES1 device.

Workaround: Use the Feature-Rich (LUT) option under Controller Implementation.

Device affected: Lattice Avant (LAV-AT-ES1)

Bug number: DNG-27444

MPPHY IP pma_rx*_blk_lock_o status port toggles using Near End Parallel Loopback.

Workaround: When using this loopback, update the following parameter values in the generated top level RTL file:

PHY_TX2RX_LPBK_RX_MPPCS_CLK_SEL_L* = “0b1”;

PHY_TX2RX_LPBK_RX_PCS_CLK_SEL_L* = “0b1”;

PHY_TX2RX_LPBK_RX_SERDES_CLK_SEL_L* = “0b1”;

Device affected: Lattice Avant (LAV-AT)

Bug number: DNG-27445

The bitstream hardware data status of LFD2NX-35/65 is missing.

The bitstream hardware data status is Preliminary.

Devices affected: Certus-NX (LFD2NX-35, LFD2NX-65)

Bug number: DNG-26738

The power file revision is shown as advanced in LFMXO5-35/35T/65/65T devices.

The power file revision should be Preliminary.

Devices affected: MachXO5-NX (LFMXO5-35, LFMXO5-35T, LFMXO5-65, LFMXO5-65T)

Bug number: DNG-26755

Incorrect number of PIOs shown in the Device Selector Window for LFD2NX-35/65 CABGA400 packages.

The correct PIO count should be 307.

Devices affected: Certus-NX (LFD2NX-35, LFD2NX-65)

Bug number: DNG-27120

The location for a secured component (Hard DPHY) cannot be changed.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-24746

Unsupported components may still pass synthesis when using both Synplify Pro and LSE.

SEDCA, UMXSPI, and UXSPI are not available for the E30ES device, but the synthesis step in Radiant project flow may still pass.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-24562

IDDRX2 has exceptionally large C2INP_DEL value.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-24167

CONFIG_LMMIE and CONFIG_LMMIB RTL simulation fails.

Devices affected: MachXO5-NX (LFMXO5)

Bug number: DNG-22187

The clock, using pclk routing and connected only to fabric registers, has a lower clock MPW at the higher speed grade (-8).

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-21315

The “Trace_Length” and “Package_Delay” data of LFD2NX-9/17's CABGA196 package is missing in the .pkt file.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-23568

Clock mismatch in Generic/PCS bypass configurations causing simulation failures when using MPPHY (IP, Generic G8B10B, X1_5X4, G70).

Device affected: Lattice Avant (LAV-AT)

Bug number: DNG-23343

Power Calculator resource usage reporting is incorrect.

The report shows that MPP is utilized at 100% regardless of the number of lanes used, due to the current power modeling treating the entire IP as a single unit.

Device affected: Lattice Avant (LAV-AT)

Bug number: DNG-23785

You may encounter an issue with CONFIG_LMMI and CONFIG_LMMA's lmmi_ready signal during simulation.

Devices affected: Certus-NX (LFD2NX), CrossLink-NX (LIFCL)

Bug number: DNG-20717

CONFIG_LMMI RTL simulation error occurs and data missing in output ports.

Devices affected: Certus-NX (LFD2NX), CrossLink-NX (LIFCL)

Bug number: DNG-20543

Synplify Pro does not correctly process macro creation constraints with escape characters.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-20134

Simulation with XCELIUM may fail when simulating projects using the CNTL_LR_U_POWER primitive due to incorrect compilation order of cmpl_libs.

Devices affected: CrossLink-NX (LIFCL-33U)

Bug number: DNG-19623

Reveal Power-on Reset (POR) Debug function does not work when using LSE with only one Trigger Unit (TU).

Workaround: Add another Trigger Unit (TU) that can be unrelated to POR Debug.

Devices affected: All devices except iCE40UP

Bug number: DNG-13901

The CSI-2/DSI D-PHY Transmitter and Receiver Soft IP simulations fail when using Synopsys VCS as simulation tool.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-13225

Post-route simulation error when using GDDR for Nexus devices due to parameters not being passed correctly from the original RTL.

Workaround: Intrinsic delay similar to the delay value on the vo.vo file needs to be added to the IP testbench.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-9639

MAP incorrectly reports number of DPHY and PCIE/ADC resources for CrossLink-NX (LIFCL) QFN72 package.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-8297