JESD204B Driver API Reference

Technical Note

FPGA-TN-02412-1.1

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This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
ADC	Analog-to-Digital Converter
API	Application Programming Interface
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
FPGA	Field Programmable Gate Array
ID	Identification
ILA	Initial Lane Alignment
IP	Intellectual Property
LMFC	Local Multi-Frame Clock
LVDS	Low-Voltage Differential Signaling
Rx	Receiver
Tx	Transmitter

1. Introduction

JESD204B is a high-speed serial interface used between data converters, such as analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), and the FPGA device to replace traditional interfaces, such as CMOS and LVDS. With converter sampling rates and data throughput increasing, the JESD204B interface offers advantages in terms of size, cost, and speed.

Refer to the JESD204B IP User Guide (FPGA-IPUG-02259) for more details about the IP core.

1.1. Purpose

This document is intended to act as a reference guide for developers by providing details of the C language driver APIs and function call flows.

1.2. Audience

The intended audience for this document includes embedded system designers and embedded software developers using the Lattice CertusPro™-NX device. The technical guide assumes readers have expertise in embedded systems and FPGA technologies.

1.3. Driver Version

JESD204B_DRV_VER “25.02.00”

1.4. Driver and IP Compatibility

Driver Version	IP Version
25.02.00	1.3.0

Refer to the JESD204B IP Release Notes (FPGA-RN-02006) for more information on the driver and IP versions.

2. API Description

2.1. jesd204b_tx_init()

This API is used to set up the JESD204B transmitter (Tx) by assigning the base address to the provided handle.

```
unsigned char jesd204b_tx_init(jesd_handle_t *handle, unsigned int base_addr)
```

In/Out	Parameter	Description	Returns
In	handle	Handle of the struct jesd_handle_t.	0: Success 1: Failure
In	base_addr	Base address to be assigned to Tx.	

2.2. jesd204b_rx_init()

This API is used to set up the JESD204B receiver (Rx) by assigning the base address to the provided handle.

```
unsigned char jesd204b_rx_init(jesd_handle_t *handle, unsigned int base_addr)
```

In/Out	Parameter	Description	Returns
In	handle	Handle of the struct jesd_handle_t.	0: Success 1: Failure
In	base_addr	Base address to be assigned to Rx.	

2.3. set_tx_config_reg_bit()

This API is used to modify a specific bit in the JESD204B Tx configuration register based on the provided index and value. It validates the input parameters and ensures the data written does not exceed the allowed width for the specified bit.

```
unsigned char set_tx_config_reg_bit(jesd_handle_t *handle, unsigned int reg, unsigned
int val)
```

In/Out	Parameter	Description	Returns
In	handle	Handle of the struct jesd_handle_t.	0: Success 1: Failure
In	reg	Encoded register information: Bits [31:16] – Width of the bit field Bits [15:8] – Bit position of the field Bits [7:0] – Register offset Refer to Table 5.1 for the encoded registers from TX_CORE_RST to TX_ILA_FCHK_L7.	
In	val	Data to be written.	

2.4. get_tx_config_reg_bit()

This function reads a specific bit or field from the JESD204B Tx configuration registers based on the provided index. The value is returned through the *val* pointer.

```
unsigned char get_tx_config_reg_bit(jesd_handle_t *handle, unsigned int reg, unsigned
int val)
```

In/Out	Parameter	Description	Returns
In	Handle	Handle of the struct jesd_handle_t.	0: Success

In/Out	Parameter	Description	Returns
In	reg	Encoded register information: Bits [31:16] – Width of the bit field Bits [15:8] – Bit position of the field Bits [7:0] – Register offset Refer to Table 5.1 for the encoded registers from TX_CORE_RST to TX_ILA_FCHK_L7.	1: Failure
In	val	Data to be read.	

2.5. set_rx_config_reg_bit()

This API is used to modify a specific bit in the JESD204B Rx configuration register based on the provided index and value. It validates the input parameters and ensures the data written does not exceed the allowed width for the specified bit.

```
unsigned char set_rx_config_reg_bit(jesd_handle_t *handle, unsigned int reg, unsigned int val)
```

In/Out	Parameter	Description	Returns
In	handle	Handle of the struct jesd_handle_t.	0: Success 1: Failure
In	reg	Encoded register information: Bits [31:16] – Width of the bit field Bits [15:8] – Bit position of the field Bits [7:0] – Register offset Refer to Table 5.1 for the encoded registers from RX_CORE_RST to RX_BUFF_FILL_LVL.	
In	val	Data to be written.	

2.6. get_rx_config_reg_bit()

This function reads a specific bit from the Rx configuration registers based on the provided index. It determines the appropriate register and bit to read based on the index and returns the value through the provided pointer.

```
unsigned char get_rx_config_reg_bit(jesd_handle_t *handle, unsigned int reg, unsigned int val)
```

In/Out	Parameter	Description	Returns
In	handle	Handle of the struct jesd_handle_t.	0: Success 1: Failure
In	reg	Encoded register information: Bits [31:16] – Width of the bit field Bits [15:8] – Bit position of the field Bits [7:0] – Register offset Refer to Table 5.1 for the encoded registers from RX_CORE_RST to RX_BUFF_FILL_LVL.	
In	val	Data to be read.	

3. Function Call Flow Diagrams

3.1. jesd204b_tx_init()

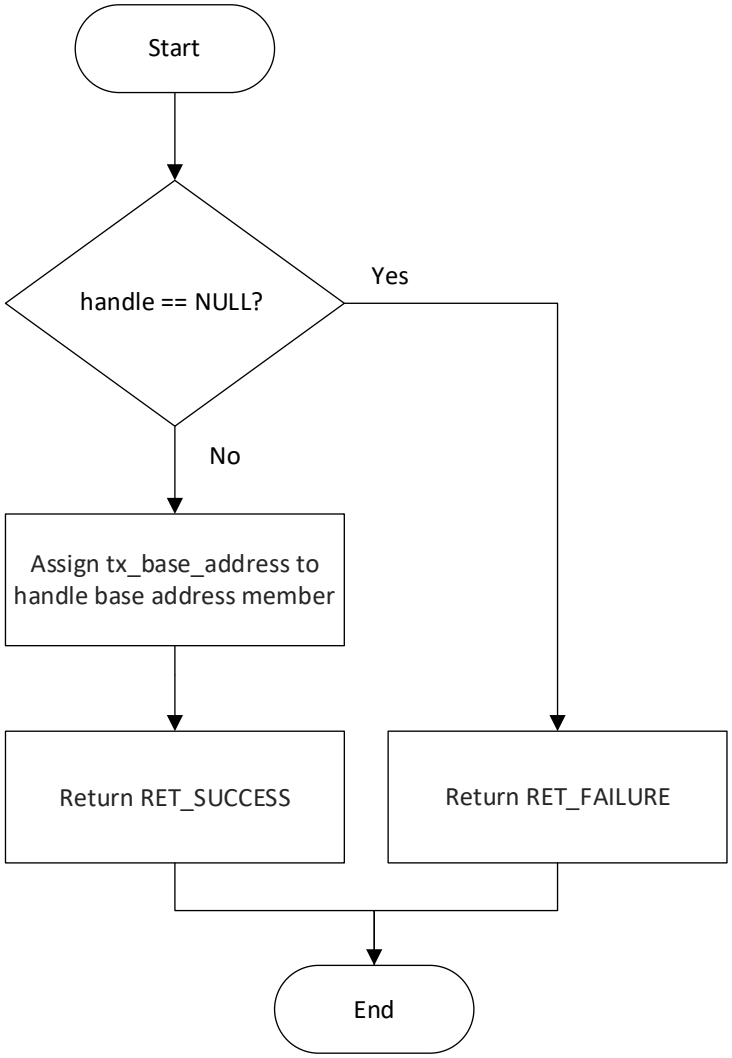

Figure 3.1. unsigned char jesd204b_tx_init()

3.2. jesd204b_rx_init()

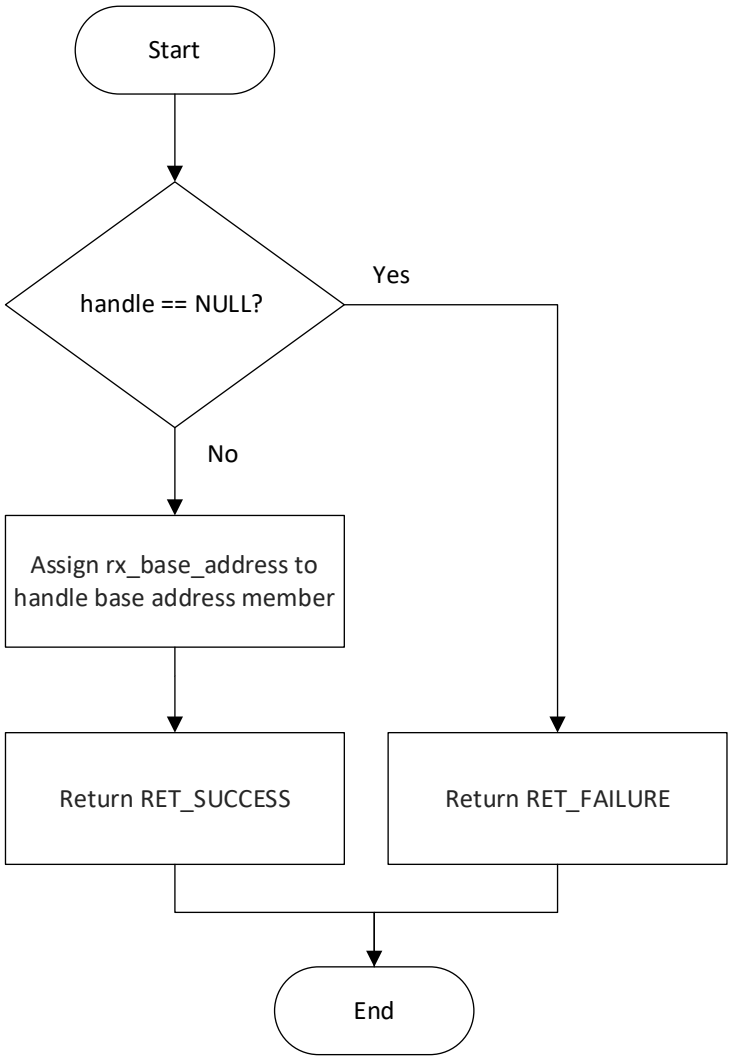

Figure 3.2. unsigned char jesd204b_rx_init()

3.3. set_tx_config_reg_bit()

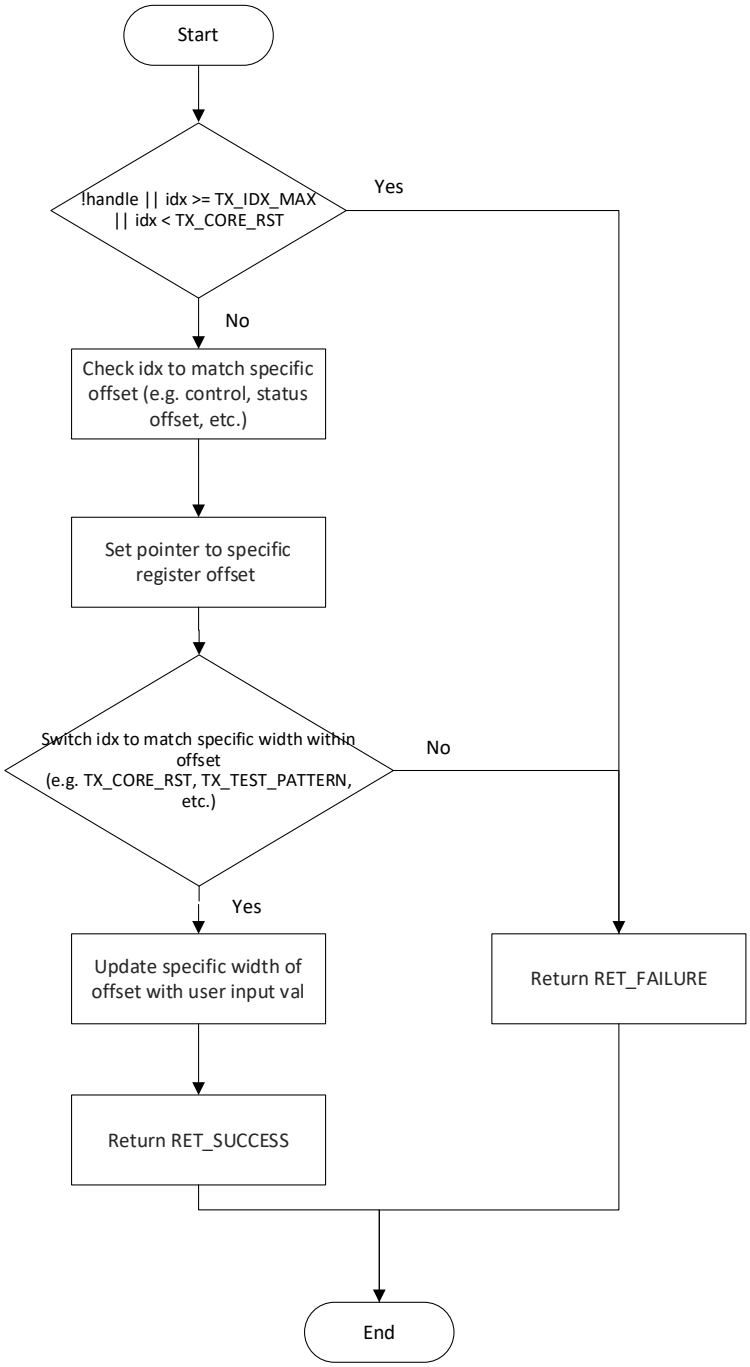

Figure 3.3. unsigned char set_tx_config_reg_bit()

3.4. get_tx_config_reg_bit()

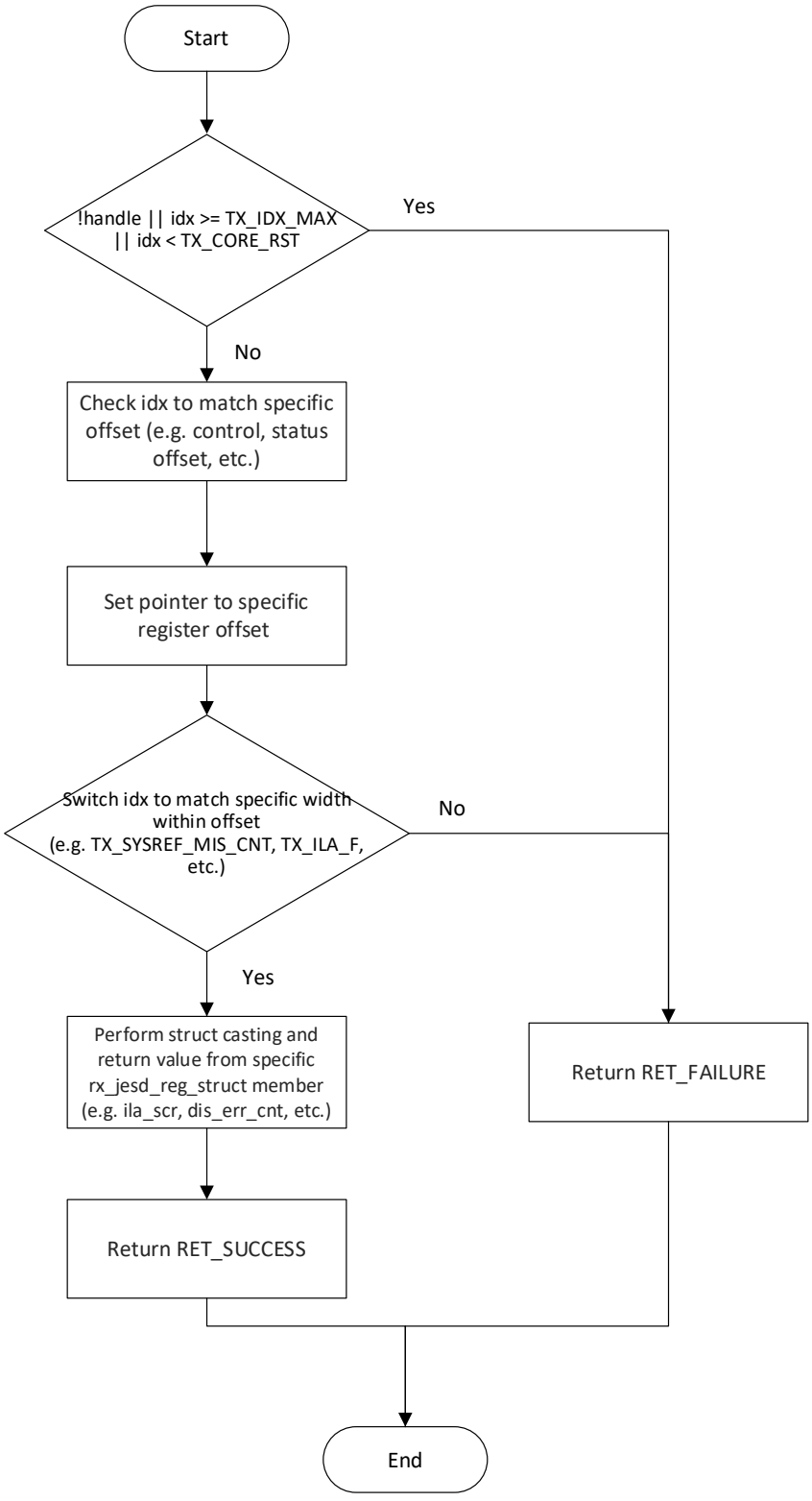

Figure 3.4. unsigned char get_tx_config_reg_bit()

3.5. set_rx_config_reg_bit()

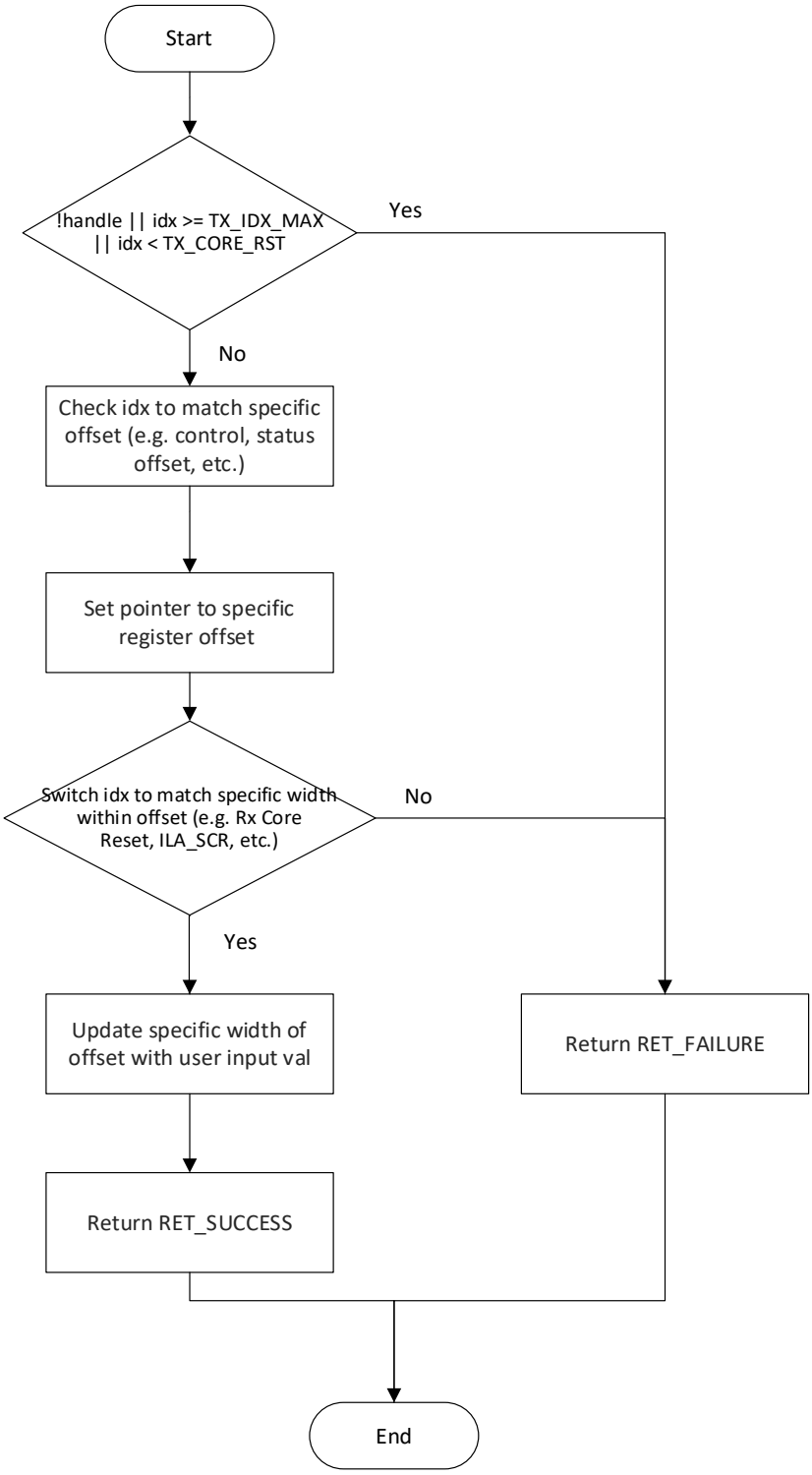

Figure 3.5. unsigned char set_rx_config_reg_bit()

3.6. get_rx_config_reg_bit()

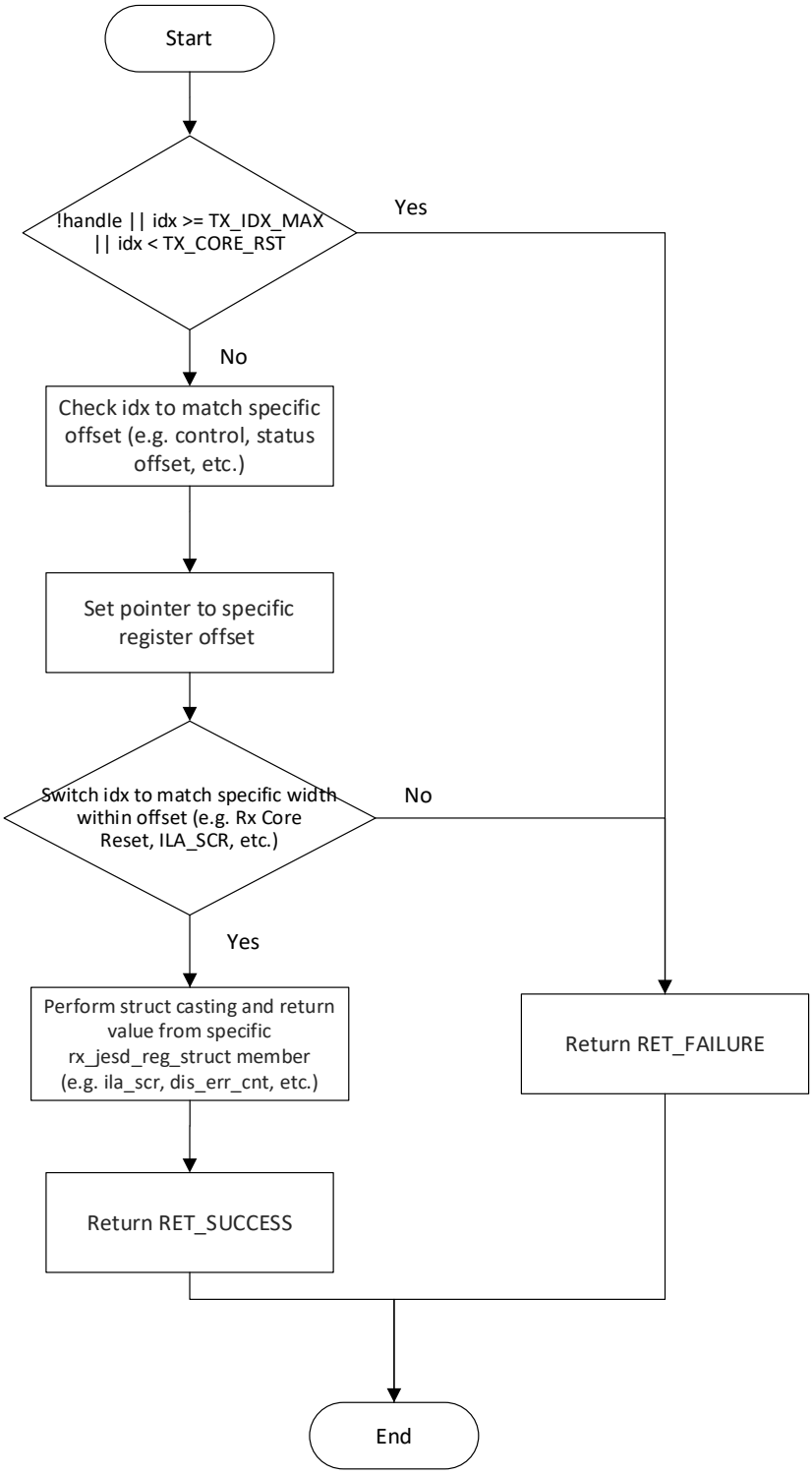

Figure 3.6. unsigned char get_rx_config_reg_bit()

4. API Data Structures

4.1. struct jesd_handle_t

Table 4.1. jesd_handle_t Parameters

Data Type	Struct Member	Description
unsigned int	tx_base_addr	Base address of Tx
unsigned int	rx_base_addr	Base address of Rx

5. API Macros

Table 5.1. API Macros Description

Macro	Description
#define JESD204B_DRV_VER	JESD204B driver version
#define RET_SUCCESS	Return value of success status
#define RET_FAILURE	Return value of failure status
#define TX_CONTROL_REG_OFFSET_STRT	Transmitter control register base offset
#define TX_STATUS_REG_OFFSET_STRT	Transmitter status register offset
#define TX_TEST_MODE_REG_OFFSET_STRT	Transmitter test mode register offset
#define TX_LINK_CFG_0_REG_OFFSET_STRT	Transmitter link configuration register 0 offset
#define TX_LINK_CFG_1_REG_OFFSET_STRT	Transmitter link configuration register 1 offset
#define TX_LINK_CFG_2_REG_OFFSET_STRT	Transmitter link configuration register 2 offset
#define TX_LINK_CFG_3_REG_OFFSET_STRT	Transmitter link configuration register 3 offset
#define TX_LINK_CFG_4_REG_OFFSET_STRT	Transmitter link configuration register 4 offset
#define TX_LINK_CFG_5_REG_OFFSET_STRT	Transmitter link configuration register 5 offset
#define TX_LINK_CFG_6_REG_OFFSET_STRT	Transmitter link configuration register 6 offset
#define TX_LINK_CFG_7_REG_OFFSET_STRT	Transmitter link configuration register 7 offset
#define TX_CORE_RST_WIDTH	Core reset field width mask
#define TX_SYSREF_MASK_WIDTH	System reference mask field width
#define TX_SYSREF_EN_WIDTH	System reference enable field width
#define TX_LMFC_BUFF_ADJ_WIDTH	LMFC buffer adjustment field width
#define TX_LINK_STATE_WIDTH	Link state field width
#define TX_SYSREF_CAPTURED_WIDTH	System reference captured flag width
#define TX_PHY_READY_WIDTH	Physical layer ready flag width
#define TX_SYSREF_MIS_CNT_WIDTH	System reference miss count field width
#define TX_TEST_PATTERN_WIDTH	Test pattern selection field width
#define TX_ILA_DID_WIDTH	Device ID field width
#define TX_ILA_BID_WIDTH	Bank ID field width
#define TX_ILA_ADJCNT_WIDTH	Adjustment count field width
#define TX_ILA_PHADJ_WIDTH	Phase adjustment field width
#define TX_ILA_ADJDIR_WIDTH	Adjustment direction field width
#define TX_ILA_L_WIDTH	Number of lanes minus 1 field width
#define TX_ILA_SCR_WIDTH	Scrambling enable field width
#define TX_ILA_F_WIDTH	Octets per frame minus 1 field width
#define TX_ILA_K_WIDTH	Frames per multiframe minus 1 field width
#define TX_ILA_M_WIDTH	Number of converters minus 1 field width
#define TX_ILA_N_WIDTH	Converter resolution minus 1 field width
#define TX_ILA_CS_WIDTH	Control bits per sample field width
#define TX_ILA_Nt_WIDTH	Total bits per sample minus 1 field width
#define TX_ILA_SUBCLASSV_WIDTH	Subclass version field width
#define TX_ILA_S_WIDTH	Number of samples per converter per frame minus 1 field width
#define TX_ILA_JESDV_WIDTH	JESD204 version field width
#define TX_ILA_CF_WIDTH	Control words per frame clock period minus 1 field width
#define TX_ILS_HD_WIDTH	High density format field width
#define TX_OCT_PER_MUL_FR_WIDTH	Octets per multiframe field width
#define TX_MUL_FR_ILA_SEQ_WIDTH	Multiframe initial lane alignment sequence field width
#define TX_ILA_LID_FCHK_WIDTH	Lane ID and frame checksum field width

Macro	Description
#define TX_CORE_RST_BIT_POS	Core reset bit position
#define TX_SYSREF_EN_BIT_POS	System reference enable bit position
#define TX_SYSREF_MASK_BIT_POS	System reference mask bit position
#define TX_LMFC_BUFF_ADJ_BIT_POS	LMFC buffer adjustment bit position
#define TX_LINK_STATE_BIT_POS	Link state bit position
#define TX_SYSREF_CAPTURED_BIT_POS	System reference captured bit position
#define TX_PHY_READY_BIT_POS	Physical layer ready bit position
#define TX_SYSREF_MIS_CNT_BIT_POS	System reference miss count bit position
#define TX_TEST_PATTERN_BIT_POS	Test pattern selection bit position
#define TX_ILA_DID_BIT_POS	Device ID bit position
#define TX_ILA_BID_BIT_POS	Bank ID bit position
#define TX_ILA_ADJCNT_BIT_POS	Adjustment count bit position
#define TX_ILA_PHADJ_BIT_POS	Phase adjustment bit position
#define TX_ILA_ADJDIR_BIT_POS	Adjustment direction bit position
#define TX_ILA_L_BIT_POS	Number of lanes minus 1 bit position
#define TX_ILA_SCR_BIT_POS	Scrambling enable bit position
#define TX_ILA_F_BIT_POS	Octets per frame minus 1 bit position
#define TX_ILA_K_BIT_POS	Frames per multiframe minus 1 bit position
#define TX_ILA_M_BIT_POS	Number of converters minus 1 bit position
#define TX_ILA_N_BIT_POS	Converter resolution minus 1 bit position
#define TX_ILA_CS_BIT_POS	Control bits per sample bit position
#define TX_ILA_Nt_BIT_POS	Total bits per sample minus 1 bit position
#define TX_ILA_SUBCLASSV_BIT_POS	Subclass version bit position
#define TX_ILA_S_BIT_POS	Number of samples per converter per frame minus 1 bit position
#define TX_ILA_JESDV_BIT_POS	JESD204 version bit position
#define TX_ILA_CF_BIT_POS	Control words per frame clock period minus 1 bit position
#define TX_ILS_HD_BIT_POS	High density format bit position
#define TX_OCT_PER_MUL_FR_BIT_POS	Octets per multiframe bit position
#define TX_MUL_FR_ILA_SEQ_BIT_POS	Multiframe initial lane alignment sequence bit position
#define TX_ILA_LID_L0_BIT_POS	Lane 0 ID bit position
#define TX_ILA_LID_L1_BIT_POS	Lane 1 ID bit position
#define TX_ILA_LID_L2_BIT_POS	Lane 2 ID bit position
#define TX_ILA_LID_L3_BIT_POS	Lane 3 ID bit position
#define TX_ILA_LID_L4_BIT_POS	Lane 4 ID bit position
#define TX_ILA_LID_L5_BIT_POS	Lane 5 ID bit position
#define TX_ILA_LID_L6_BIT_POS	Lane 6 ID bit position
#define TX_ILA_LID_L7_BIT_POS	Lane 7 ID bit position
#define TX_ILA_FCHK_L0_BIT_POS	Lane 0 frame checksum bit position
#define TX_ILA_FCHK_L1_BIT_POS	Lane 1 frame checksum bit position
#define TX_ILA_FCHK_L2_BIT_POS	Lane 2 frame checksum bit position
#define TX_ILA_FCHK_L3_BIT_POS	Lane 3 frame checksum bit position
#define TX_ILA_FCHK_L4_BIT_POS	Lane 4 frame checksum bit position
#define TX_ILA_FCHK_L5_BIT_POS	Lane 5 frame checksum bit position
#define TX_ILA_FCHK_L6_BIT_POS	Lane 6 frame checksum bit position
#define TX_ILA_FCHK_L7_BIT_POS	Lane 7 frame checksum bit position
#define TX_CORE_RST	Core reset control field
#define TX_SYSREF_EN	System reference enable control field

Macro	Description
#define TX_SYSREF_MASK	System reference mask control field
#define TX_LMFC_BUFF_ADJ	LMFC buffer adjustment control field
#define TX_LINK_STATE	Current link state status field
#define TX_SYSREF_CAPTURED	System reference captured status field
#define TX_PHY_READY	Physical layer ready status field
#define TX_SYSREF_MIS_CNT	System reference miss count status field
#define TX_TEST_PATTERN	Test pattern selection field
#define TX_ILA_DID	Device ID configuration field
#define TX_ILA_BID	Bank ID configuration field
#define TX_ILA_ADJCNT	Adjustment count configuration field
#define TX_ILA_PHADJ	Phase adjustment configuration field
#define TX_ILA_ADJDIR	Adjustment direction configuration field
#define TX_ILA_L	Number of lanes minus 1 configuration field
#define TX_ILA_SCR	Scrambling enable configuration field
#define TX_ILA_F	Octets per frame minus 1 configuration field
#define TX_ILA_K	Frames per multiframe minus 1 configuration field
#define TX_ILA_M	Number of converters minus 1 configuration field
#define TX_ILA_N	Converter resolution minus 1 configuration field
#define TX_ILA_CS	Control bits per sample configuration field
#define TX_ILA_Nt	Total bits per sample minus 1 configuration field
#define TX_ILA_SUBCLASSV	Subclass version configuration field
#define TX_ILA_S	Number of samples per converter per frame minus 1 configuration field
#define TX_ILA_JESDV	JESD204 version configuration field
#define TX_ILA_CF	Control words per frame clock period minus 1 configuration field
#define TX_ILS_HD	High density format configuration field
#define TX_OCT_PER_MUL_FR	Octets per multiframe configuration field
#define TX_MUL_FR_ILA_SEQ	Multiframe initial lane alignment sequence configuration field
#define TX_ILA_LID_L0	Lane 0 ID configuration field
#define TX_ILA_LID_L1	Lane 1 ID configuration field
#define TX_ILA_LID_L2	Lane 2 ID configuration field
#define TX_ILA_LID_L3	Lane 3 ID configuration field
#define TX_ILA_LID_L4	Lane 4 ID configuration field
#define TX_ILA_LID_L5	Lane 5 ID configuration field
#define TX_ILA_LID_L6	Lane 6 ID configuration field
#define TX_ILA_LID_L7	Lane 7 ID configuration field
#define TX_ILA_FCHK_L0	Lane 0 frame checksum configuration field
#define TX_ILA_FCHK_L1	Lane 1 frame checksum configuration field
#define TX_ILA_FCHK_L2	Lane 2 frame checksum configuration field
#define TX_ILA_FCHK_L3	Lane 3 frame checksum configuration field
#define TX_ILA_FCHK_L4	Lane 4 frame checksum configuration field
#define TX_ILA_FCHK_L5	Lane 5 frame checksum configuration field
#define TX_ILA_FCHK_L6	Lane 6 frame checksum configuration field
#define TX_ILA_FCHK_L7	Lane 7 frame checksum configuration field
#define RX_CONTROL_REG_OFFSET_STRT	Receiver control register base offset
#define RX_STATUS_REG_OFFSET_STRT	Receiver status register offset
#define RX_ERR_STATUS_REG_OFFSET_STRT	Receiver error status register offset

Macro	Description
#define RX_LINK_CFG_0_REG_OFFSET_STRT	Receiver link configuration register 0 offset
#define RX_LINK_CFG_1_REG_OFFSET_STRT	Receiver link configuration register 1 offset
#define RX_LINK_CFG_2_REG_OFFSET_STRT	Receiver link configuration register 2 offset
#define RX_LINK_CFG_3_REG_OFFSET_STRT	Receiver link configuration register 3 offset
#define RX_LINK_CFG_4_REG_OFFSET_STRT	Receiver link configuration register 4 offset (Lane ID L0-L3)
#define RX_LINK_CFG_5_REG_OFFSET_STRT	Receiver link configuration register 5 offset (Lane ID L4-L7)
#define RX_LINK_CFG_6_REG_OFFSET_STRT	Receiver link configuration register 6 offset (Frame Check L0-L3)
#define RX_LINK_CFG_7_REG_OFFSET_STRT	Receiver link configuration register 7 offset (Frame Check L4-L7)
#define RX_ERR_CNT_REG_OFFSET_STRT	Receiver error counter register offset
#define RX_BUFF_FILL_LVL_REG_OFFSET_STRT	Receiver buffer fill level register offset
#define RX_CORE_RST_WIDTH	Core reset field width mask
#define RX_CORE_REINIT_WIDTH	Core reinitialize field width mask
#define RX_SYSREF_EN_WIDTH	System reference enable field width
#define RX_SYSREF_MASK_WIDTH	System reference mask field width
#define RX_LMFC_BUFF_ADJ_WIDTH	LMFC buffer adjustment field width
#define RX_LINK_STATE_WIDTH	Link state field width
#define RX_SYSREF_CAPTURED_WIDTH	System reference captured flag width
#define RX_PHY_READY_WIDTH	Physical layer ready flag width
#define RX_SYSREF_MIS_CNT_WIDTH	System reference miss count field width
#define RX_DISPARITY_ERR_FLG_WIDTH	Disparity error flag field width
#define RX_NOT_IN_TABLE_ERR_FLG_WIDTH	Not-in-table error flag field width
#define RX_UNEXP_CTRL_CHAR_FLG_WIDTH	Unexpected control character error flag field width
#define RX_ERR_CNT_RD_CHN_SEL_WIDTH	Error counter read channel selection field width
#define RX_ILA_DID_WIDTH	Device ID field width
#define RX_ILA_BID_WIDTH	Bank ID field width
#define RX_ILA_ADJCNT_WIDTH	Adjustment count field width
#define RX_ILA_PHADJ_WIDTH	Phase adjustment field width
#define RX_ILA_ADJDIR_WIDTH	Adjustment direction field width
#define RX_ILA_L_WIDTH	Number of lanes minus 1 field width
#define RX_ILA_SCR_WIDTH	Scrambling enable field width
#define RX_ILA_F_WIDTH	Octets per frame minus 1 field width
#define RX_ILA_K_WIDTH	Frames per multiframe minus 1 field width
#define RX_ILA_M_WIDTH	Number of converters minus 1 field width
#define RX_ILA_N_WIDTH	Converter resolution minus 1 field width
#define RX_ILA_CS_WIDTH	Control bits per sample field width
#define RX_ILA_Nt_WIDTH	Total bits per sample minus 1 field width
#define RX_ILA_SUBCLASSV_WIDTH	Subclass version field width
#define RX_ILA_S_WIDTH	Number of samples per converter per frame minus 1 field width
#define RX_ILA_JESDV_WIDTH	JESD204 version field width
#define RX_ILA_CF_WIDTH	Control words per frame clock period minus 1 field width
#define RX_ILS_HD_WIDTH	High density format field width
#define RX_OCT_PER_MUL_FR_WIDTH	Octets per multiframe field width
#define RX_MUL_FR_ILA_SEQ_WIDTH	Multiframe initial lane alignment sequence field width
#define RX_ILA_LID_FCHK_ERR_CNT_WIDTH	Lane ID, frame checksum, and error counter field width
#define RX_BUFF_FILL_LEVEL_WIDTH	Buffer fill level field width

Macro	Description
#define RX_CORE_RST_BIT_POS	Core reset bit position
#define RX_CORE_REINIT_BIT_POS	Core reinitialize bit position
#define RX_SYSREF_EN_BIT_POS	System reference enable bit position
#define RX_SYSREF_MASK_BIT_POS	System reference mask bit position
#define RX_LMFC_BUFF_ADJ_BIT_POS	LMFC buffer adjustment bit position
#define RX_LINK_STATE_BIT_POS	Link state bit position
#define RX_SYSREF_CAPTURED_BIT_POS	System reference captured bit position
#define RX_PHY_READY_BIT_POS	Physical layer ready bit position
#define RX_SYSREF_MIS_CNT_BIT_POS	System reference miss count bit position
#define RX_DISPARITY_ERR_FLG_BIT_POS	Disparity error flag bit position
#define RX_NOT_IN_TABLE_ERR_FLG_BIT_POS	Not-in-table error flag bit position
#define RX_UNEXP_CTRL_CHAR_FLG_BIT_POS	Unexpected control character error flag bit position
#define RX_ERR_CNT_RD_CHN_SEL_BIT_POS	Error counter read channel selection bit position
#define RX_ILA_DID_BIT_POS	Device ID bit position
#define RX_ILA_BID_BIT_POS	Bank ID bit position
#define RX_ILA_ADJCNT_BIT_POS	Adjustment count bit position
#define RX_ILA_PHADJ_BIT_POS	Phase adjustment bit position
#define RX_ILA_ADJDIR_BIT_POS	Adjustment direction bit position
#define RX_ILA_L_BIT_POS	Number of lanes minus 1 bit position
#define RX_ILA_SCR_BIT_POS	Scrambling enable bit position
#define RX_ILA_F_BIT_POS	Octets per frame minus 1 bit position
#define RX_ILA_K_BIT_POS	Frames per multiframe minus 1 bit position
#define RX_ILA_M_BIT_POS	Number of converters minus 1 bit position
#define RX_ILA_N_BIT_POS	Converter resolution minus 1 bit position
#define RX_ILA_CS_BIT_POS	Control bits per sample bit position
#define RX_ILA_Nt_BIT_POS	Total bits per sample minus 1 bit position
#define RX_ILA_SUBCLASSV_BIT_POS	Subclass version bit position
#define RX_ILA_S_BIT_POS	Number of samples per converter per frame minus 1 bit position
#define RX_ILA_JESDV_BIT_POS	JESD204 version bit position
#define RX_ILA_CF_BIT_POS	Control words per frame clock period minus 1 bit position
#define RX_ILS_HD_BIT_POS	High density format bit position
#define RX_OCT_PER_MUL_FR_BIT_POS	Octets per multiframe bit position
#define RX_MUL_FR_ILA_SEQ_BIT_POS	Multiframe initial lane alignment sequence bit position
#define RX_ILA_LID_L0_BIT_POS	Lane 0 ID bit position
#define RX_ILA_LID_L1_BIT_POS	Lane 1 ID bit position
#define RX_ILA_LID_L2_BIT_POS	Lane 2 ID bit position
#define RX_ILA_LID_L3_BIT_POS	Lane 3 ID bit position
#define RX_ILA_LID_L4_BIT_POS	Lane 4 ID bit position
#define RX_ILA_LID_L5_BIT_POS	Lane 5 ID bit position
#define RX_ILA_LID_L6_BIT_POS	Lane 6 ID bit position
#define RX_ILA_LID_L7_BIT_POS	Lane 7 ID bit position
#define RX_ILA_FCHK_L0_BIT_POS	Lane 0 frame checksum bit position
#define RX_ILA_FCHK_L1_BIT_POS	Lane 1 frame checksum bit position
#define RX_ILA_FCHK_L2_BIT_POS	Lane 2 frame checksum bit position
#define RX_ILA_FCHK_L3_BIT_POS	Lane 3 frame checksum bit position
#define RX_ILA_FCHK_L4_BIT_POS	Lane 4 frame checksum bit position
#define RX_ILA_FCHK_L5_BIT_POS	Lane 5 frame checksum bit position

Macro	Description
#define RX_ILA_FCHK_L6_BIT_POS	Lane 6 frame checksum bit position
#define RX_ILA_FCHK_L7_BIT_POS	Lane 7 frame checksum bit position
#define RX_DISPARITY_ERR_CNT_BIT_POS	Disparity error counter bit position
#define RX_NT_IN_TABLE_ERR_CNT_BIT_POS	Not-in-table error counter bit position
#define RX_UNEXP_CTRL_CHAR_BIT_POS	Unexpected control character counter bit position
#define RX_BUFF_FILL_LVL_BIT_POS	Buffer fill level bit position
#define RX_CORE_RST	Core reset control field
#define RX_SYSREF_EN	System reference enable control field
#define RX_SYSREF_MASK	System reference mask control field
#define RX_CORE_REINIT	Core reinitialize control field
#define RX_LMFC_BUFF_ADJ	LMFC buffer adjustment control field
#define RX_LINK_STATE	Current link state status field
#define RX_SYSREF_CAPTURED	System reference captured status field
#define RX_PHY_READY	Physical layer ready status field
#define RX_SYSREF_MIS_CNT	System reference miss count status field
#define RX_DISPARITY_ERR_FLG	Disparity error flag status field
#define RX_NOT_IN_TABLE_ERR_FLG	Not-in-table error flag status field
#define RX_UNEXP_CTRL_CHAR_FLG	Unexpected control character error flag status field
#define RX_ERR_CNT_RD_CHN_SEL	Error counter read channel selection field
#define RX_ILA_DID	Device ID configuration field
#define RX_ILA_BID	Bank ID configuration field
#define RX_ILA_ADJCNT	Adjustment count configuration field
#define RX_ILA_PHADJ	Phase adjustment configuration field
#define RX_ILA_ADJDIR	Adjustment direction configuration field
#define RX_ILA_L	Number of lanes minus 1 configuration field
#define RX_ILA_SCR	Scrambling enable configuration field
#define RX_ILA_F	Octets per frame minus 1 configuration field
#define RX_ILA_K	Frames per multiframe minus 1 configuration field
#define RX_ILA_M	Number of converters minus 1 configuration field
#define RX_ILA_N	Converter resolution minus 1 configuration field
#define RX_ILA_CS	Control bits per sample configuration field
#define RX_ILA_Nt	Total bits per sample minus 1 configuration field
#define RX_ILA_SUBCLASSV	Subclass version field
#define RX_ILA_S	Number of samples per converter per frame minus 1 field
#define RX_ILA_JESDV	JESD204 version field
#define RX_ILA_CF	Control words per frame clock period minus field
#define RX_ILS_HD	High density format field
#define RX_OCT_PER_MUL_FR	Octets per multiframe field
#define RX_MUL_FR_ILA_SEQ	Multiframe initial lane alignment sequence field
#define RX_ILA_LID_L0	Lane 0 ID field
#define RX_ILA_LID_L1	Lane 1 ID field
#define RX_ILA_LID_L2	Lane 2 ID field
#define RX_ILA_LID_L3	Lane 3 ID field
#define RX_ILA_LID_L4	Lane 4 ID field
#define RX_ILA_LID_L5	Lane 5 ID field
#define RX_ILA_LID_L6	Lane 6 ID field
#define RX_ILA_LID_L7	Lane 7 ID field
#define RX_ILA_FCHK_L0	Lane 0 frame checksum field

Macro	Description
#define RX_ILA_FCHK_L1	Lane 1 frame checksum field
#define RX_ILA_FCHK_L2	Lane 2 frame checksum field
#define RX_ILA_FCHK_L3	Lane 3 frame checksum field
#define RX_ILA_FCHK_L4	Lane 4 frame checksum field
#define RX_ILA_FCHK_L5	Lane 5 frame checksum field
#define RX_ILA_FCHK_L6	Lane 6 frame checksum field
#define RX_ILA_FCHK_L7	Lane 7 frame checksum field
#define RX_DISPARITY_ERR_CNT	Disparity error counter field
#define RX_NT_IN_TABLE_ERR_CNT	Not-in-table error counter field
#define RX_UNEXP_CTRL_CHAR	Unexpected control character counter field
#define RX_BUFF_FILL_LVL	Buffer fill level field

References

- JESD204B IP User Guide (FPGA-IPUG-02259)
- JESD204B IP Release Notes (FPGA-RN-02006)
- CertusPro-NX web page
- JESD204B IP Core web page
- Lattice Radiant Software web page
- Lattice Propel Design Environment web page
- Lattice Solutions IP Cores web page
- Lattice Solutions Reference Designs web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.1, December 2025

Section	Change Summary
All	Made minor editorial changes.
Abbreviations in This Document	Removed *CGS*, *EOF*, *EOMF*, *JSPAT*, *RPAT*, *SOF*, and *SOMF*.
Introduction	• Updated driver version in the Driver Version section. • Updated driver version and IP version in the Driver and IP Compatibility section.
API Description	In the set_tx_config_reg_bit(), get_tx_config_reg_bit(), set_rx_config_reg_bit(), and get_rx_config_reg_bit() sections: • Updated parameter in code from idx to reg. • Removed idx parameter from table. • Added reg parameter to table.
API Data Structures	Removed the struct tx_reg_map_t, struct rx_reg_map_t, struct tx_cntl_reg_t, struct tx_sts_reg_t, struct tx_test_mode_reg_t, struct tx_link_conf_0_reg_t, struct tx_link_conf_1_reg_t, struct tx_link_conf_2_reg_t, struct tx_link_conf_3_reg_t, struct tx_link_conf_4_reg_t, struct tx_link_conf_5_reg_t, struct tx_link_conf_6_reg_t, struct tx_link_conf_7_reg_t, struct rx_cntl_reg_t, struct rx_sts_reg_t, struct rx_err_sts_reg_t, struct rx_link_conf_0_reg_t, struct rx_link_conf_1_reg_t, struct rx_link_conf_2_reg_t, struct rx_link_conf_3_reg_t, struct rx_link_conf_4_reg_t, struct rx_link_conf_5_reg_t, struct rx_link_conf_6_reg_t, struct rx_link_conf_7_reg_t, and struct rx_err_cnt_reg_t sections.
Union Data Structures	Removed section.
API Enum	Removed section.
API Macros	In Table 5.1. API Macros Description: • Removed macros #define TX_CORE_RST_WIDTH, #define TX_SYSREF_MASK_WIDTH, #define TX_SYSREF_EN_WIDTH, #define LMFC_BUFF_ADJ_WIDTH, #define TX_TEST_PATTERN_WIDTH, #define TX_SCRAMBLE_WIDTH, #define RX_CORE_RST_WIDTH, #define RX_CODE_REINIT_WIDTH, #define RX_SYSREF_MASK_WIDTH, #define RX_SYSREF_EN_WIDTH, #define RX_LMFC_BUFF_ADJ_WIDTH, #define DISPARITY_ERR_FLAG_WIDTH, #define NT_TABLE_ERR_FLAG_WIDTH, #define UNEXP_CNTL_CHAR_FLAG_WIDTH, and #define ERR_CNT_READ_CH_SEL_WIDTH. • Added macros #define TX_CONTROL_REG_OFFSET_STRT, #define TX_STATUS_REG_OFFSET_STRT, #define TX_TEST_MODE_REG_OFFSET_STRT, #define TX_LINK_CFG_0_REG_OFFSET_STRT, #define TX_LINK_CFG_1_REG_OFFSET_STRT, #define TX_LINK_CFG_2_REG_OFFSET_STRT, #define TX_LINK_CFG_3_REG_OFFSET_STRT, #define TX_LINK_CFG_4_REG_OFFSET_STRT, #define TX_LINK_CFG_5_REG_OFFSET_STRT, #define TX_LINK_CFG_6_REG_OFFSET_STRT, #define TX_LINK_CFG_7_REG_OFFSET_STRT, #define TX_CORE_RST_WIDTH, #define TX_SYSREF_MASK_WIDTH, #define TX_SYSREF_EN_WIDTH, #define TX_LMFC_BUFF_ADJ_WIDTH, #define TX_LINK_STATE_WIDTH, #define TX_SYSREF_CAPTURED_WIDTH, #define TX_PHY_READY_WIDTH, #define TX_SYSREF_MIS_CNT_WIDTH, #define TX_TEST_PATTERN_WIDTH, #define TX_ILA_DID_WIDTH, #define TX_ILA_BID_WIDTH, #define TX_ILA_ADJCNT_WIDTH, #define TX_ILA_PHADJ_WIDTH, #define TX_ILA_ADJDIR_WIDTH, #define TX_ILA_L_WIDTH, #define TX_ILA_SCR_WIDTH, #define TX_ILA_F_WIDTH, #define TX_ILA_K_WIDTH, #define TX_ILA_M_WIDTH, #define TX_ILA_N_WIDTH, #define TX_ILA_CS_WIDTH, #define TX_ILA_Nt_WIDTH, #define TX_ILA_SUBCLASSV_WIDTH, #define TX_ILA_S_WIDTH, #define TX_ILA_JESDV_WIDTH, #define TX_ILA_CF_WIDTH, #define TX_ILS_HD_WIDTH, #define TX_OCT_PER_MUL_FR_WIDTH, #define TX_MUL_FR_ILA_SEQ_WIDTH, #define TX_ILA_LID_FCHK_WIDTH, #define TX_CORE_RST_BIT_POS, #define TX_SYSREF_EN_BIT_POS, #define TX_SYSREF_MASK_BIT_POS, #define TX_LMFC_BUFF_ADJ_BIT_POS, #define TX_LINK_STATE_BIT_POS, #define TX_SYSREF_CAPTURED_BIT_POS, #define TX_PHY_READY_BIT_POS, #define TX_SYSREF_MIS_CNT_BIT_POS, #define TX_TEST_PATTERN_BIT_POS, #define

Section	Change Summary
	TX_ILA_DID_BIT_POS, #define TX_ILA_BID_BIT_POS, #define TX_ILA_ADJCNT_BIT_POS, #define TX_ILA_PHADJ_BIT_POS, #define TX_ILA_ADJDIR_BIT_POS, #define TX_ILA_L_BIT_POS, #define TX_ILA_SCR_BIT_POS, #define TX_ILA_F_BIT_POS, #define TX_ILA_K_BIT_POS, #define TX_ILA_M_BIT_POS, #define TX_ILA_N_BIT_POS, #define TX_ILA_CS_BIT_POS, #define TX_ILA_Nt_BIT_POS, #define TX_ILA_SUBCLASSV_BIT_POS, #define TX_ILA_S_BIT_POS, #define TX_ILA_JESDV_BIT_POS, #define TX_ILA_CF_BIT_POS, #define TX_ILS_HD_BIT_POS, #define TX_OCT_PER_MUL_FR_BIT_POS, #define TX_MUL_FR_ILA_SEQ_BIT_POS, #define TX_ILA_LID_L0_BIT_POS, #define TX_ILA_LID_L1_BIT_POS, #define TX_ILA_LID_L2_BIT_POS, #define TX_ILA_LID_L3_BIT_POS, #define TX_ILA_LID_L4_BIT_POS, #define TX_ILA_LID_L5_BIT_POS, #define TX_ILA_LID_L6_BIT_POS, #define TX_ILA_LID_L7_BIT_POS, #define TX_ILA_FCHK_L0_BIT_POS, #define TX_ILA_FCHK_L1_BIT_POS, #define TX_ILA_FCHK_L2_BIT_POS, #define TX_ILA_FCHK_L3_BIT_POS, #define TX_ILA_FCHK_L4_BIT_POS, #define TX_ILA_FCHK_L5_BIT_POS, #define TX_ILA_FCHK_L6_BIT_POS, #define TX_ILA_FCHK_L7_BIT_POS, #define TX_CORE_RST, #define TX_SYSREF_EN, #define TX_SYSREF_MASK, #define TX_LMFC_BUFF_ADJ, #define TX_LINK_STATE, #define TX_SYSREF_CAPTURED, #define TX_PHY_READY, #define TX_SYSREF_MIS_CNT, #define TX_TEST_PATTERN, #define TX_ILA_DID, #define TX_ILA_BID, #define TX_ILA_ADJCNT, #define TX_ILA_PHADJ, #define TX_ILA_ADJDIR, #define TX_ILA_L, #define TX_ILA_SCR, #define TX_ILA_F, #define TX_ILA_K, #define TX_ILA_M, #define TX_ILA_N, #define TX_ILA_CS, #define TX_ILA_Nt, #define TX_ILA_SUBCLASSV, #define TX_ILA_S, #define TX_ILA_JESDV, #define TX_ILA_CF, #define TX_ILS_HD, #define TX_OCT_PER_MUL_FR, #define TX_MUL_FR_ILA_SEQ, #define TX_ILA_LID_L0, #define TX_ILA_LID_L1, #define TX_ILA_LID_L2, #define TX_ILA_LID_L3, #define TX_ILA_LID_L4, #define TX_ILA_LID_L5, #define TX_ILA_LID_L6, #define TX_ILA_LID_L7, #define TX_ILA_FCHK_L0, #define TX_ILA_FCHK_L1, #define TX_ILA_FCHK_L2, #define TX_ILA_FCHK_L3, #define TX_ILA_FCHK_L4, #define TX_ILA_FCHK_L5, #define TX_ILA_FCHK_L6, #define TX_ILA_FCHK_L7, #define RX_CONTROL_REG_OFFSET_STRT, #define RX_STATUS_REG_OFFSET_STRT, #define RX_ERR_STATUS_REG_OFFSET_STRT, #define RX_LINK_CFG_0_REG_OFFSET_STRT, #define RX_LINK_CFG_1_REG_OFFSET_STRT, #define RX_LINK_CFG_2_REG_OFFSET_STRT, #define RX_LINK_CFG_3_REG_OFFSET_STRT, #define RX_LINK_CFG_4_REG_OFFSET_STRT, #define RX_LINK_CFG_5_REG_OFFSET_STRT, #define RX_LINK_CFG_6_REG_OFFSET_STRT, #define RX_LINK_CFG_7_REG_OFFSET_STRT, #define RX_ERR_CNT_REG_OFFSET_STRT, #define RX_BUFF_FILL_LVL_REG_OFFSET_STRT, #define RX_CORE_RST_WIDTH, #define RX_CORE_REINIT_WIDTH, #define RX_SYSREF_EN_WIDTH, #define RX_SYSREF_MASK_WIDTH, #define RX_LMFC_BUFF_ADJ_WIDTH, #define RX_LINK_STATE_WIDTH, #define RX_SYSREF_CAPTURED_WIDTH, #define RX_PHY_READY_WIDTH, #define RX_SYSREF_MIS_CNT_WIDTH, #define RX_DISPARITY_ERR_FLG_WIDTH, #define RX_NOT_IN_TABLE_ERR_FLG_WIDTH, #define RX_UNEXP_CTRL_CHAR_FLG_WIDTH, #define RX_ERR_CNT_RD_CHN_SEL_WIDTH, #define RX_ILA_DID_WIDTH, #define RX_ILA_BID_WIDTH, #define RX_ILA_ADJCNT_WIDTH, #define RX_ILA_PHADJ_WIDTH, #define RX_ILA_ADJDIR_WIDTH, #define RX_ILA_L_WIDTH, #define RX_ILA_SCR_WIDTH, #define RX_ILA_F_WIDTH, #define RX_ILA_K_WIDTH, #define RX_ILA_M_WIDTH, #define RX_ILA_N_WIDTH, #define RX_ILA_CS_WIDTH, #define RX_ILA_Nt_WIDTH, #define RX_ILA_SUBCLASSV_WIDTH, #define RX_ILA_S_WIDTH, #define RX_ILA_JESDV_WIDTH, #define RX_ILA_CF_WIDTH, #define RX_ILS_HD_WIDTH, #define RX_OCT_PER_MUL_FR_WIDTH, #define RX_MUL_FR_ILA_SEQ_WIDTH, #define RX_ILA_LID_FCHK_ERR_CNT_WIDTH, #define RX_BUFF_FILL_LEVEL_WIDTH, #define RX_CORE_RST_BIT_POS, #define RX_CORE_REINIT_BIT_POS, #define RX_SYSREF_EN_BIT_POS, #define RX_SYSREF_MASK_BIT_POS, #define RX_LMFC_BUFF_ADJ_BIT_POS, #define RX_LINK_STATE_BIT_POS, #define RX_SYSREF_CAPTURED_BIT_POS, #define RX_PHY_READY_BIT_POS, #define RX_SYSREF_MIS_CNT_BIT_POS, #define RX_DISPARITY_ERR_FLG_BIT_POS, #define RX_NOT_IN_TABLE_ERR_FLG_BIT_POS, #define RX_UNEXP_CTRL_CHAR_FLG_BIT_POS, #define RX_ERR_CNT_RD_CHN_SEL_BIT_POS, #define RX_ILA_DID_BIT_POS, #define

Section	Change Summary
	RX_ILA_BID_BIT_POS, #define RX_ILA_ADJCNT_BIT_POS, #define RX_ILA_PHADJ_BIT_POS, #define RX_ILA_ADJDIR_BIT_POS, #define RX_ILA_L_BIT_POS, #define RX_ILA_SCR_BIT_POS, #define RX_ILA_F_BIT_POS, #define RX_ILA_K_BIT_POS, #define RX_ILA_M_BIT_POS, #define RX_ILA_N_BIT_POS, #define RX_ILA_CS_BIT_POS, #define RX_ILA_Nt_BIT_POS, #define RX_ILA_SUBCLASSV_BIT_POS, #define RX_ILA_S_BIT_POS, #define RX_ILA_JESDV_BIT_POS, #define RX_ILA_CF_BIT_POS, #define RX_ILS_HD_BIT_POS, #define RX_OCT_PER_MUL_FR_BIT_POS, #define RX_MUL_FR_ILA_SEQ_BIT_POS, #define RX_ILA_LID_L0_BIT_POS, #define RX_ILA_LID_L1_BIT_POS, #define RX_ILA_LID_L2_BIT_POS, #define RX_ILA_LID_L3_BIT_POS, #define RX_ILA_LID_L4_BIT_POS, #define RX_ILA_LID_L5_BIT_POS, #define RX_ILA_LID_L6_BIT_POS, #define RX_ILA_LID_L7_BIT_POS, #define RX_ILA_FCHK_L0_BIT_POS, #define RX_ILA_FCHK_L1_BIT_POS, #define RX_ILA_FCHK_L2_BIT_POS, #define RX_ILA_FCHK_L3_BIT_POS, #define RX_ILA_FCHK_L4_BIT_POS, #define RX_ILA_FCHK_L5_BIT_POS, #define RX_ILA_FCHK_L6_BIT_POS, #define RX_ILA_FCHK_L7_BIT_POS, #define RX_DISPARITY_ERR_CNT_BIT_POS, #define RX_NT_IN_TABLE_ERR_CNT_BIT_POS, #define RX_UNEXP_CTRL_CHAR_BIT_POS, #define RX_BUFF_FILL_LVL_BIT_POS, #define RX_CORE_RST, #define RX_SYSREF_EN, #define RX_SYSREF_MASK, #define RX_CORE_REINIT, #define RX_LMFC_BUFF_ADJ, #define RX_LINK_STATE, #define RX_SYSREF_CAPTURED, #define RX_PHY_READY, #define RX_SYSREF_MIS_CNT, #define RX_DISPARITY_ERR_FLG, #define RX_NOT_IN_TABLE_ERR_FLG, #define RX_UNEXP_CTRL_CHAR_FLG, #define RX_ERR_CNT_RD_CHN_SEL, #define RX_ILA_DID, #define RX_ILA_BID, #define RX_ILA_ADJCNT, #define RX_ILA_PHADJ, #define RX_ILA_ADJDIR, #define RX_ILA_L, #define RX_ILA_SCR, #define RX_ILA_F, #define RX_ILA_K, #define RX_ILA_M, #define RX_ILA_N, #define RX_ILA_CS, #define RX_ILA_Nt, #define RX_ILA_SUBCLASSV, #define RX_ILA_S, #define RX_ILA_JESDV, #define RX_ILA_CF, #define RX_ILS_HD, #define RX_OCT_PER_MUL_FR, #define RX_MUL_FR_ILA_SEQ, #define RX_ILA_LID_L0, #define RX_ILA_LID_L1, #define RX_ILA_LID_L2, #define RX_ILA_LID_L3, #define RX_ILA_LID_L4, #define RX_ILA_LID_L5, #define RX_ILA_LID_L6, #define RX_ILA_LID_L7, #define RX_ILA_FCHK_L0, #define RX_ILA_FCHK_L1, #define RX_ILA_FCHK_L2, #define RX_ILA_FCHK_L3, #define RX_ILA_FCHK_L4, #define RX_ILA_FCHK_L5, #define RX_ILA_FCHK_L6, #define RX_ILA_FCHK_L7, #define RX_DISPARITY_ERR_CNT, #define RX_NT_IN_TABLE_ERR_CNT, #define RX_UNEXP_CTRL_CHAR, and #define RX_BUFF_FILL_LVL.
References	Removed Avant-G and Avant-X web pages.

Revision 1.0, June 2025

Section	Change Summary
All	Initial release.

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