DDR Memory Module IP

IP Version: v2.1.0

Release Notes

FPGA-RN-02080-1.0

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Contents

1. Introduction

This document contains the Release Notes for the DDR Memory Module IP. For specific details about the IP, refer to the following:

- DDR Memory Module IP User Guide (FPGA-IPUG-02060)

DDR Memory Module IP v2.1.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1	• Added delay configuration for clock, command, and address lines • Updated PLL • Added support for constraints to be consumed by the Radiant Constraint Propagation Engine • Added DRC on unsupported configurations

DDR Memory Module IP Earlier Versions

IP Version	Summary of Changes
2.0.0	Modified DDR clock from differential to two single-ended complementary signals
1.4.0	Added UT24C and UT24CP support
1.3.0	• Added LFMXO5 support • Updated calculation of PLL settings
1.2.0	• Added LFCPNX support • Updated PLL instance
1.1.0	• Added LFD2NX support • Improved selectable values in GUI • Updated PLL instance
1.0.1	• Added optional PLL • Improved implementation of X4 gearing ratio
1.0.0	Initial release

References

- DDR Memory Module IP User Guide (FPGA-IPUG-02060)
- CertusPro-NX web page
- Certus-NX web page
- CrossLink-NX web page
- IP Core for Nexus Devices
- Lattice Radiant Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

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For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

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