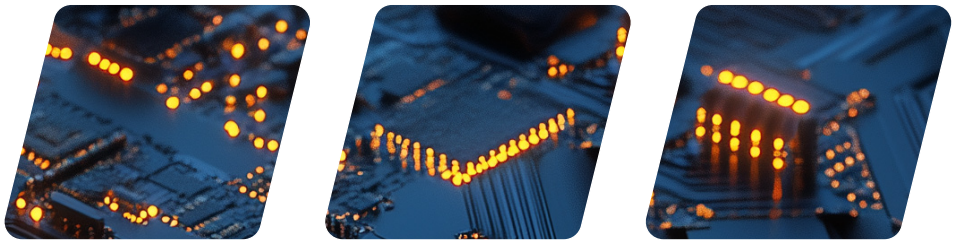
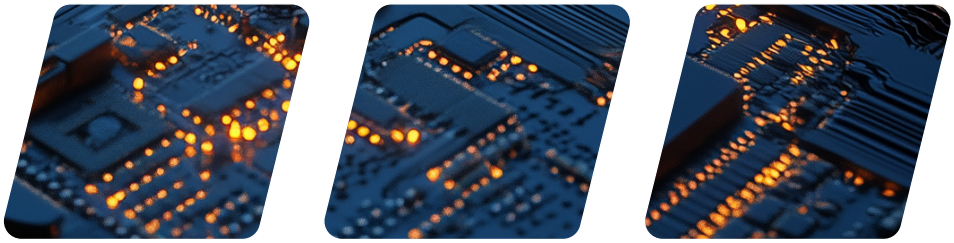


5G OFDM Modulation with Lattice iFFT and FIR IPs Use Case



White Paper

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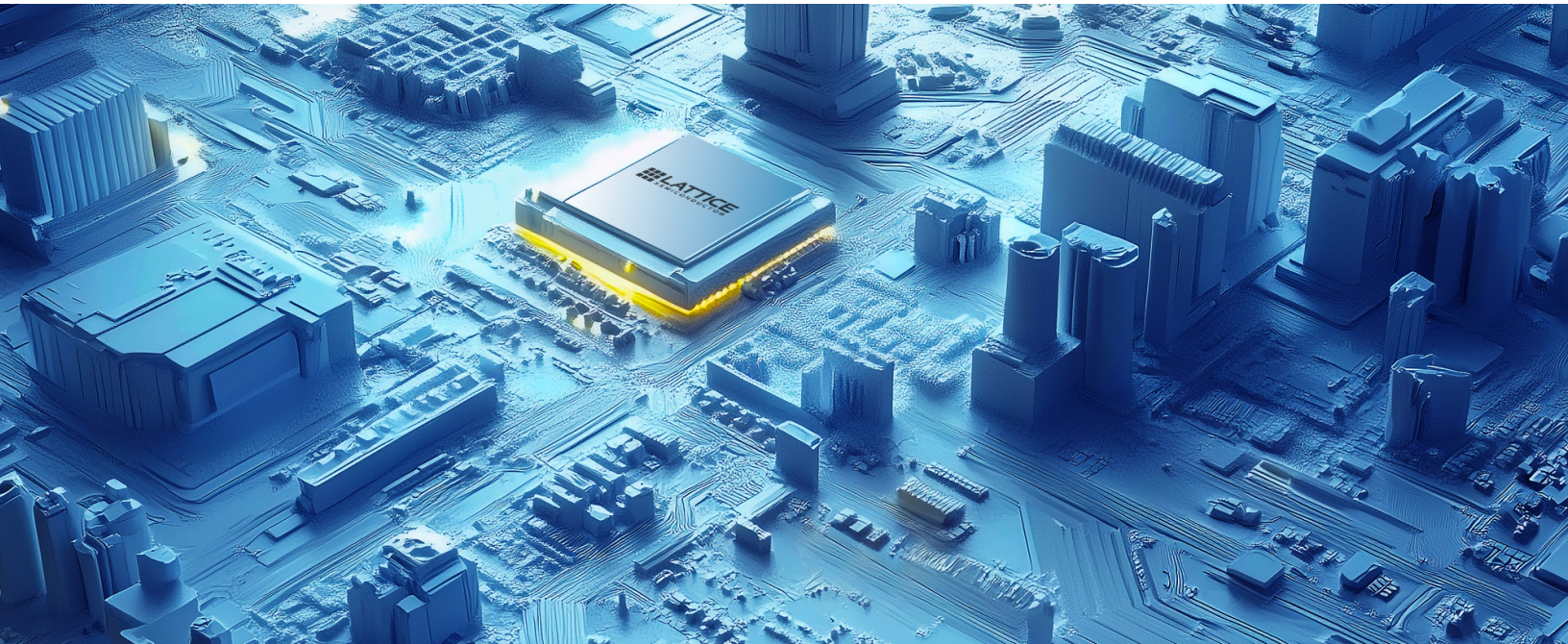
ABSTRACT

This paper introduces an enhanced Orthogonal Frequency Division Multiplexing (OFDM) modulator design implemented in FPGAs, utilizing the Lattice Fast Fourier Transform (FFT) Compiler IP Core in inverse FFT mode and the Lattice Finite Impulse Response (FIR) Filter IP Core. This design addresses the common challenge of generating complex test patterns without a host controller, significantly improving the efficiency of wireless link testing.

By enabling direct testing of the JESD204B link to the analog front end, the OFDM modulator eliminates the dependency on a host controller, thereby streamlining the initial bring-up process. The design can be directly implemented in the Lattice FPGA core, resulting in cost savings and reduced development turnaround time.

The modulator's effectiveness was validated through interoperability with the Analog Devices, Inc. (ADI) 5G RF Front-end ADRV9029 evaluation board via the Lattice JESD204B IP link using the Avant-X70 Versa Board. This setup demonstrates the modulator's capability to generate OFDM patterns and validate wireless links efficiently.

In conclusion, this paper presents a novel OFDM modulator design integrated with Lattice FIR and iFFT IP cores, simplifying wireless link validation and reducing both cost and development time.



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1. Introduction

Orthogonal Frequency Division Multiplexing (OFDM) is a key technology used in many wireless and wired communication systems, especially 5G and Wi-Fi 4/5/6/7 standards. OFDM is known for its high spectral efficiency, robustness to channel fading, and flexibility.

This paper introduces an enhanced solution to a common problem encountered in these systems - the need for complex test patterns that can be difficult to generate without a host controller. The design and implementation of an OFDM modulator is presented in this paper. This functionality is particularly useful for wireless link testing. The design was developed through the integration of Lattice FPGA optimized Fast Fourier Transform (FFT) Compiler IP Core in inverse FFT mode and Finite Impulse Response (FIR) Filter IP Core, offering an alternative method to the previous method using HDL Coder generated FIR and iFFT modules [1] which remains a valid and effective solution.

The Lattice FFT Compiler IP Core, provides forward and inverse FFT modes with configurable point sizes and implementation modes, ensuring flexibility and efficiency in signal processing. In this design, the inverse mode FFT Compiler IP Core (iFFT) is used. The Lattice FIR Filter IP Core is implemented using high-performance Digital Signal Processing (DSP) blocks available in Lattice devices. It offers configurable input data, coefficient, and output data widths, supporting a wide range of applications.

This paper also addresses a common problem encountered during the initial bring-up of a wireless link - the unavailability of a host controller to feed OFDM patterns into the FPGA. Dependency on the host for OFDM patterns would necessitate the bring-up of a matching interface between FPGA and host, such as Peripheral Component Interconnect Express® (PCIe), as well as host software required to perform the test before the wireless link test can commence. This process is not only time-consuming and inefficient but also challenging to debug when issues arise.

To further enhance the testing process, this paper showcases interoperability with the Analog Devices, Inc. (ADI) 5G RF Front-end ADRV9029 evaluation board through the Lattice JESD204B IP link using Lattice Avant™-X70 Versa Board. The ADRV9029 is a quad-channel wideband RF transceiver designed for 5G applications. This setup demonstrates the capability of the modulator to generate OFDM patterns and validate the wireless link without any dependency on the host, significantly improving the efficiency of the testing process.

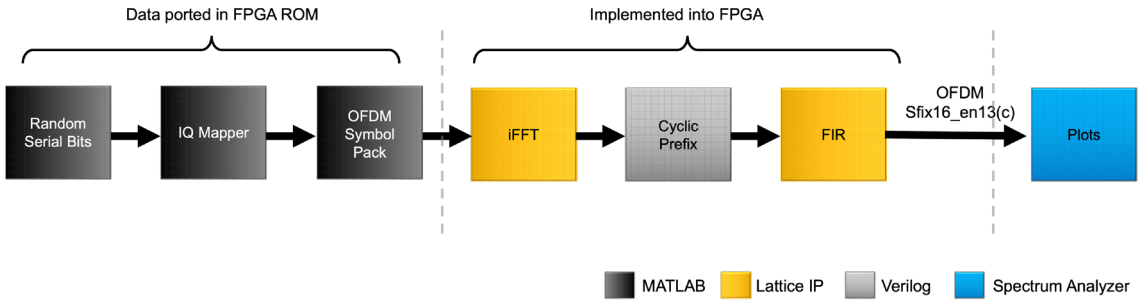
With the introduction of the OFDM modulator, integrated with Lattice FIR and iFFT IP cores, we can now validate the FPGA wireless link more effectively and efficiently.

2. OFDM Modulator Design with FIR and iFFT IPs

2.1. DESIGN DETAILS

The OFDM modulator design leverages various design techniques, tools and Lattice IP cores, including MATLAB®, iFFT, FIR and hand-coded RTL. Figure 1 shows the high-level block diagram of the OFDM modulator design data path. This transmit-chain of a OFDM modulator with FIR highlights the merits of this modulation scheme for 5G communication systems.

FIGURE 1. BLOCK DIAGRAM OF THE OFDM MODULATOR DESIGN



The color coding in the Figure 1 differentiates the implementation methods:

- **Dark grey:** MATLAB generated symbols into FPGA ROM
- **Yellow:** Blocks implemented with Lattice IP cores
- **Light grey:** Blocks implemented with hand-coded Verilog
- **Blue:** Spectrum plots with spectrum analyzer for verification

2.2. OFDM PATTERN GENERATION

The OFDM pattern generator continuously repeats and outputs the same OFDM symbol with its cyclic prefix. A set of random modulation symbols are pre-generated in MATLAB, processed and stored in a FPGA ROM. The ROM content was read into subsequent blocks including iFFT IP, cyclic prefix block, and FIR IP to form the OFDM pattern and generates IQ data to feed to the RF Front End. The following table shows the OFDM pattern system parameters used in the design.

TABLE 1. OFDM PATTERN SYSTEM PARAMETERS

PARAMETER	VALUE
FFT Size (Total number of Subcarriers)	1024
Number of Data Subcarriers	700
Number of Guard Subcarriers	324
Subcarrier Spacing	15 KHz
Oversampling	10
Cyclic Prefix Length	64
Modulation	64QAM
Number of OFDM Symbols	1
Sampling Frequency	153.6 MHz
DAC Number of Input bits	16

2.3. UNIQUE FEATURES AND ADVANTAGES

- **Integrated Design:** Users can implement this design directly in the FPGA core without the need for external equipment.
- **Cost and Time Efficiency:** This design reduces the cost and time associated with purchasing or loaning external equipment and setting up complex test systems.
- **Comprehensive Verification:** Users can hook up with the JESD204B IP in the FPGA and perform verification from functional simulation to hardware validation on development kits.

2.4. DESIGN PROCESS

This section discusses the design process for the OFDM modulator design, starting from MATLAB model implementation to Lattice FPGA implementation.

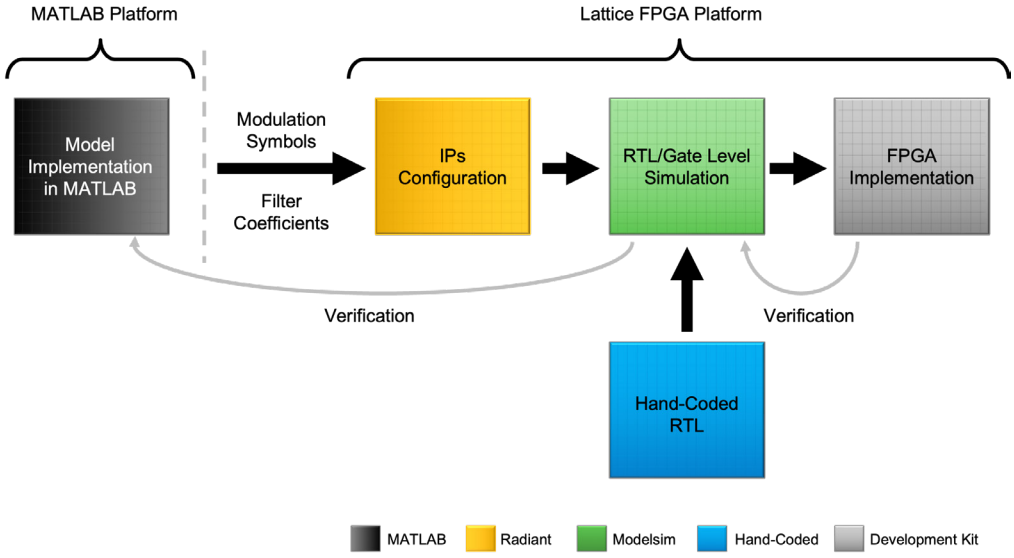
2.4.1. DEVELOPMENT FLOW

The development flow for the OFDM modulator design in a Lattice FPGA begins with the initial model implementation in MATLAB. This stage involves modeling the modulator with required parameters. Modulator output was verified with Power Spectrum Density (PSD) plot. The generated modulation symbols and sinc filter coefficients are subsequently ported to the Lattice Avant™ FPGA. Avant FPGA was chosen for its optimal combination of hardened DSP blocks and embedded memory, providing an efficient mix of processing power and storage capacity. These elements are integrated into the ROM IP and FIR IP, ensuring seamless data handling. Additionally, other crucial FPGA IPs, such as the iFFT, are configured according to the FFT size used during modulation symbol generation.

Next, these IPs are combined with hand-coded RTL modules, including cyclic prefix module, to form the complete design. To ensure the design's functionality, RTL simulations are conducted in QuestaSim™ Lattice Edition, with results meticulously compared against MATLAB simulations for accuracy.

The final step involves implementing the design into a Lattice FPGA development kit. Here, hardware output results are rigorously checked against RTL simulations. Any discrepancies observed during verification prompt thorough debugging and revisiting of previous stages to apply necessary fixes, ensuring a robust and reliable OFDM modulator design, see Figure 2.

FIGURE 2. DEVELOPMENT FLOW FOR THE OFDM MODULATOR DESIGN



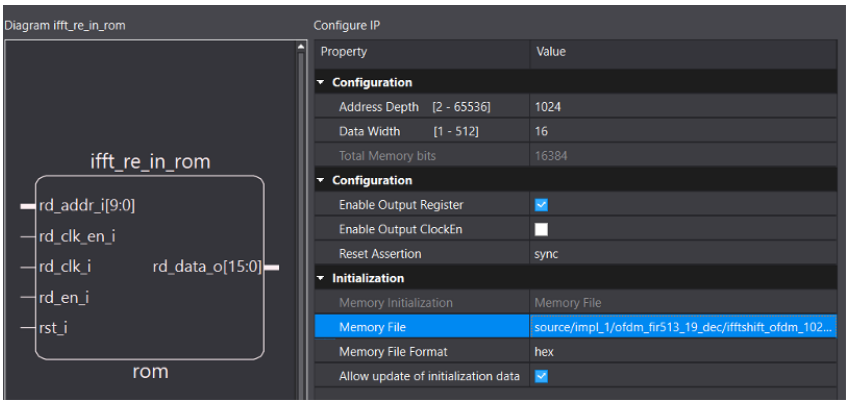
2.4.2. FPGA DESIGN BLOCKS

This section discusses the modules used in the FPGA to implement the OFDM modulator.

2.4.2.1. ROM

The OFDM modulation symbols generated by MATLAB were separated into their real and imaginary components before being converted to fixed-point format. These fixed-point values were then transformed into hexadecimal (HEX) format and stored in the FPGA ROMs. During user mode, the ROM content was fed into the IFFT IP. Figure 3 shows the example configuration of Lattice ROM IP used in this design.

FIGURE 3. THE CONFIGURATION OF THE ROM IP TO STORE THE REAL PART OF OFDM MODULATION SYMBOLS.

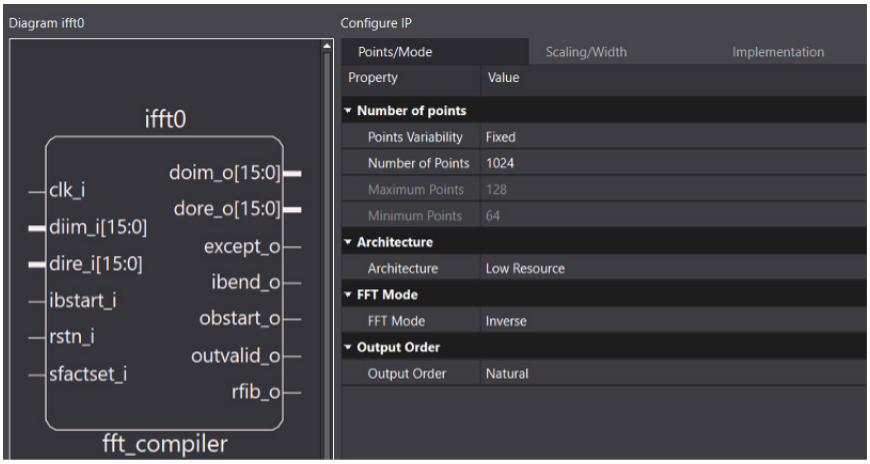


2.4.2. 2. IFFT

In transmitters using OFDM as a multicarrier modulation technology, the OFDM symbol is constructed in the frequency domain by mapping the input bits on the I- and Q- components of the 64QAM modulated symbols and then ordering them in a sequence with specific length (aka iFFT size) according to the number of subcarriers in the OFDM symbol. That is, by the mapping and ordering process, one constructs the frequency components of the OFDM symbol. To transmit them, the signal must be represented in time domain. This is accomplished by the inverse fast Fourier transform.

In this modulator design, each 64QAM symbol is mapped into one frequency sub-carrier and converted to time-domain using Lattice FFT Compiler IP in inverse mode. Figure 4 shows the example configuration of Lattice FFT Compiler IP used in this design.

FIGURE 4. THE CONFIGURATION OF THE INVERSE-MODE FFT COMPILER IP



2.4.3. CYCLIC PREFIX

The cyclic prefix is an essential element that improves the reliability and efficiency of data transmission. In this design, the final 64 samples of the OFDM symbol are duplicated at the start of the same symbol. This duplication helps to reduce inter-symbol interference (ISI) during the signal transmission. The output from the iFFT goes into the hand-coded cyclic prefix block.

2.4.4. FIR COMPILER IP

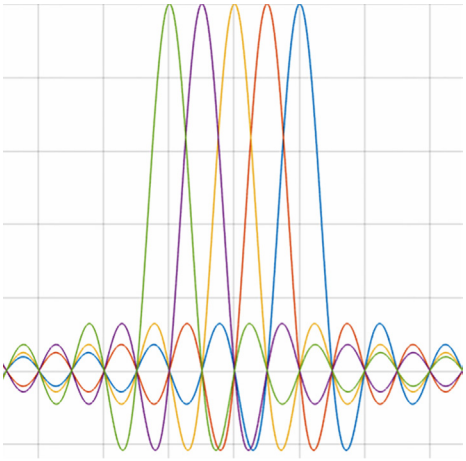
The final block in the data path is a filter. The filter is applied to the time domain OFDM symbol to improve the out-of-band radiation of the sub-band signal, while maintaining the complex-domain orthogonality of OFDM symbols. To achieve this, the FIR filter needs to satisfy the following criteria:

- Flat Passband over the subcarriers in the sub-band
- Sharp transition band to minimize guard-bands
- Sufficient stop-band attenuation

A filter with a rectangular frequency response, i.e. a sinc impulse response, meets these criteria. To make this causal, the low-pass filter is realized using a window, which, effectively truncates the impulse response and offers smooth transitions to zero on both ends [2].

Figure 5 shows an example plot of 5 adjacent subcarriers in the frequency domain, normalized to an amplitude of 1 and a frequency separation of 1. The subcarriers shown are orthogonal. Each frequency bin is represented as a sinc function in frequency domain.

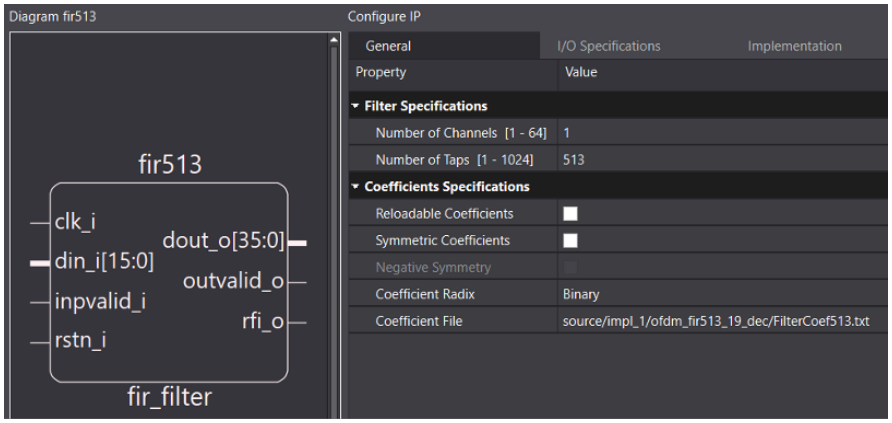
FIGURE 5. EXAMPLE PLOT OF ADJACENT AND ORTHOGONAL SUBCARRIERS



In OFDM with FIR, the sub-band OFDM signal is passed through the designed FIR. As the filter's passband corresponds to the signal's bandwidth, only the few subcarriers close to the edge are affected. A key consideration is that the filter length can be allowed to exceed the cyclic prefix length for OFDM [3]. The inter-symbol interference incurred is minimized due to the FIR design using windowing (with soft truncation).

In this design, the 513-tap coefficients of the sinc function were generated using MATLAB and then ported to the FIR Compiler IP. Figure 6 shows the example configuration of the Lattice FIR Compiler IP used in this design.

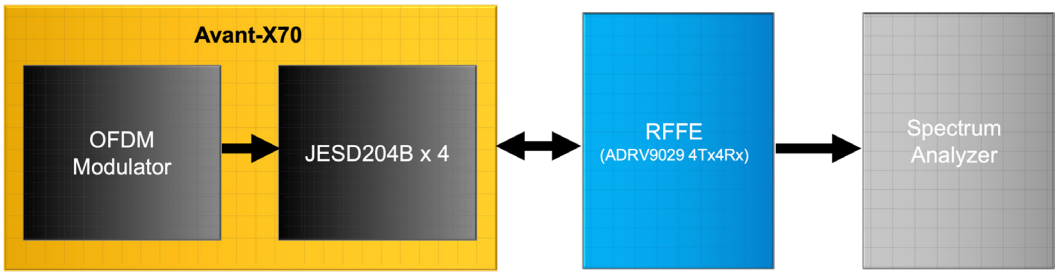
FIGURE 6. THE CONFIGURATION OF THE FIR COMPILER IP



3. Implementation

The OFDM modulator design was implemented into the Avant-X70 device using the Avant-X70 Versa Board. The OFDM modulator interfaces with the JESD204B link layer and PHY layer to send data to the RF Front-end ADRV9029. There are a total of 4 JESD204B lanes, each running up to 6.144Gbps. The OFDM modulator and JESD204B IP run on the 153.6 MHz clock generated on the ADRV9029 Evaluation Board, see Figure 7.

FIGURE 7. BLOCK DIAGRAM OF THE INTEROPERABILITY TEST SETUP: AVANT JESD204B AND ADRV9029



3.1. SOFTWARE AND HARDWARE USED

The software and hardware used in this design are as follows:

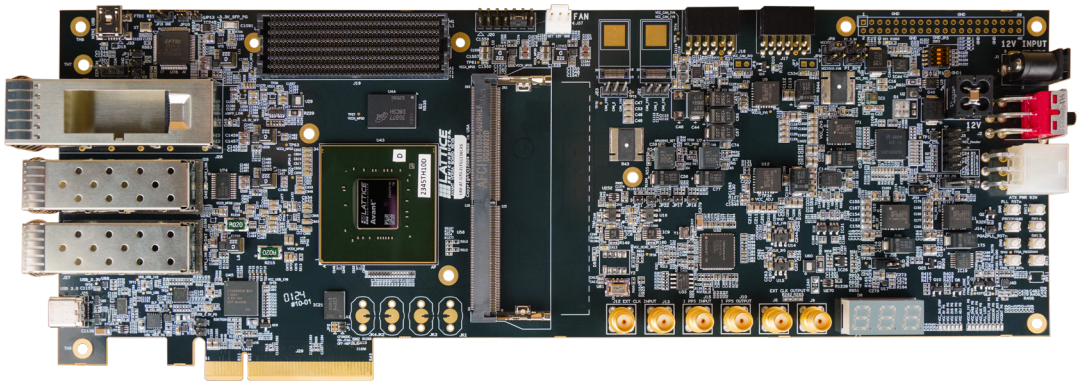
Software:

- Lattice Radiant™ Software
- tinySA®-App
- MATLAB

Hardware:

- Lattice Avant-X70 (Package LAV-AT-X70-2LFG1156C)
- Lattice Avant-X70 Versa Board
- ADRV9029 Evaluation Board
- tinySA Ultra Spectrum Analyzer

FIGURE 8. TOP VIEW OF THE AVANT-X70 VERSA BOARD



3.2. DESIGN VERIFICATION

This design was verified on hardware by the interoperability test with Avant-X70 Versa Board and ADRV9029 Evaluation Board through JESD204B interface. This comprehensive verification process ensures the robustness and reliability of the design implementation. The following sections describe the test methodologies used.

3.2.1. INTEROPERABILITY TEST

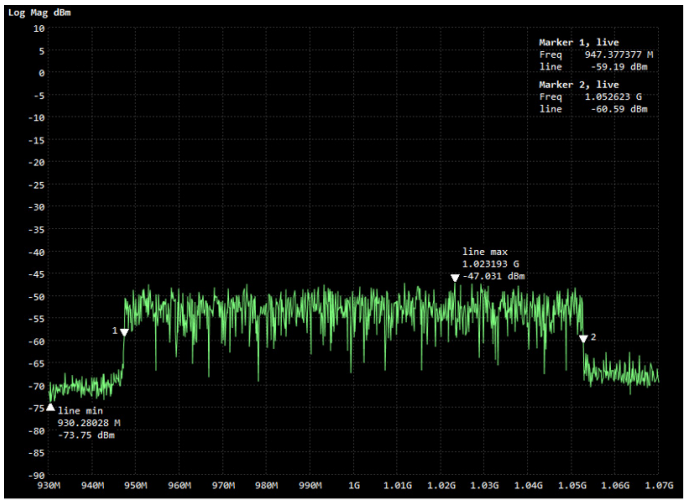
- The Avant-X70 Versa Board was connected to the ADRV9029 Evaluation Board through FPGA Mezzanine Card (FMC) connection on the boards.
- The RF signal output from ADRV9029 was connect to the spectrum analyzer using SMA cable to capture the PSD plot
- The bandwidth of the plot was compared with the theoretical value to ensure correct implementation.

4. Results and Discussion

4.1. HARDWARE TESTING ON AVANT-X70 VERSA BOARD

The RF signal output from ADRV9029 Evaluation board was connected to the spectrum analyzer to capture the PSD plot. The bandwidth of the PSD plot is measured using Markers. Figure 9 shows the PSD plot of one of the RF signal outputs.

FIGURE 9. PSD SPECTRUM PLOT AT THE SPECTRUM ANALYZER



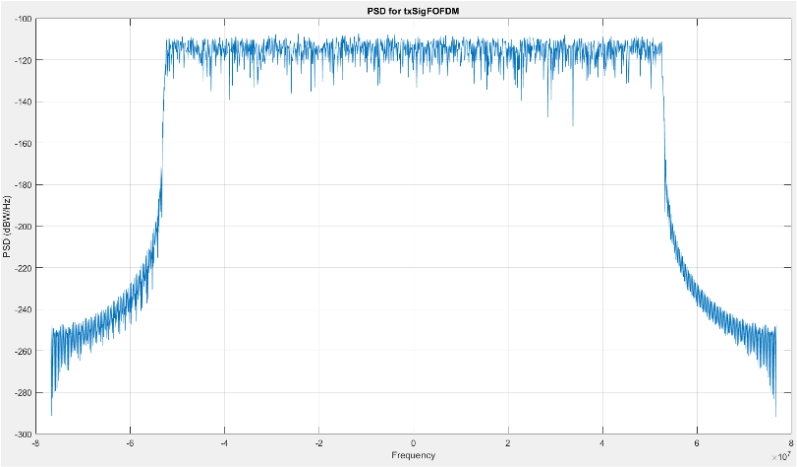
The key observations from the hardware testing results are:

- The PSD plot is of the rectangular shape
- The bandwidth measured = 1052MHz – 947MHz = 105MHz

4.2. MATLAB SIMULATION

The PSD of the OFDM modulator output from the MATLAB model was plotted to compare with the PSD spectrum captured by the spectrum analyzer. It was observed that both the shape and bandwidth of the PSD plots matched between the MATLAB model and the hardware testing results.

FIGURE 10. PSD PLOT OF OFDM OUTPUT FROM MATLAB MODEL



4.3. ANALYSIS AND INTERPRETATION OF THESE RESULTS

With the OFDM pattern system parameters as described in Table 1, the following are the theoretical calculation of the expected bandwidth of the PSD spectrum bandwidth captured in spectrum analyzer.

OFDM bandwidth = Number of Data Subcarriers x Subcarrier Spacing x Oversampling
= 700 X 15K x 10
= 105 MHz

The expected bandwidth of the PSD spectrum is 105 MHz, which matches the bandwidth values derived from the plots in both the MATLAB simulation and the spectrum analyzer.

5. Conclusion

5.1. SUMMARY OF THE RESEARCH AND ITS FINDINGS

This paper presented the design and implementation of a OFDM modulator through the integration of Lattice FFT Compiler IP Core, Lattice FIR Filter IP Core and hand-coded RTLs. The results obtained from the interoperability test with Avant-X70 Versa Board and ADRV9029 Evaluation Board through JESD204B links, demonstrated the robustness and reliability of the design. Furthermore, the matching PSD spectrum bandwidth results between theoretical value and spectrum analyzer capture, validate the functionality of the design.

5.2. SUGGESTIONS FOR FUTURE RESEARCH

Future research could focus on the following areas:

- OFDM demodulator development: The demodulator would complete the loopback data path where the received OFDM symbol can be recovered and check against the sent symbol.

6. References

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7. Abbreviations in This Document

A LIST OF ABBREVIATIONS USED IN THIS DOCUMENT

ABBREVIATIONS	DEFINITION
DSP	Digital Signal Processing
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
IP	Intellectual Property
ISI	Inter-Symbol Interference
OFDM	Orthogonal Frequency Division Multiplexing
PCIe	Peripheral Component Interconnect Express
PSD	Power Spectral Density
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
RFFE	RF Front-end
ROM	Read-Only Memory
RTL	Register Transfer Level

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