JTAG Bridge IP – Lattice Propel Builder 2025.1

IP Version: v1.0.0

User Guide

FPGA-IPUG-02288-1.0

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Contents

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AXI4	Advanced eXtensible Interface 4
CPU	Central Processing Unit
GUI	Graphical User Interface
HDL	Hardware Description Language
IP	Intellectual Property
JTAG	Joint Test Action Group
PC	Personal Computer
SoC	System on Chip
TAP	Test Access Port
TCL	Tool Command Language
UART	Universal Asynchronous Receiver/Transmitter

1. Introduction

The JTAG Bridge IP provides an efficient solution for debugging on-board issues by allowing you to access memory and peripheral registers directly using this IP, without involving the processor. It converts Joint Test Action Group (JTAG) Test Access Port (TAP) signals into Advanced eXtensible Interface 4 (AXI4) transactions, enabling you to perform read and write operations with byte, half-word, or word lengths.

The JTAG Bridge IP is implemented using Verilog HDL and it can be configured and generated using the Lattice Propel™ Builder software. The IP supports Certus™-N2, Lattice Avant™, MachXO5™-NX, CrossLinkU™-NX, CrossLink™-NX, CertusPro™-NX FPGA and Certus-NX devices.

1.1. Quick Facts

Table 1.1 presents a summary of the JTAG Bridge IP.

Table 1.1. JTAG Bridge IP Quick Facts

IP Requirements	Supported Devices	Certus-N2, Lattice Avant, MachXO5-NX, CrossLinkU-NX, CrossLink-NX, CertusPro-NX, and Certus-NX
Resource Utilization	Supported User Interfaces	AXI4 Interface, JTAG Interface
	Resources	See Table A.1 and Table A.2.
Design Tool Support	Lattice Implementation	IP v1.0.0 – Lattice Propel Builder 2025.1, Lattice Radiant™ Software 2025.1
	Simulation	No simulation module available.

1.2. Features

The JTAG Bridge IP has the following features:

- Supports AXI4 Interface.
- Supports configurable address width.
- Supports data mask and data size.
- Supports word-only access, or combination of word, half-word, and byte operations.

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal Names that end with:

- _n are active low.
- _i are input signals.
- _o are output signals.
- _io are bi-directional input/output signals.

1.4. Licensing and Ordering Information

The JTAG Bridge IP is provided at no additional cost with the Lattice Propel design environment. The IP can be fully evaluated in hardware without requiring an IP license string.

2. Functional Descriptions

2.1. Overview

The JTAG Bridge IP uses memory-mapped registers to convert JTAG TAP to AXI4 read or write operations. You can use Tool Command Language (TCL) scripts to transmit Address, Data, and Mask information. The IP returns the exact value for the given address or returns error status if the system hangs. Figure 2.1 shows the JTAG Bridge IP diagram.

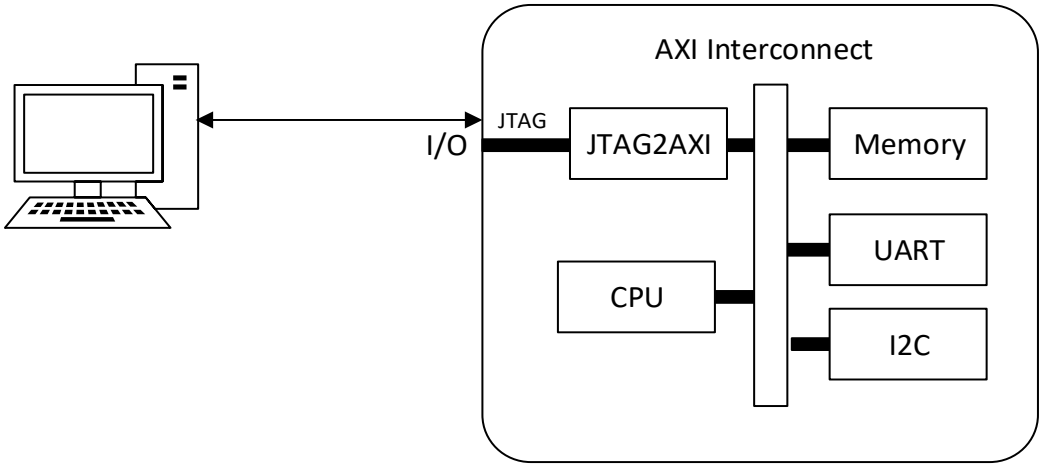

Figure 2.1. JTAG Bridge IP Diagram

2.2. Modules Description

The JTAG bridge IP output interface is fixed to AXI4 interface. The input interface is fixed to formal JTAG interface for the initial version.

As Figure 2.1 shows, the JTAG port should be exported to the top level of the design and assigned to the valid pins on board. The TCK signal should be assigned to the pclk pin. To find the valid pins, refer to the board schematics of the target device or board.

The AXI4 interface should be connected to the targeted memory or peripherals by AXI Interconnect. The default data width is 32 bits. You should enable mask and size settings if they need to access the specific memory space with 8-bit or 16-bit access.

Lattice Propel Builder provides user-friendly TCL scripts to use this IP. Refer to JTAG Bridge IP Generation and IP Demo sections for details.

2.3. Signal Description

Table 2.1, Table 2.2, and Table 2.3 list the ports of the soft IP in different categories.

2.3.1. Clock and Reset

Table 2.1. Clock and Reset Ports

Name	Direction	Width	Description
clk	In	1	SoC clock domain.
rst_n	In	1	SoC clock domain reset, active low.

2.3.2. AXI4 Interface

Table 2.2. AXI4 Manager Ports

Name	Direction	Width	Group	Description
AWREADY_m	In	1	AXI4 Mandatory Write Address Channel	—
AWVALID_m	Out	1		—
AWADDR_m	Out	32		—
AWLEN_m	Out	8		—
AWSIZE_m	Out	3		—
AWBURST_m	Out	2		Not implemented.
AWLOCK_m	Out	1		Not implemented.
AWCACHE_m	Out	4		Not implemented.
AWPROT_m	Out	3		Not implemented.
AWQOS_m	Out	4		Not implemented.
AWREGION_m	Out	4		Not implemented.
AWID_m	Out	1		Not implemented.
WREADY_m	In	1	AXI4 Mandatory Write Data Channel	—
WVALID_m	Out	1		—
WDATA_m	Out	32		—
WLAST_m	Out	1		Not implemented.
WSTRB_m	Out	4		—
BVALID_m	In	1	AXI4 Mandatory Write Response Channel	—
BRESP_m	In	2		b'00: OKAY[1] b'10: SLVERR[1] b'11: DECERR[1]
BID_m	In	1		Not implemented.
BREADY_m	Out	1		—
ARVALID_m	Out	1	AXI4 Mandatory Read Address Channel	—
ARREADY_m	In	1		—
ARCACHE_m	Out	4		Not implemented.
ARPROT_m	Out	3		Not implemented.
ARQOS_m	Out	4		Not implemented.
ARREGION_m	Out	4		Not implemented.
ARID_m	Out	1		Not implemented.
ARADDR_m	Out	32		—
ARLEN_m	Out	8		—
ARSIZE_m	Out	3		—
ARBURST_m	Out	2		Fixed 2'b01.
ARLOCK_m	Out	1		Not implemented.
RID_m	In	1	AXI4 Mandatory Read Data Channel	Not implemented.
RDATA_m	In	32		—
RRESP_m	In	2		b'00: OKAY[1] b'10: SLVERR[1] b'11: DECERR[1]
RLAST_m	In	1		—
RVALID_m	In	1		—

Name	Direction	Width	Group	Description
RREADY_m	Out	1		—

Note:

1. Refer to the AMBA AXI Protocol Specification for more detailed descriptions of these responses.

2.3.3. JTAG Interface

Table 2.3. JTAG Ports

Name	Type	Width	Description
TCK	In	1	JTAG Clock. Assign it to pclk.
TDI	In	1	—
TMS	In	1	—
TDO	Out	1	—

2.4. Attribute Summary

The configurable attributes of the JTAG Bridge IP are listed and described in Table 2.4 and Table 2.5.

The attributes can be configured through the Lattice Propel Builder software.

Table 2.4. Attributes Summary

Attribute	Values	Default	Dependency on Other Attributes
Bus Type	AXI4	AXI4	—
Address Width	7 to 32	32	—
AXI ID Width	1 to 15	4	—
AXI Port ID Number	0 to $2^{\text{AXI ID WIDTH}}-1$	0	—
Enable Mask and Size Settings	Enabled, Disabled	Disable	—

Table 2.5. Attributes Description

Attribute	Description
Bus Type	Interface type
Address Width	Address width
AXI ID Width	AXI Channel ID width
AXI Port ID Number	AXI Channel ID number
Enable Mask and Size Settings	Enable customized size and mask function

3. JTAG Bridge IP Generation

This section provides information on how to generate the JTAG Bridge IP module using the Lattice Propel Builder software.

To generate the JTAG Bridge IP module:

1. In the Lattice Propel Builder software, create a new design. Select the JTAG Bridge package.
2. Enter the component name. Click **Next**, as shown in Figure 3.1.

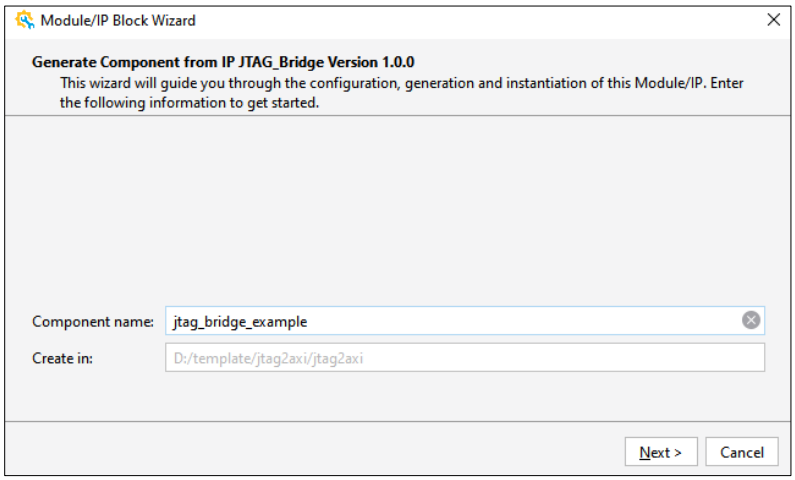

Figure 3.1. Entering Component Name

3. Configure the parameters as needed. Click **Generate** (Figure 3.2).

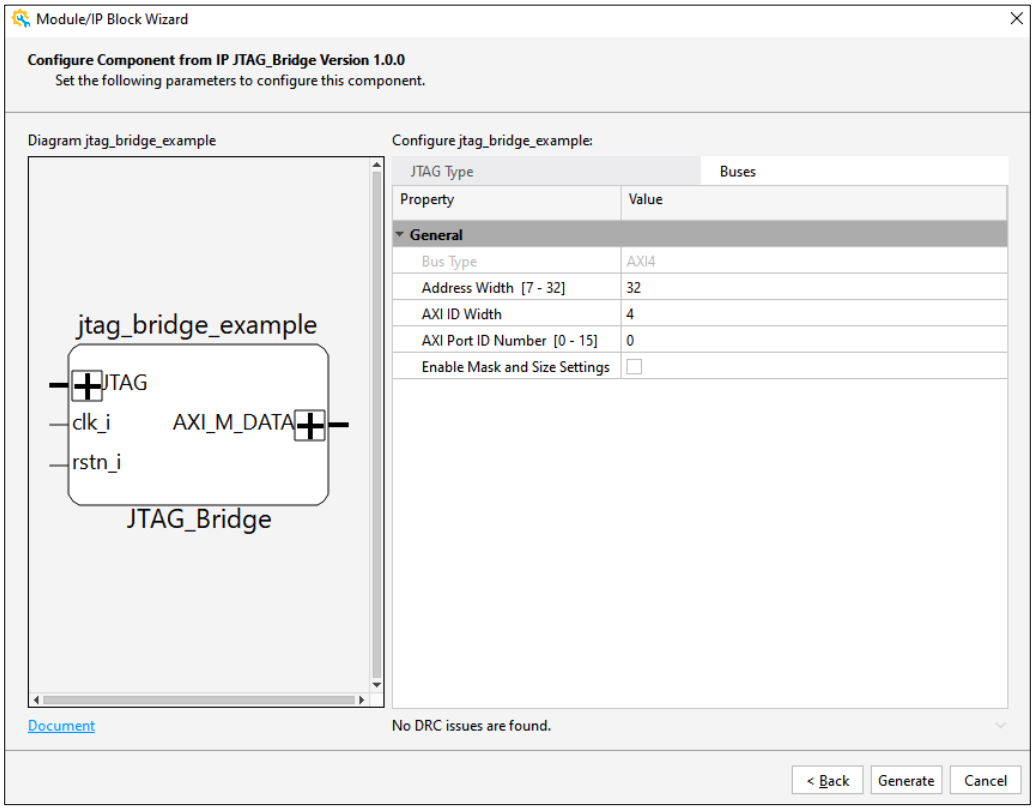

Figure 3.2. Configuring Parameters

4. Verify the information. Click **Finish** (Figure 3.3).

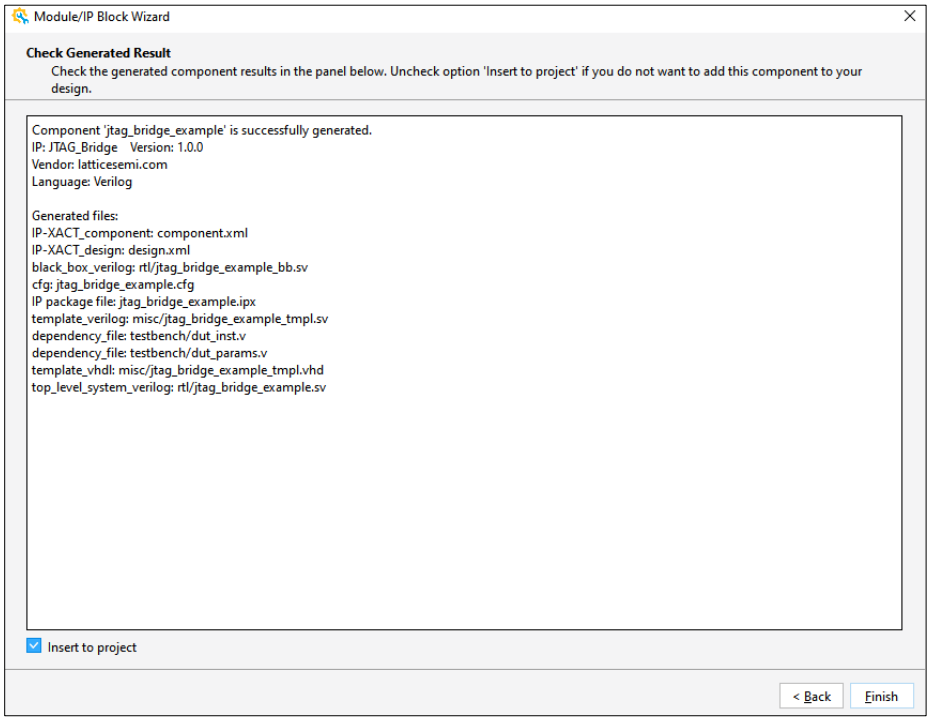

Figure 3.3. Verifying Results

5. Confirm or modify the module instance name. Click **OK** (Figure 3.4).

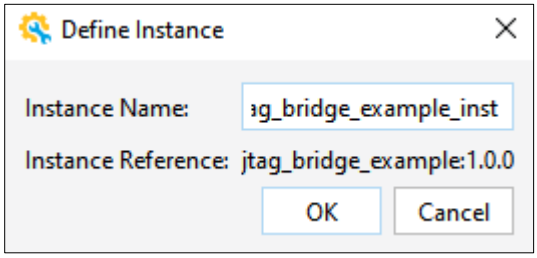

Figure 3.4. Specifying Instance Name

6. The JTAG Bridge IP instance is successfully generated, as shown in Figure 3.5.

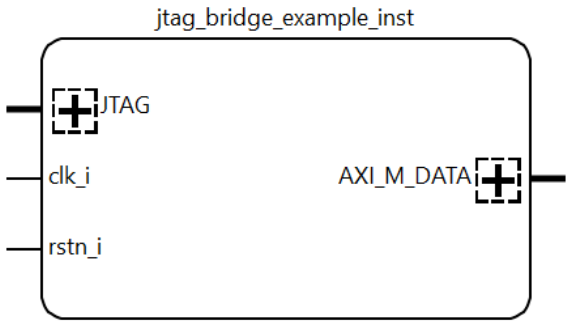

Figure 3.5. Generated Instance

4. IP Demonstration

4.1. Export JTAG Interface to Top

To export the JTAG interface signals to the top module through the Lattice Propel Builder GUI, right click on the JTAG interface and click on the **Export** button. An example is shown in Figure 4.1.

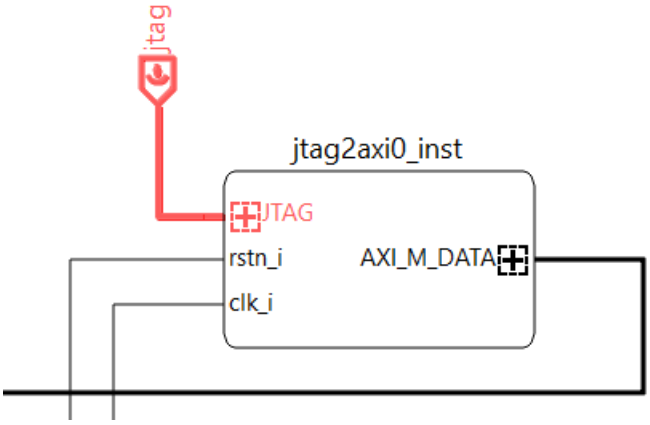

Figure 4.1. Export JTAG Interface to Top Module

Some SoC projects generated through Lattice Propel Builder may include additional Lattice Radiant top modules alongside the Lattice Propel top modules. In such cases, it is necessary to connect the JTAG interface signals to the appropriate inputs or outputs of the corresponding Radiant top module. This step also applies if you manually add one or more Lattice Radiant top-level RTL files to the generated SoC project.

4.2. Assign JTAG Ports to Specific Pins

To assign JTAG inputs and outputs to valid pins, run the Synthesis flow in the Lattice Radiant software. Then, open Device Constraints Editor or create a post-synthesis constraint file. The TCK should be assigned to pclk pins. Otherwise, you should add command line options in Place & Route Design strategies to pass the Lattice Radiant software flow. An example command line is shown below:

```
-exp WARNING_ON_PCLKPLC1=1
```

For details of pclk, refer to the Radiant Help document.

4.3. Generate Bitstream and Download to the Board

Run **Export Files** to generate a bitstream. Download it to the user board and run the SoC.

You should connect a USBN-2B cable to the I/O ports of the JTAG interface before moving to the next step.

4.4. Start Propel Builder TCL Console

Install the latest Lattice Propel Builder 2025.1 to use this feature. The TCL Console is by default at the bottom of the software GUI.

4.5. Open the USB Port to Connect to the IP

Use the following command to search for the valid ports on your PC (Figure 4.2):

```
sbp_cable list
```

```
% sbp_cable list
-------------------------------------------------------------------
 Port |   Name   |          Cable           | Channel | Location
-------------------------------------------------------------------
 0    | FTUSB-0  | Dual RS232-HS A          | A       | 0
 1    | FTUSB-1  | Dual RS232-HS B          | B       | 1
-------------------------------------------------------------------
```

Figure 4.2. Search for Cable List

Note that there might be multiple ports that you can see. You need to identify which one is the USBN-2B cable.

Then, use the following command to open the desired port, such as port 0 (Figure 4.3):

```
sbp_cable open -port 0
```

```
%  sbp_cable open -port 0
Open USB port 0 successfully.
%
```

Figure 4.3. Open Ports

Now the PC is connected to the IP.

4.6. Send Read/Write Commands

You can use the following command to read data from the target address of the SoC (Figure 4.4):

```
sbp_read_memory -addr 0x4000000
```

```
% sbp_read_memory -addr 0x4000000
0x00000000
```

Figure 4.4. Read Commands

The TCL command tool return the result from the target address.

You can use the following command to write data to the target address with specific data width if the Enable Mask and Size Settings option is enabled (Figure 4.5):

```
sbp_cable write -addr 0x40000000 -data 0x12345678 -data_width 32
```

```
% sbp_write_memory -addr 0x4000000 -data 0x0 -data_width 32
```

Figure 4.5. Write Commands

Note that the data width should be 8, 16, or 32 if Enable Mask and Size Settings is enabled. If this option is disabled, the data width should be 32.

You should align the address with the data width.

If the system hangs due to some reason, the tool shows a time-out warning.

Appendix A. Resource Utilization

Table A.1. Resource Utilization in CertusPro-NX-100 Device

Configuration	LUTs	Registers	sysMEM EBRs
Address Width = 32, AXI ID Width = 4, MASK = 0	203	197	0
Address Width = 32, AXI ID Width = 4, MASK = 1	203	197	0

Table A.2. Resource Utilization in LAV-AT-E70 Device

Configuration	LUTs	Registers	sysMEM EBRs
Address Width = 32, AXI ID Width = 4, MASK = 0	286	194	0
Address Width = 32, AXI ID Width = 4, MASK = 1	277	206	0

References

- Lattice Propel Builder 2025.1 User Guide (FPGA-UG-02235)
- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)
- AMBA AXI and ACE Protocol Specification

For more information, refer to:

- Lattice Propel Design Environment web page
- Lattice Certus-N2 Family Devices web page
- Lattice Avant-E Family Devices web page
- Lattice Avant-G Family Devices web page
- Lattice Avant-X Family Devices web page
- MachXO5-NX Family Devices web page
- CrossLink-NX Family Devices web page
- CertusPro-NX Family Devices web page
- Certus-NX Family Devices web page
- Lattice Insights for Training Series and Learning Plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, IP v1.0.0, June 2025

Section	Change Summary
All	Production release.

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