



RISC-V AHB-L IOPMP IP – Lattice Propel Builder 2025.1

IP Version: v1.0.0

User Guide

FPGA-IPUG-02286-1.0

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AHB-L	Advanced High-Performance Bus
CPU	Central Processing Unit
DMA	Direct Memory Access
FPGA	Field Programmable Gate Array
GUI	Graphic User Interface
HDL	Hardware Description Language
IOPMP	I/O Physical Memory Protection
IP	Intellectual Property
IRQ	Interrupt Request
LUT	Look Up Table
MD	Memory Domain
RISC-V	Reduced Instruction Set Computer-V (five)
TOR	Top of Range
WARL	Write Any Read Legal
RRID	Request Role ID

1. Introduction

The Lattice Semiconductor RISC-V AHB-L IOPMP IP is a separate physical memory protection unit that prevents illegal or unexpected access to some specific regions. These regions can be accessed by the RISC-V CPU but should not be accessed by some controllers, such as Direct Memory Access (DMA) or Ethernet. The RISC-V AHB-L IOPMP IP includes three AHB-Lite interfaces. The AHB-Lite control interface connects to the memory-mapped control and status registers while the two data interfaces bridge for the data path. The control path justifies the accessibility based on the address and entry settings. It decides whether or not to block this access, raise an interrupt, and respond with errors when the access is illegal.

The RISC-V AHB-L IOPMP IP is implemented using Verilog HDL and it can be configured and generated using the Lattice Propel™ Builder software. The IP supports Certus™-N2, Lattice Avant™, MachXO5™-NX, CrossLinkU™-NX, CrossLink™-NX, CertusPro™-NX, and Certus-NX FPGA devices.

1.1. Quick Facts

Table 1.1 presents a summary of the RISC-V AHB-L IOPMP IP.

Table 1.1. RISC-V AHB-L IOPMP IP Quick Facts

IP Requirements	Supported Devices	Certus-N2, Lattice Avant, MachXO5-NX, CrossLinkU-NX, CrossLink-NX, CertusPro-NX, and Certus-NX
Resource Utilization	Supported User Interfaces	AHB-Lite Interface
	Resources	See Table A.1 and Table A.2 .
Design Tool Support	Lattice Implementation	IP v1.0.0 – Lattice Propel Builder 2025.1, Lattice Radiant™ Software 2025.1
	Simulation	For a list of supported simulators, see the Lattice Radiant software user guide.

1.2. Features

The RISC-V AHB-L IOPMP IP has the following features:

- AHB-Lite interface bridge
- AHB-Lite interface memory-mapped registers
- Compact-K model based controller
- Up to four RISC-V AHB-L IOPMP entries with TOR support

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal Names that end with:

- `_n` are active low.
- `_i` are input signals.
- `_o` are output signals.
- `_io` are bi-directional input/output signals.

1.4. Licensing and Ordering Information

The RISC-V AHB-L IOPMP IP is provided at no additional cost with the Lattice Propel design environment. The IP can be fully evaluated in hardware without requiring an IP license string.

2. Functional Descriptions

2.1. Overview

The RISC-V AHB-L IOPMP IP has three interfaces, as shown in [Figure 2.1](#) and [Figure 2.2](#). For multi-processor use cases, if there is a main core CPU0 in the system, you may use CPU0 to set up the AHB-Lite interface for memory-mapped registers and handle the interrupts. For single-processor use cases, you may initialize the RISC-V AHB-L IOPMP module at the beginning and enable it by setting the enable bit in HWCFG0 register. The RISC-V AHB-L IOPMP is by default not enabled. For register settings, refer to the [Modules Description](#) section.

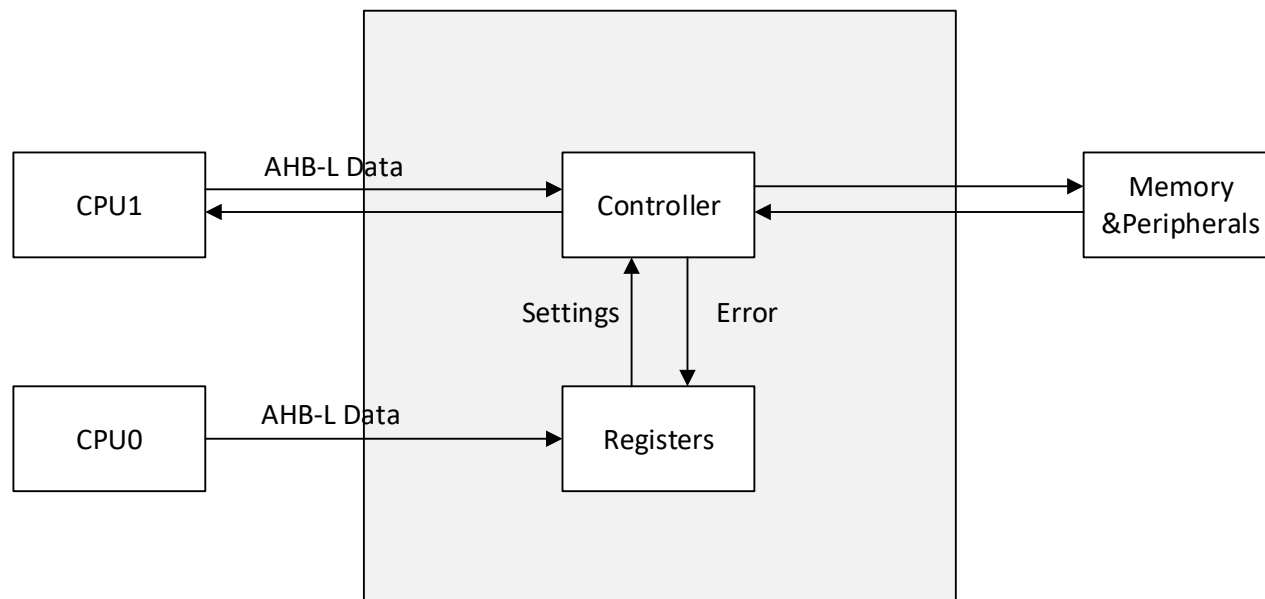


Figure 2.1. RISC-V AHB-L IOPMP IP Diagram for Multiple Processors

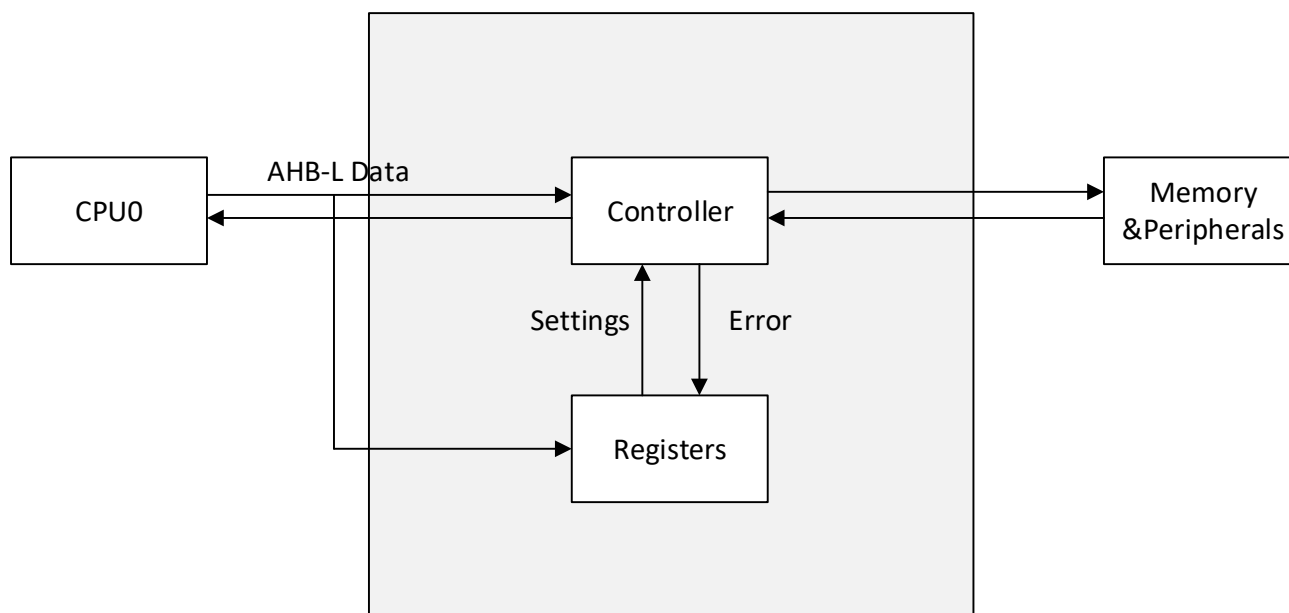


Figure 2.2. RISC-V AHB-L IOPMP IP Diagram for a Single Processor

2.2. Modules Description

2.2.1. Compact-K Model

The Lattice RISC-V AHB-L IOPMP IP follows the compact-K model. The module defines that the entire Lattice RISC-V subsystem is in one memory domain (MD), and the MD has exactly four entries. Either the number of memory domains or the number of entries is not configurable.

The request role ID (RRID) associated with the MD is based on GUI settings. Since the AHB-Lite protocol does not support ID certification, you should set a fixed number of ID to the IP during IP generation. The RISC-V AHB-L IOPMP IP passes the ID information to specific registers when the access is denied.

Table 2.1. RISC-V AHB-L IOPMP IP Control and Status Registers

Address	Register Name	Access	Fields
0x0000	VERSION	Read-Only	- vendor[23:0]: Vendor ID. - specver[31:24]: Specification version.
0x0004	IMPLEMENTATION	Read-Only	impid[31:0]: Implementation ID.
0x0008	HWCFG0	WARL	- model[3:0]: 0x4 – Compact-K model. - tor_en[4]: 0x1 – Top of Range (TOR) is supported. - sps_en[5]: 0x0 – Secondary permission settings is not supported. - user_cfg_en[6]: 0x0 – User customized attributes are not supported. - prient_progp[7]: 0x0 – Priority is not programmable. - rrid_transl_en[8]: 0x0 – Tagging a new RRID is not supported. - chk_x[10]: 0x0 – Instruction fetch is not supported. - no_w[12]: 0x1 – Write accesses always fail, as no rule is matched. - stall_en[13]: 0x0 – Stall-related features are not supported. - peis[14]: 0x0 – Interrupt suppression is not supported. - pees[15]: 0x0 – Error suppression is not supported. - mfr_en[16]: 0x0 – Multi Faults Record Extension is not supported. - md_num[30:24]: 0x1 – One MD is supported. - enable[31]: 0x0 – IOPMP check is enabled when this bit is asserted.
0x000C	HWCFG1	Read-Only	- rrid_num[15:0]: Indicates the supported number of RRID in the instance. - entry_num[31:16]: Indicates the supported number of entries in the instance.
0x0010	HWCFG2	WARL	- prio_entry[15:0]: Indicates the number of entries that are matched with certain priority. These rules should be placed in the lowest order. Within these rules, the lower the order, the higher the priority. - rrid_transl[31:16]: RRID tagged to outgoing transactions. Support only for HWCFG0.rrid_transl_en=1.
0x0014	ENTRYOFFSET	Read-Only	offset[31:0]: Indicates the offset address of the IOPMP array from the base of an IOPMP instance.
0x0048	MDCFLCK	Read-Only	lock[0]: Lock bit to the MDCFLCK register. It is hardwired to be one for the Compact-K model.
0x004C	ENTRYLCK	WARL	- lock[0:0]: Lock bit to the ENTRYLCK register. - f[16:1]: Indicates the number of locked IOPMP entries.

Address	Register Name	Access	Fields
0x0060	ERR_CFG	Read-Write	- lock[0:0]: Lock bit to the ERR_CFG register. - ie[1:1]: Enables the interrupt of IOPMP. - rs[2:2]: Response to an illegal read access. 0x0 – Responds with an implementation-dependent error. 0x1 – Responds with the success of a pre-defined value.
0x0064	ERR_REQINFO	bit[0] : Read & W1C bit[6:1]: Read-Only	- valid[0:0]: Indicates if the illegal capture recorder has valid content and keeps the content until the bit is cleared. - ttype[2:1]: Indicates the transaction type. 0x1 – Read. 0x2 – Write. 0x3 – Instruction fetch. - etype[6:4]: Indicates the type of violation. 0x0 – No error. 0x1 – Illegal read access. 0x2 – Illegal write access. 0x3 – Illegal instruction fetch. 0x4 – Partial hit on a priority rule. 0x5 – Does not hit any rule. 0x6 – Unknown RRID. 0x7 – User-defined error.
0x0070	ERR_REQID	Read-Only	Indicates the error address[33:2].
0x0800	MDCFG	Read-Only	t[15:0]: Indicates the number of entries.
ENTRYOFFSET + i * 16	ENTRY_ADDR(i)	WARL	addr[31:0]: Physical address[33:2] of the protected memory region.
ENTRYOFFSET + i * 16 + 8	ENTRY_CFG(i)	Read-Write	- r[0:0]: Read permission to the protected memory region. - w[1:1]: Write permission to the protected memory region. - a[4:3]: Address mode of the IOPMP entry. 0x0 – OFF 0x1 – TOR - sire[5:5]: Suppresses the interrupt for an illegal read. - siwe[6:6]: Suppresses the interrupt for an illegal write. - sere[8:8]: Suppresses the error for an illegal read. - siwe[9:9]: Suppresses the error for an illegal write.

2.2.2. RISC-V AHB-L IOPMP Entry

The RISC-V AHB-L IOPMP entries are described by a group of configurable registers. There are four entries in the Lattice RISC-V AHB-L IOPMP IP. Each entry includes an address register and a configuration register. These entries control the accessible memory range from the lower limit to the upper limit. All the registers are Write Any Read Legal (WARL). The fields that are not supported are zeros and cannot be revised.

2.2.3. Address Matching

The RISC-V AHB-L IOPMP IP supports the top boundary of an arbitrary range only, with the support of four-byte granularity. When selecting TOR, each entry controls an address range. This range starts either from the address of the previous entry and includes the address of the previous entry, or, if it is entry 0, it starts from 0. The range then extends up to but does not include the address of the current entry. If the address of the current entry is less than or equal to the previous entry, this entry does not work.

For each memory region, the RISC-V AHB-L IOPMP IP can block either the read or write access. When the access violates the entry rules, the IP receives either an error response, or a fake success response based on the ERR_CFG register. It can also raise an interrupt, which can inform the processor there is an illegal access from the RISC-V AHB-L IOPMP.

2.2.4. Lock

The RISC-V AHB-L IOPMP entries can be locked by the ENTRYLOCK register. The number stores in the field of ENTRYLOCK.f means the number of entries that are locked, counting from entry 0. If the number is equal to or larger than 4, all the entries are locked. When entries are locked, they cannot be modified by the hart.

The ENTRYLOCK can be locked by its bit 0. When this bit is locked, it cannot be unlocked until the system is reset.

2.2.5. Priority

Priority is not supported in this release.

2.3. Programming Flow

2.3.1. Program the RISC-V AHB-L IOPMP Entry

- Read the offset of the PMP entries from ENTRYOFFSET.
- Setup the correct upper limit of each memory region to ENTRY_ADDR.
- Setup the accessible and enable TOR to ENTRY_CFG.
- Setup the error response type and interrupt to ERR_CFG.
- Lock the entries to ENTRYLOCK if necessary.
- Lock the ENTRYLOCK register if necessary.

2.3.2. Interrupt Handler

- Read the information of error from ERR_REQINFO and ERR_REQID.
- Set the bit 0 of ERR_REQINFO to clear the interrupt.

2.3.3. Enable Memory Protection

Set the field enable[31] of the HWCFG0 register to enable the Memory Protection function.

2.4. Signal Description

Table 2.2 to Table 2.6 list the ports of the soft IP in different categories.

2.4.1. Clock and Reset

Table 2.2. Clock and Reset Ports

Name	Direction	Width	Description
clk	In	1	RISC-V AHB-L IOPMP soft IP clock.
rst_n	In	1	Global reset, active low.

2.4.2. AHB-L Interface

Table 2.3. AHB-Lite Data Manager Ports

Name	Direction	Width	Description
AHBL_M0_HADDR	Out	32	Sent to AHB-L Subordinate if the access is legal.
AHBL_M0_HWRITE	Out	1	
AHBL_M0_HSIZE	Out	3	
AHBL_M0_HPROT	Out	4	
AHBL_M0_HTRANS	Out	2	
AHBL_M0_HBURST	Out	3	
AHBL_M0_HMASTLOCK	Out	1	
AHBL_M0_HWDATA	Out	32	

Name	Direction	Width	Description
AHBL_M0_HRDATA	In	32	
AHBL_M0_HREADY	In	1	
AHBL_M0_HRESP	In	1	

Note:

1. Refer to the [AMBA 3 AHB-Lite Protocol Specification](#) for more detailed descriptions of these responses.

Table 2.4. AHB-Lite Data Subordinate Ports

Name	Direction	Width	Description
AHBL_S0_HADDR	In	32	Get from AHB-L Managers.
AHBL_S0_HWRITE	In	1	
AHBL_S0_HSIZE	In	3	
AHBL_S0_HPROT	In	4	
AHBL_S0_HTRANS	In	2	
AHBL_S0_HBURST	In	3	
AHBL_S0_HMASTLOCK	In	1	
AHBL_S0_HWDATA	In	32	
AHBL_S0_HRDATA	Out	32	
AHBL_S0_HREADY	Out	1	
AHBL_S0_HRESP	Out	1	

Note:

1. Refer to the [AMBA 3 AHB-Lite Protocol Specification](#) for more detailed descriptions of these responses.

Table 2.5. AHB-Lite Control Subordinate Ports

Name	Direction	Width	Description
AHBL_CTR_HADDR	In	32	Address to memory-mapped register
AHBL_CTR_HWRITE	In	1	• 1 – Write • 0 – Read
AHBL_CTR_HSIZE	In	3	• 2 – Word • 1 – Half-word • 0 – Byte
AHBL_CTR_HPROT	In	4	—
AHBL_CTR_HTRANS	In	2	Only 2'b10 is accepted for a single burst.
AHBL_CTR_HBURST	In	3	—
AHBL_CTR_HMASTLOCK	In	1	—
AHBL_CTR_HWDATA	In	32	Write data
AHBL_CTR_HRDATA	Out	32	Read data
AHBL_CTR_HREADY	Out	1	Transaction is done.
AHBL_CTR_HRESP	Out	1	Fixed to 0.

Note:

1. Refer to the [AMBA 3 AHB-Lite Protocol Specification](#) for more detailed descriptions of these responses.

2.4.3. Interrupt Interface

Table 2.6. Interrupt Ports

Name	Type	Width	Description
Irq	In	1	Peripheral interrupts.

2.5. Attribute Summary

The configurable attributes of the RISC-V AHB-L IOPMP IP are described in [Table 2.7](#).

The attributes can be configured through the Lattice Propel Builder software.

Table 2.7. Attributes Description

Attribute	Description
ERROR ID	ID number. Used for RRID. If there are more than one RISC-V AHB-L IOPMP module, the ERROR ID should be set separately.

3. RISC-V AHB-L IOPMP IP Generation

This section provides information on how to generate the RISC-V AHB-L IOPMP IP module using the Lattice Propel Builder software.

To generate the RISC-V AHB-L IOPMP IP module:

1. In the Lattice Propel Builder software, create a new design. Select the AHB-L IOPMP package.
2. Enter the component name. Click **Next**, as shown in [Figure 3.1](#).

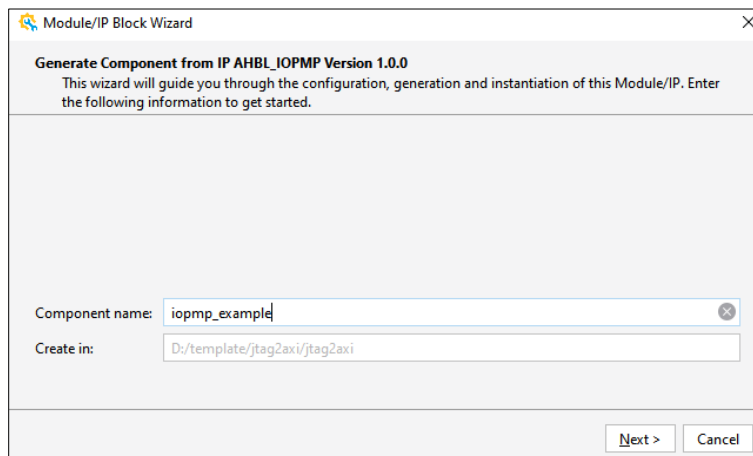


Figure 3.1. Entering Component Name

3. Configure the parameters as needed. Click **Generate** ([Figure 3.2](#)).

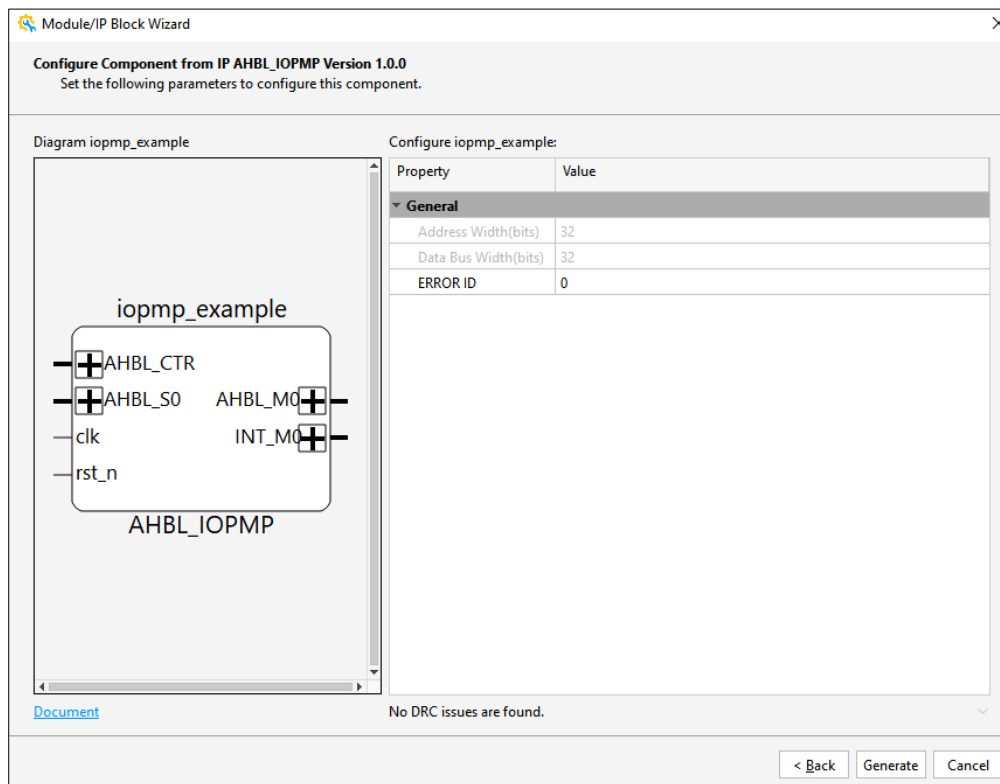


Figure 3.2. Configuring Parameters

4. Verify the information. Click **Finish** (Figure 3.3).

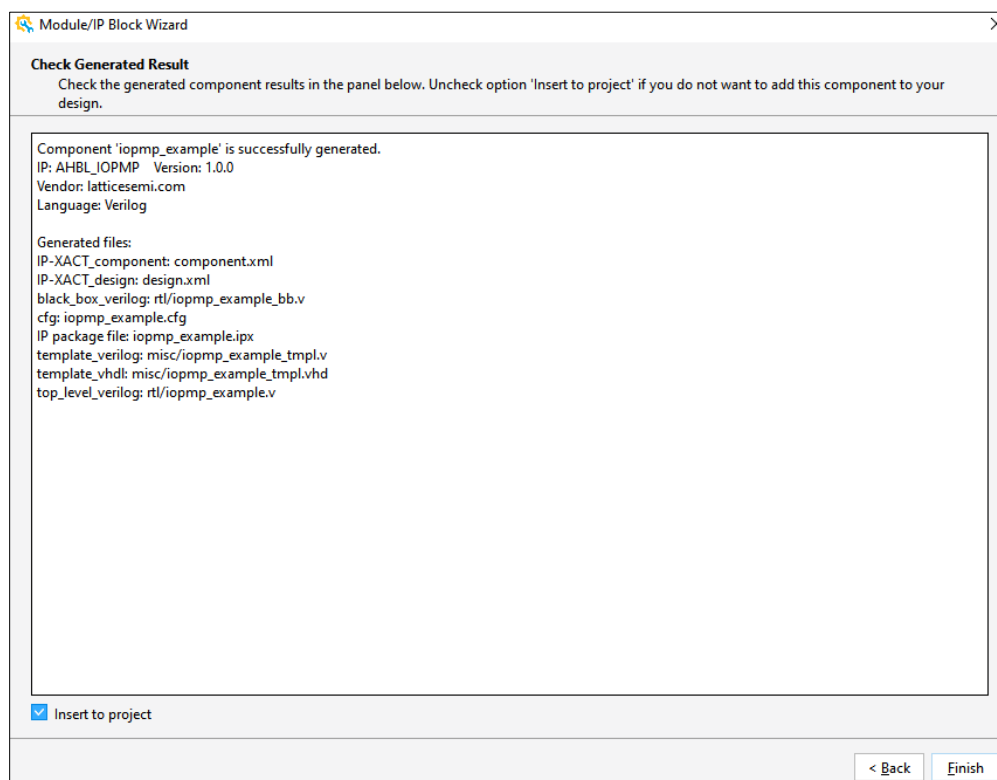


Figure 3.3. Verifying Results

5. Confirm or modify the module instance name. Click **OK** (Figure 3.4).

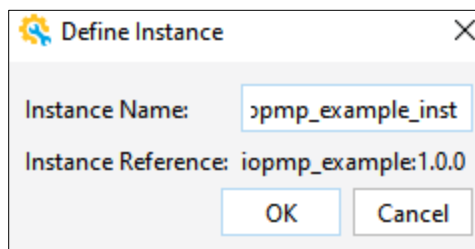


Figure 3.4. Specifying Instance Name

6. The RISC-V AHB-L IOPMP IP instance is successfully generated, as shown in Figure 3.5.

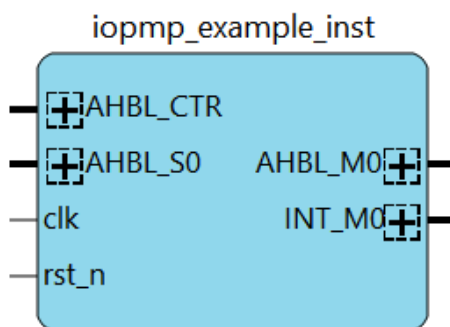


Figure 3.5. Generated Instance

Appendix A. Resource Utilization

Table A.1. Resource Utilization in LFCPNX-100 Device

Configuration	LUTs	Registers	sysMEM EBRs
RISC-V AHB-L IOPMP	541	411	0

Table A.2. Resource Utilization in LAV-AT-E70 Device

Configuration	LUTs	Registers	sysMEM EBRs
RISC-V AHB-L IOPMP	514	411	0

References

- [Lattice Propel Builder 2025.1 User Guide \(FPGA-UG-02235\)](#)
- [Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide \(FPGA-UG-02039\)](#)
- [AMBA 3 AHB-Lite Protocol Specification](#)
- [RISC-V IOPMP Architecture Specification](#)

For more information, refer to:

- [Lattice Propel web page](#)
- [Lattice Certus-N2 Family Devices web page](#)
- [Lattice Avant-E Family Devices web page](#)
- [Lattice Avant-G Family Devices web page](#)
- [Lattice Avant-X Family Devices web page](#)
- [MachXO5-NX Family Devices web page](#)
- [Certus-NX Family Devices web page](#)
- [CertusPro-NX Family Devices web page](#)
- [CrossLink-NX Family Devices web page](#)
- [Lattice Insights for Training Series and Learning Plans](#)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, IP v1.0.0, June 2025

Section	Change Summary
All	Production release.



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