Mutex IP – Lattice Propel Builder 2025.1

IP Version: v1.0.0

User Guide

FPGA-IPUG-02285-1.0

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AXI	Advanced eXtensible Interface
CPU	Central Processing Unit
RISC-V	Reduced Instruction Set Computer-V (Five)
FPGA	Field Programmable Gate Array
GUI	Graphic User Interface
HDL	Hardware Description Language
IP	Intellectual Property
IRQ	Interrupt Request
LUT	Look Up Table
WARL	Write Any Read Legal

1. Introduction

The Lattice Semiconductor Mutex IP is used in multi-processor environment to solve the competition of the shared resources between different processors. The Mutex provides a configurable number of registers for processors to claim they gain exclusive access to particular resources, like shared memory space or shared peripherals.

The Mutex IP is implemented using Verilog HDL and it can be configured and generated using the Lattice Propel™ Builder software. The IP supports Certus™-N2, Lattice Avant™, MachXO5™-NX, CrossLinkU™-NX, CrossLink™-NX, CertusPro™-NX, and Certus-NX FPGA devices.

1.1. Quick Facts

Table 1.1 presents a summary of the Mutex IP.

Table 1.1. Mutex IP Quick Facts

IP Requirements	Supported Devices	Certus-N2, Lattice Avant, MachXO5-NX, CrossLinkU-NX, CrossLink-NX, CertusPro-NX, and Certus-NX
Resource Utilization	Supported User Interfaces	AXI-Lite Interface and AHB-Lite Interface
	Resources	See Table A.1 and Table A.2.
Design Tool Support	Lattice Implementation	IP v1.0.0 – Lattice Propel Builder 2025.1, Lattice Radiant™ Software 2025.1
	Simulation	For a list of supported simulators, see the Lattice Radiant software user guide.

1.2. Features

The Mutex IP has the following features:

- AXI-Lite interface and AHB-Lite interface
- Configurable number of mutex
- Configurable interface numbers
- Configurable CPUID width to clarify the owner of mutex
- Selectable hardware identification support

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal Names that end with:

- _n are active low.
- _i are input signals.
- _o are output signals.
- _io are bi-directional input/output signals.

1.4. Licensing and Ordering Information

The Mutex IP is provided at no additional cost with the Lattice Propel design environment. The IP can be fully evaluated in hardware without requiring an IP license string.

2. Functional Descriptions

2.1. Overview

In a multi-processor system, there can be multiple processors sharing the same resources, such as memory space or peripherals. The Mutex IP provides several mutex registers for processors to claim exclusive access to one or more resources. A typical connection of the Mutex IP is shown in Figure 2.1.

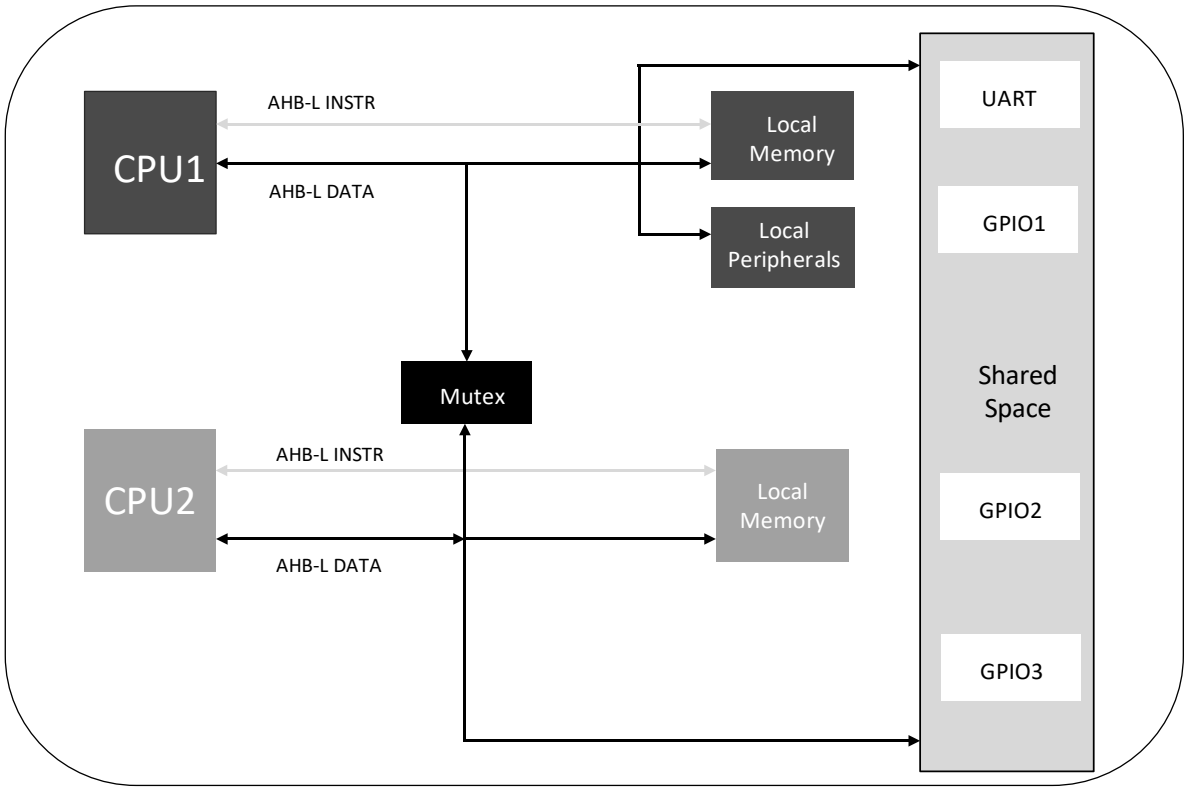

Figure 2.1. Mutex IP Diagram

2.2. Modules Description

2.2.1. Bus Interface

The Mutex IP supports two to eight bus interfaces for a multi-processor system. The interface type can be set as the AXI-Lite interface or the AHB-Lite interface.

2.2.2. Registers

The Mutex IP provides configurable numbers of mutex register. Each mutex register contains a lock bit and a field to claim the identification of the processor. The mutex registers provide a mechanism for mutual exclusion.

Table 2.1. Register Memory Map

Address	Register Name	Access	Description	Fields
0x100 * i	Mutex[i]	WARL	Mutex Register, i = 0 to Mutex_Number	[ID_WIDTH:1] Identification: CPUID to clarify the owner of the mutex. [0] Lock: Indicates whether the mutex is locked. • 0 = Mutex is free. • 1 = Mutex is locked.

2.3. Program Process

To lock a mutex register:

1. Write the Identification field of the target mutex register and set the Lock bit to one.
2. Read back the mutex register to verify the ownership of the register and the status of the lock bit. If the identification field matches the current processor, then the mutex register is owned by the processor.

To free a mutex register:

1. Write the identification field of the mutex register and set the lock bit to zero.
2. Read back the mutex register to verify that the ownership no longer belongs to the current processor.

If Port Protection is checked, when the processor is trying to lock one mutex register, its port ID is stored in another register. The same port ID is later used to free the locked mutex register. It protects the mutex from being unlocked by other processors using the same Identification number.

2.4. Signal Description

Table 2.2 to Table 2.4 list the ports of the soft IP in different categories.

2.4.1. Clock and Reset

Table 2.2. Clock and Reset Ports

Name	Direction	Width	Description
clk	In	1	Mutex soft IP clock.
rst_n	In	1	Global reset, active low.

2.4.2. AXI-Lite Interface

Table 2.3. AXI-Lite Subordinate Ports

Name	Direction	Width	Group	Description
AWREADY_Sx	Out	1	AXI4 Mandatory Write Address Channel	—
AWVALID_Sx	In	1		—
AWADDR_Sx	In	32		—

Name	Direction	Width	Group	Description
AWPROT_Sx	In	3		Not implemented.
WREADY_Sx	Out	1	AXI4 Mandatory Write Data Channel	—
WVALID_Sx	In	1		—
WDATA_Sx	In	32		—
WSTRB_Sx	In	4		—
BVALID_Sx	Out	1	AXI4 Mandatory Write Response Channel	—
BRESP_Sx	Out	2		b'00: OKAY[1] b'10: SLVERR[1] b'11: DECERR[1]
BREADY_Sx	In	1		—
ARVALID_Sx	In	1	AXI4 Mandatory Read Address Channel	—
ARREADY_Sx	Out	1		—
ARADDR_Sx	In	32		—
RDATA_Sx	Out	32		—
RRESP_Sx	Out	2		b'00: OKAY[1] b'10: SLVERR[1] b'11: DECERR[1]
RVALID_Sx	Out	1		—
RREADY_Sx	In	1		—

Note:

1. Refer to the AMBA AXI Protocol Specification for more detailed descriptions of these responses.
2. Sx represents the subordinate number from 0 to 7.

2.4.3. AHB-Lite Interface

Table 2.4. AHB-Lite Subordinate Ports

Name	Direction	Width	Description
AHBL_Sx_HADDR	In	32	—
AHBL_Sx_HWRITE	In	1	—
AHBL_Sx_HSIZE	In	3	—
AHBL_Sx_HPROT	In	4	Not implemented.
AHBL_Sx_HTRANS	In	2	—
AHBL_Sx_HBURST	In	3	Not implemented.
AHBL_Sx_HMASTLOCK	In	1	Not implemented.
AHBL_Sx_HWDATA	In	32	—
AHBL_Sx_HRDATA	Out	32	—
AHBL_Sx_HREADY	Out	1	—
AHBL_Sx_HRESP	Out	1	—

Note:

1. Refer to the AMBA3 AHBL Protocol Specification for more detailed descriptions of these responses.
2. Sx represents the subordinate number from 0 to 7.

2.5. Attribute Summary

The configurable attributes of the Mutex IP are described in Table 2.5. .

The attributes can be configured through the Lattice Propel Builder software.

Table 2.5. Attributes Summary

Attribute	Selectable Values	Default	Dependency on Other Attributes
Mutex Number	1 to 16	2	—
Port Number	2 to 8	2	—
Port Protection	Checked, Unchecked	Unchecked	—
CPU ID Width	clog(Port_Number)1 to 5	4	—
Interface Type	AXI-L, AHB-L	AXI-L	—

Note:

1. clog(x) = ceil($\log_2$(x)). The Minimum integer is greater than $\log_2$ of port number.

Table 2.6. Attributes Description

Attribute	Description
Mutex Number	Total mutex register number
Port Number	Number of bus interfaces
Port Protection	Hardware protection option
CPU ID Width	The bit width of ID number
Interface Type	Bus interfaces type

3. Mutex IP Generation

This section provides information on how to generate the Mutex IP module using the Lattice Propel Builder software.

To generate the Mutex IP module:

1. In the Lattice Propel Builder software, create a new design. Select the Mutex package.
2. Enter the component name. Click **Next**, as shown in Figure 3.1.

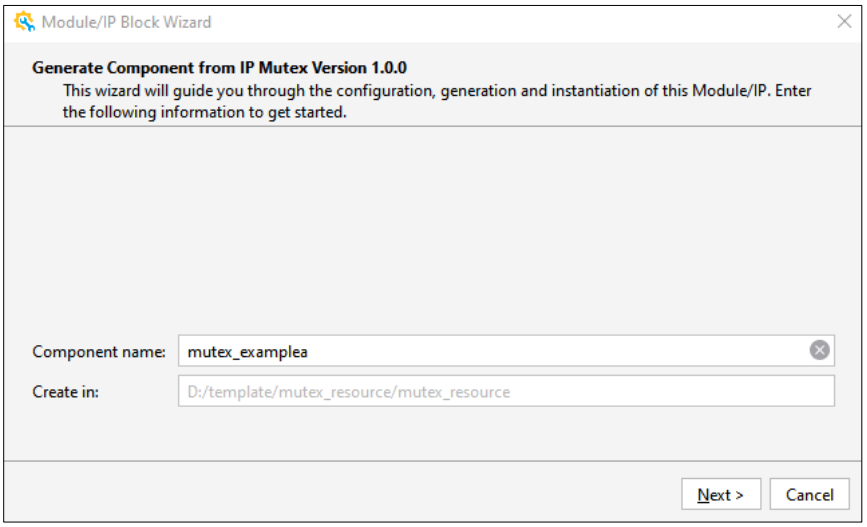

Figure 3.1. Entering Component Name

3. Configure the parameters as needed. Click **Generate** (Figure 3.2).

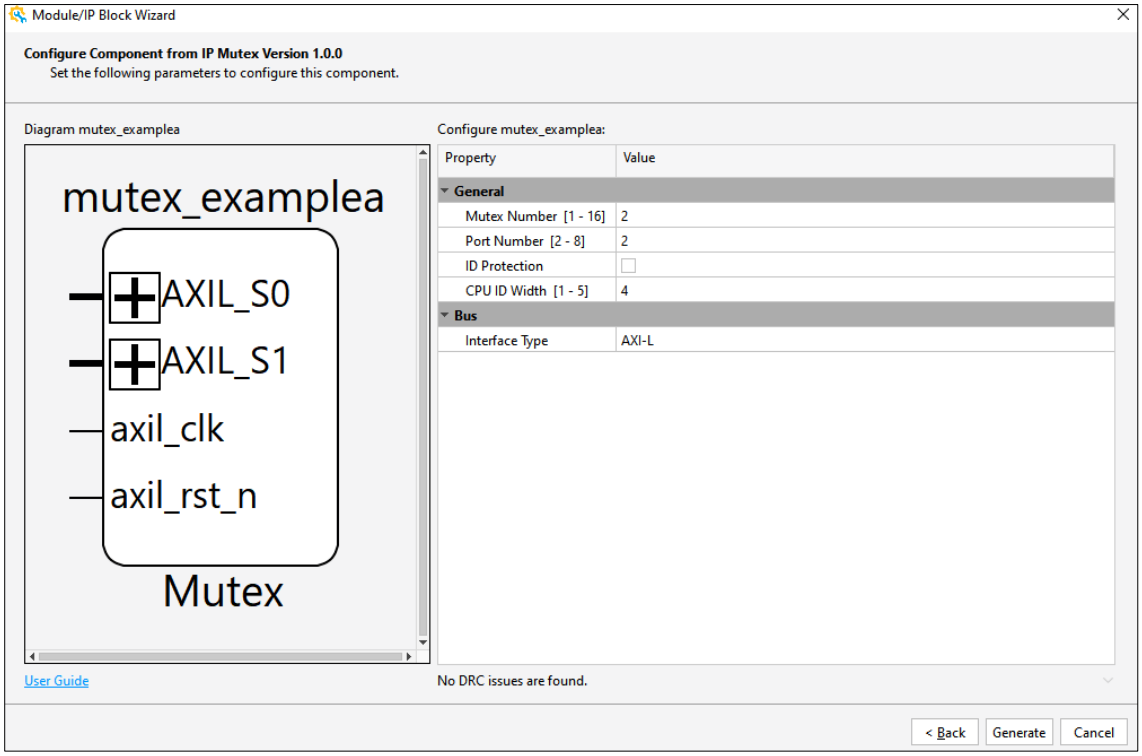

Figure 3.2. Configuring Parameters

4. Verify the information. Click **Finish** (Figure 3.3).

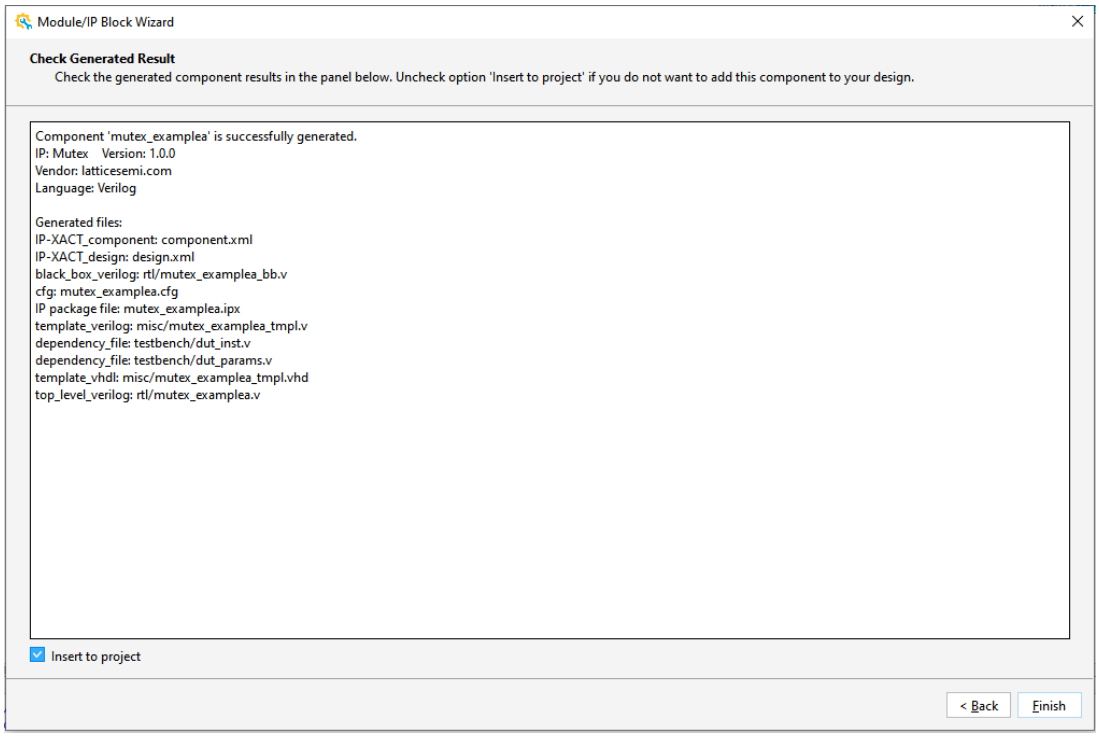

Figure 3.3. Verifying Results

5. Confirm or modify the module instance name. Click **OK** (Figure 3.4).

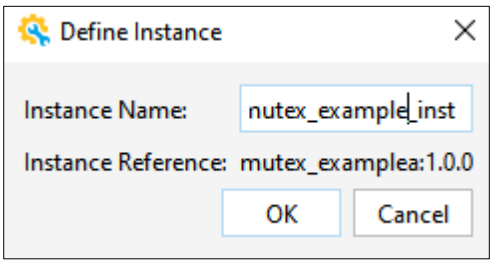

Figure 3.4. Specifying Instance Name

6. The Mutex IP instance is successfully generated, as shown in Figure 3.5.

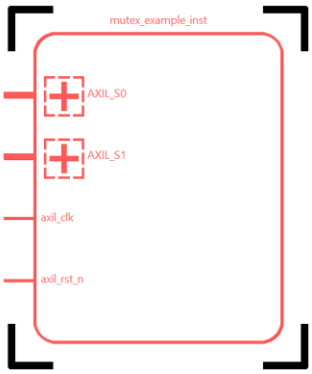

Figure 3.5. Generated Instance

Appendix A. Resource Utilization

Table A.1. Resource Utilization in CertusPro-NX-100 Device

Configuration	LUTs	Registers
Mutex_Number = 2, Port_Number = 2, Port Protection = 0, ID WIDTH = 4, Interface = AHB-L	67	34
Mutex_Number = 2, Port_Number = 2, Port Protection = 1, ID WIDTH = 4, Interface = AHB-L	71	36
Mutex_Number = 16, Port_Number = 2, Port Protection = 0, ID WIDTH = 4, Interface = AHB-L	329	104
Mutex_Number = 16, Port_Number = 2, Port Protection = 1, ID WIDTH = 4, Interface = AHB-L	402	120
Mutex_Number = 16, Port_Number = 8, Port Protection = 0, ID WIDTH = 4, Interface = AHB-L	1805	238
Mutex_Number = 16, Port_Number = 8, Port Protection = 1, ID WIDTH = 4, Interface = AHB-L	1966	313
Mutex_Number = 2, Port_Number = 2, Port Protection = 0, ID WIDTH = 4, Interface = AXI-L	85	60
Mutex_Number = 16, Port_Number = 8, Port Protection = 0, ID WIDTH = 4, Interface = AXI-L	1805	327
Mutex_Number = 16, Port_Number = 8, Port Protection = 1, ID WIDTH = 4, Interface = AXI-L	2308	404

Table A.2. Resource Utilization in LAV-AT-E70 Device

Configuration	LUTs	Registers
Mutex_Number = 2, Port_Number = 2, Port Protection = 0, ID WIDTH = 4, Interface = AHB-L	56	34
Mutex_Number = 2, Port_Number = 2, Port Protection = 1, ID WIDTH = 4, Interface = AHB-L	60	36
Mutex_Number = 16, Port_Number = 2, Port Protection = 0, ID WIDTH = 4, Interface = AHB-L	330	118
Mutex_Number = 16, Port_Number = 2, Port Protection = 1, ID WIDTH = 4, Interface = AHB-L	398	140
Mutex_Number = 16, Port_Number = 8, Port Protection = 0, ID WIDTH = 4, Interface = AHB-L	1694	240
Mutex_Number = 16, Port_Number = 8, Port Protection = 1, ID WIDTH = 4, Interface = AHB-L	1948	289
Mutex_Number = 2, Port_Number = 2, Port Protection = 0, ID WIDTH = 4, Interface = AXI-L	77	60
Mutex_Number = 16, Port_Number = 8, Port Protection = 0, ID WIDTH = 4, Interface = AXI-L	1623	339
Mutex_Number = 16, Port_Number = 8, Port Protection = 1, ID WIDTH = 4, Interface = AXI-L	2107	407

References

- Lattice Propel Builder 2025.1 User Guide (FPGA-UG-02235)
- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)
- AMBA AXI and ACE Protocol Specification

For more information, refer to:

- Lattice Propel web page
- Lattice Certus-N2 Family Devices web page
- Lattice Avant-E Family Devices web page
- Lattice Avant-G Family Devices web page
- Lattice Avant-X Family Devices web page
- MachXO5-NX Family Devices web page
- Certus-NX Family Devices web page
- CertusPro-NX Family Devices web page
- CrossLink-NX Family Devices web page
- Lattice Insights for Training Series and Learning Plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, IP v1.0.0, June 2025

Section	Change Summary
All	Production release.

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