Mailbox IP – Lattice Propel Builder 2025.1

IP Version: v1.0.0

User Guide

FPGA-IPUG-02284-1.0

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Contents

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AXI-Lite	Advanced eXtensible Interface – Lite
AHB-Lite	Advanced High-Performance Bus – Lite
CPU	Central Processing Unit
FIFO	First In First Out
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input/Output
HDL	Hardware Description Language
IP	Intellectual Property
IRQ	Interrupt Request
LUT	Look Up Table
UART	Universal Asynchronous Receiver/Transmitter
W1C	Write One Clear

1. Introduction

The Lattice Semiconductor Mailbox IP is designed for a multi-processor environment that requires sharing data between each processor. The mailbox IP provides a bi-directional communication interface between two processors. The IP can be connected to the processor through AHB-Lite or AXI-Lite interfaces.

The Mailbox IP is implemented using Verilog HDL and it can be configured and generated using the Lattice Propel™ Builder software. The IP supports Certus™-N2, Lattice Avant™, MachXO5™-NX, CrossLinkU™-NX, CrossLink™-NX, CertusPro™-NX, and Certus-NX FPGA devices.

1.1. Quick Facts

Table 1.1 presents a summary of the Mailbox IP.

Table 1.1. Mailbox IP Quick Facts

IP Requirements	Supported Devices	Certus-N2, Lattice Avant, MachXO5-NX, CrossLinkU-NX, CrossLink-NX, CertusPro-NX, and Certus-NX
Resource Utilization	Supported User Interfaces	AXI-Lite Interface and AHB-Lite Interface
	Resources	See Table A.1.
Design Tool Support	Lattice Implementation	IP v1.0.0 – Lattice Propel Builder 2025.1, Lattice Radiant™ Software 2025.1
	Simulation	For a list of supported simulators, see the Lattice Radiant software user guide.

1.2. Features

The Mailbox IP has the following features:

- AXI-Lite interface and AHB-Lite interface
- Configurable depth of mailbox
- Configurable interrupt thresholds and maskable interrupts

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal Names that end with:

- _n are active low.
- _i are input signals.
- _o are output signals.
- _io are bi-directional input/output signals.

1.4. Licensing and Ordering Information

The Mailbox IP is provided at no additional cost with the Lattice Propel design environment. The IP can be fully evaluated in hardware without requiring an IP license string.

2. Functional Descriptions

2.1. Overview

The Mailbox IP is used for multi-processor SoCs for bi-directional communications between two processors or two subsystems. Figure 2.1 shows a typical connection for the AHB-Lite system to share data between CPU1 and CPU2. You can configure the interrupt threshold and the Mailbox IP can notify the processors to start to receive data or stop sending data. The data flow is FIFO-based. You may select the FIFO implementation and FIFO depth through configurable attributes.

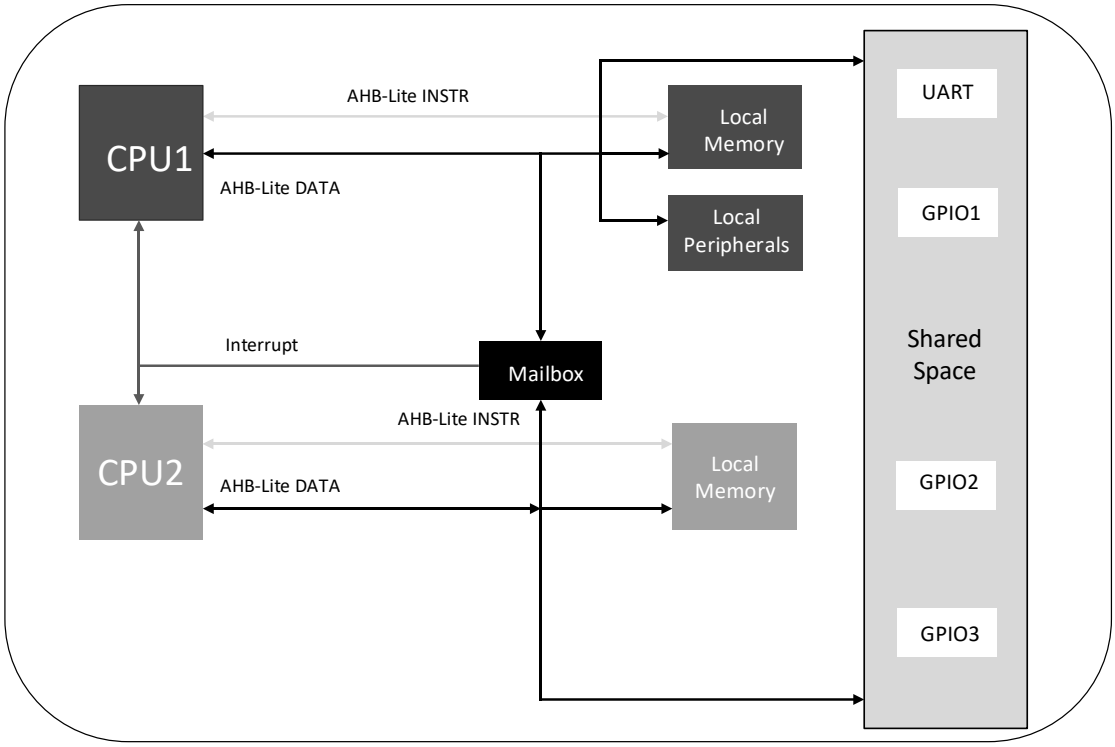

Figure 2.1. Mailbox IP Diagram

2.2. Modules Description

2.2.1. Bus Interface

The Mailbox IP has two data bus interfaces to access internal memory-mapped registers. These interfaces need to be connected to different processors in a multi-processor system. Each interface can be configured as AXI-Lite or AHB-Lite.

2.2.2. Registers

- Read and Write Data Registers: Processors can send data to or receive data from these registers. The registers are FIFO-based, and the depth can be configured through attributes.
- Status Registers: Processors can access these registers to get the status of the IP.
- Interrupt Registers: Processors can handle the interrupt behaviors, such as interrupt thresholds, mask, and interrupts status through these registers.

Table 2.1. Register Memory Map

Address	Register Name	Access	Description	Fields
0x00	FIFO_WR	Write-Only	Write Data address	[31:0] Write data
0x08	FIFO_RD	Read-Only	Read Data address	[31:0] Read data
0x10	Status	Read-Only	Status of Mailbox	[31] Empty: • 0 = There is data in the Receive FIFO. • 1 = The Receive FIFO is empty. [30] Full: • 0 = The Send FIFO can receive more data. • 1 = The Send FIFO is full. [29]: Almost Full: • 0 = The Send FIFO level is greater than the WR_Thresholds. • 1 = The Send FIFO level is less or equal to the WR_Thresholds. [28]: Almost Empty: • 0 = The Receive FIFO level is less or equal to the RD_Thresholds. • 1 = The Receive FIFO level is greater than the RD_Thresholds.
0x14	Error	Read-Only	Error Flags. A read clears the status.	[31] Empty Error: Asserts when the processor tries to read the Empty FIFO. The read is ignored. [30] Full Error: Assert when the processor tries to write the Full FIFO. The write is ignored.
0x18	WR_Thresholds	Read-Write	Threshold to raise the write interrupt.	[31:0] Write Thresholds: Thresholds for the Send FIFO
0x1C	RD_Thresholds	Read-Write	Threshold to raise the read interrupt	[31:0] Read Thresholds: Thresholds for the Receive FIFO
0x20	IRQ_STATUS	Read-W1C	Interrupt status	[31]: Write Threshold Interrupt: The Send FIFO level is greater than WR_Threshold. [30]: Read Threshold Interrupt: The Receive FIFO level is greater than or equal to RD_Threshold. [29]: Error Interrupt: The mailbox IP encounters a read or write error.
0x24	IRQ_ENABLE	Read-Write	Enable each type of interrupts	[31]: Write Threshold Interrupt Enable [30]: Read Threshold Interrupt Enable [29]: Error Interrupt Enable

Address	Register Name	Access	Description	Fields
0x28	IRQ_PENDING	Read-only	Current pending interrupts.	[31]: Write Threshold Interrupt Pending [30]: Read Threshold Interrupt Pending [29]: Error Interrupt Pending

2.3. Signal Description

Table 2.2 to Table 2.5 list the ports of the soft IP in different categories.

2.3.1. Clock and Reset

Table 2.2. Clock and Reset Ports

Name	Direction	Width	Description
port0_clk	In	1	Mailbox port 0 system clock.
port1_clk	In	1	Mailbox port 1 system clock.
port0_rst_n	In	1	Port 0 global reset, active low.
port1_rst_n	In	1	Port 1 global reset, active low.

2.3.2. AXI-Lite Interface

Table 2.3. AXI-Lite Subordinate Ports

Name	Direction	Width	Group	Description
AWREADY_Sx	Out	1	AXI4 Mandatory Write Address Channel	—
AWVALID_Sx	In	1		—
AWADDR_Sx	In	32		—
AWPROT_Sx	In	3		Not implemented.
WREADY_Sx	Out	1	AXI4 Mandatory Write Data Channel	—
WVALID_Sx	In	1		—
WDATA_Sx	In	32		—
WSTRB_Sx	In	4		—
BVALID_Sx	Out	1	AXI4 Mandatory Write Response Channel	—
BRESP_Sx	Out	2		b'00: OKAY[1] b'10: SLVERR[1] b'11: DECERR[1]
BREADY_Sx	In	1		—
ARVALID_Sx	In	1	AXI4 Mandatory Read Address Channel	—
ARREADY_Sx	Out	1		—
ARADDR_Sx	In	32		—
RDATA_Sx	Out	32		—
RRESP_Sx	Out	2		b'00: OKAY[1] b'10: SLVERR[1] b'11: DECERR[1]
RVALID_Sx	Out	1		—
RREADY_Sx	In	1		—

Note:

1. Refer to the AMBA AXI Protocol Specification for more detailed descriptions of these responses.
2. Sx represents the subordinate number from 0 to 7.

2.3.3. AHB-Lite Interface

Table 2.4. AHB-Lite Subordinate Ports

Name	Direction	Width	Description
AHBL_Sx_HADDR	In	32	—
AHBL_Sx_HWRITE	In	1	—
AHBL_Sx_HSIZE	In	3	—
AHBL_Sx_HPROT	In	4	Not implemented.
AHBL_Sx_HTRANS	In	2	—
AHBL_Sx_HBURST	In	3	Not implemented.
AHBL_Sx_HMASTLOCK	In	1	Not implemented.
AHBL_Sx_HWDATA	In	32	—
AHBL_Sx_HRDATA	Out	32	—
AHBL_Sx_HREADY	Out	1	—
AHBL_Sx_HRESP	Out	1	—

Note:

1. Refer to the AMBA3 AHBL Protocol Specification for more detailed descriptions of these responses.
2. Sx represents the subordinate number from 0 to 7.

2.3.4. Interrupt Interface

Table 2.5. Interrupt Ports

Name	Type	Width	Description
Irq0	Out	1	Interrupt for Port0.
Irq1	Out	1	Interrupt for Port1.

2.4. Attribute Summary

The configurable attributes of the Mailbox IP are listed and described in Table 2.6 and Table 2.7.

The attributes can be configured through the Lattice Propel Builder software.

Table 2.6. Configurable Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
Mailbox FIFO Depth	16 to 8192 four-byte words	16	—
Mailbox FIFO Type	EBR, Distributed-RAM	EBR	—
Enable Output Register	Checked, Unchecked	Unchecked	—
Write Threshold Reset Value	1 to (FIFO Depth – 1)	15	—
Read Threshold Reset Value	1 to (FIFO Depth – 1)	1	—
Interface Type	AXI-L, AHB-L	AXI-L	—

Table 2.7. Attributes Description

Attribute	Description
Mailbox FIFO Depth	Mailbox FIFO depth
Mailbox FIFO Type	Mailbox FIFO implementation type
Enable Output Register	FIFO output register
Write Threshold Reset Value	FIFO WR_Threshold reset value
Read Threshold Reset Value	FIFO RD_Threshold reset value
Interface Type	Memory-mapped register interface type

3. Mailbox IP Generation

This section provides information on how to generate the Mailbox IP module using the Lattice Propel Builder software.

To generate the Mailbox IP module:

1. In the Lattice Propel Builder software, create a new design. Select the Mailbox package.
2. Enter the component name. Click **Next**, as shown in Figure 3.1.

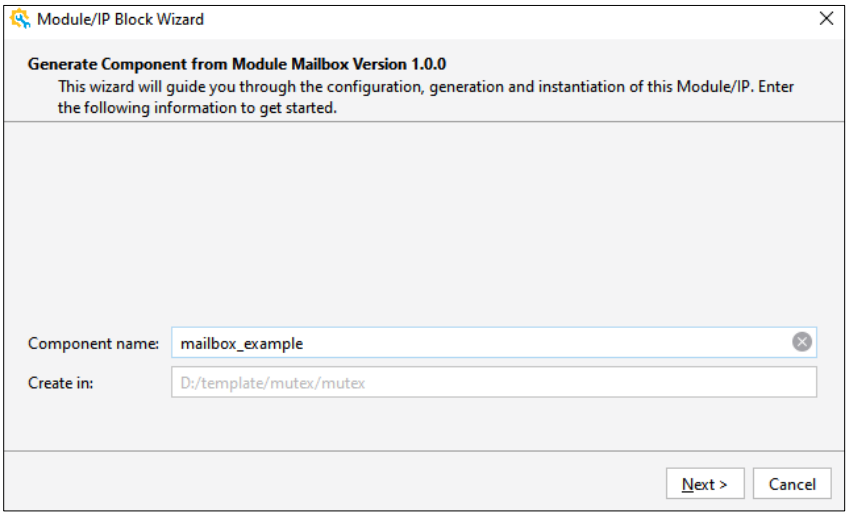

Figure 3.1. Entering Component Name

3. Configure the parameters as needed. Click **Generate** (Figure 3.2).

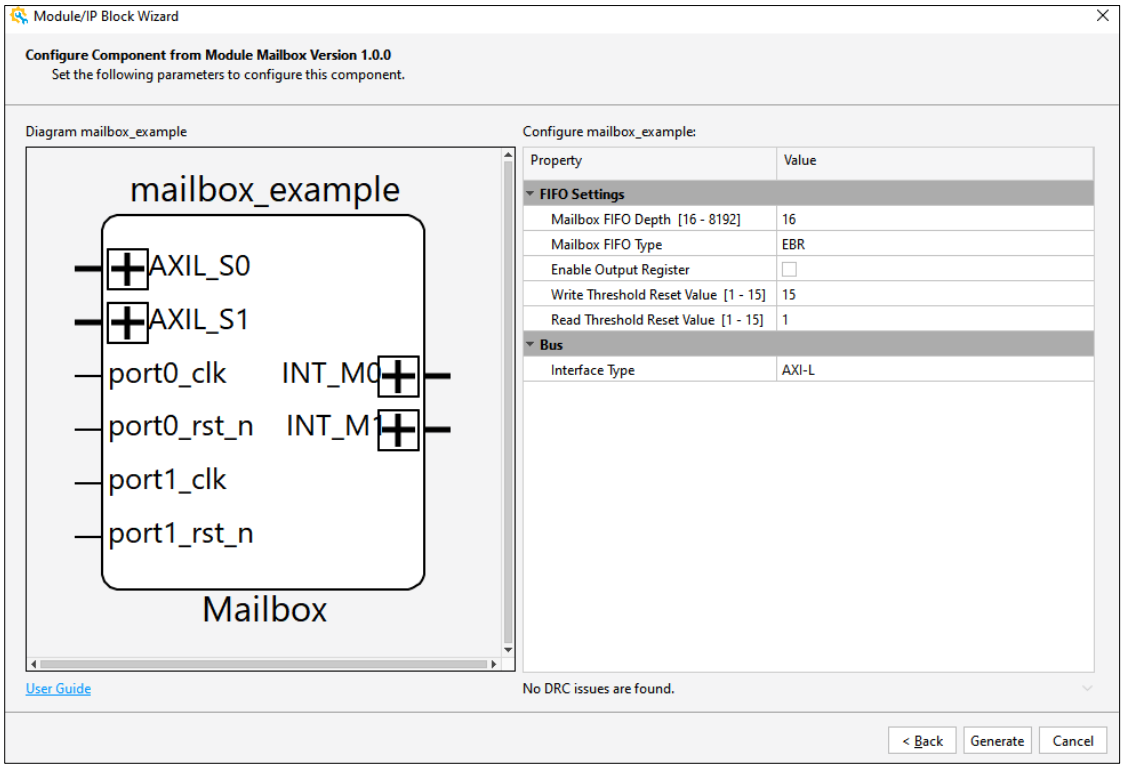

Figure 3.2. Configuring Parameters

4. Verify the information. Click **Finish** (Figure 3.3).

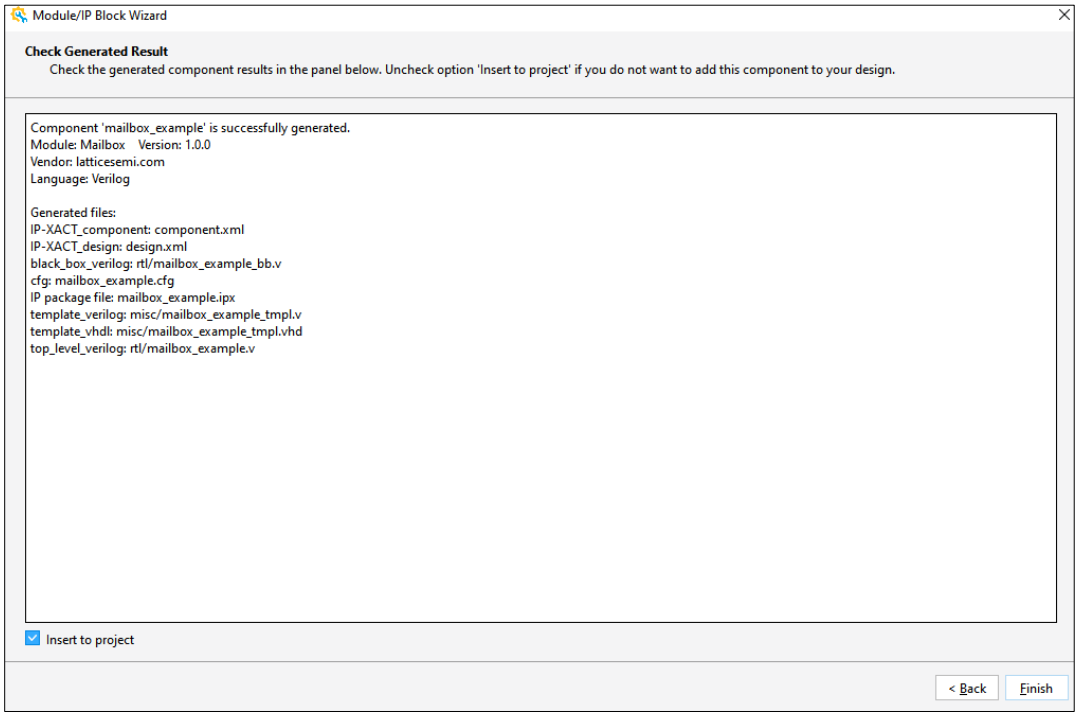

Figure 3.3. Verifying Results

5. Confirm or modify the module instance name. Click **OK** (Figure 3.4).

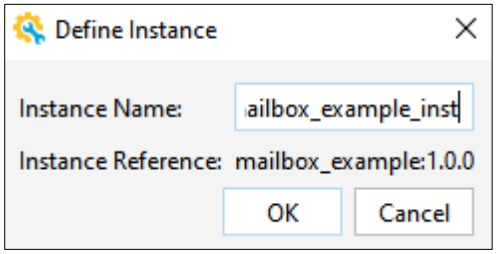

Figure 3.4. Specifying Instance Name

6. The Mailbox IP instance is successfully generated, as shown in Figure 3.5.

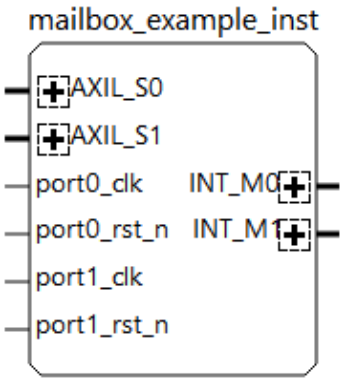

Figure 3.5. Generated Instance

Appendix A. Resource Utilization

Table A.1. Resource Utilization in LFCPNX-100 Device

Configuration	LUTs	Registers	sysMEM EBRs
Interface = AHB-Lite, FIFO Depth = 16, FIFO Type = EBR	360	195	2
Interface = AHB-Lite, FIFO Depth = 16, FIFO Type = Distributed-RAM	456	259	0
Interface = AHB-Lite, FIFO Depth = 8192, FIFO Type = EBR	759	440	32

Table A.2. Resource Utilization in LAV-AT-E70 Device

Configuration	LUTs	Registers	sysMEM EBRs
Interface = AHB-Lite, FIFO Depth = 16, FIFO Type = EBR	341	183	2
Interface = AHB-Lite, FIFO Depth = 16, FIFO Type = Distributed-RAM	441	247	0
Interface = AHB-Lite, FIFO Depth = 8192, FIFO Type = EBR	728	404	16

References

- Lattice Propel Builder 2025.1 User Guide (FPGA-UG-02235)
- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)
- AMBA AXI and ACE Protocol Specification
- AMBA 3 AHB-Lite Protocol Specification

For more information, refer to:

- Lattice Propel web page
- Lattice Certus-N2 Family Devices web page
- Lattice Avant-E Family Devices web page
- Lattice Avant-G Family Devices web page
- Lattice Avant-X Family Devices web page
- MachXO5-NX Family Devices web page
- Certus-NX Family Devices web page
- CertusPro-NX Family Devices web page
- CrossLink-NX Family Devices web page
- Lattice Insights for Training Series and Learning Plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, IP v1.0.0, June 2025

Section	Change Summary
All	Production release.

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