DDR Memory PHY Module

IP Version: v2.5.0

Release Notes

FPGA-RN-02072-1.2

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Contents

1. Introduction

This document contains the Release Notes for the DDR Memory PHY Module IP. For specific details about the IP, refer to the following:

- DDR Memory PHY Module (FPGA-IPUG-02195)

DDR Memory PHY Module IP v2.5.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.2	• Added support for DQ Bit Swizzle within DQS group. • Updated constraints for the PLL instance. • Updated sequence for changing CK delay during auto-CBT to avoid glitch. • Enabled Bit-Level Trim Sweep for 1,600 Mbps and 1,866 Mbps.

DDR Memory PHY Module IP v2.4.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1	• Added support for LAV-AT-G30 and LAV-AT-X30 devices. • Added DRAM and MC Vref settings in the IP GUI. • Added PHY IO settings in the IP GUI. • Updated the ODT default values and removed unused settings in the IP GUI for DDR4. • Added the CS delay attribute in the IP GUI. • Updated Read Latency and Write Latency options for each DDR4 clock frequency. • Removed Enable DBI option for DDR4. • Enhanced DDR4 training routine based on HW validation.

DDR Memory PHY Module IP v2.3.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2.1	• Improved the LPDDR4 bit-level trim sweep. • Added 2D Vref training. • Improved PLL clock frequency change sequence to not lose lock. • Removed DDR3L and DDR5 options because they are not yet hardware validated.

DDR Memory PHY Module IP Earlier Versions

IP Version	Summary of Changes
2.2.0	• Added support for LN2-CT-20 device. • Improved the LPDDR4 bit-level trim sweep.
2.1.0	• Added support for LN2-CT-20 device. • Updated constraints. • Updated PLL.
2.0.0	• Added DDR5 support. • Enhanced DDR4 training based on HW validation.
1.3.0	• Added DDR3L and enhanced DDR4 to support more latencies. Added support for 1,066 MHz and 1,200 MHz DDR clock.
1.2.0	• Added dual rank support.

IP Version	Summary of Changes
1.1.0	• Added DDR4 Support. • Added support for 266 MHz, 666 MHz and 933 MHz DDR clock. • Added PLL lock signal.
1.0.0	• Initial release.

References

- DDR Memory PHY Module (FPGA-IPUG-02195)
- Lattice Avant Platform web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Certus-N2 web page
- IP Core for Avant devices
- Lattice Propel Builder software
- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

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For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase

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