Lattice Avant PLL Module

IP Version: v2.6.0

Release Notes

FPGA-RN-02066-1.0

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Contents

1. Introduction

This document contains the Release Notes for the Lattice Avant PLL Module. For specific details about the IP, refer to the following:

- Lattice Avant PLL Module User Guide (FPGA-IPUG-02220)

Lattice Avant PLL Module v2.6.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	• De-feature Config wait for lock. • Updated constraint. • Added limitation on maximum VCO when using dynamic phase shift with phase advance. • Updated CLKPHY output divider range up to 256.

Lattice Avant PLL Module Earlier Versions

IP Version	Summary of Changes
2.5.0	Added bandwidth initialization logic.
2.4.0	• Set the LOSS_LOCK_DETECTION parameter to disable. • Updated device name.
2.3.0	Restricted feedback divider to integer only when using external clock as feedback.
2.2.0	Updated VCO range and parameter optimization calculation.
2.1.0	• Updated port name in constraint file. • Added the CONFIG_WAIT_FOR_LOCK parameter.
2.0.0	Added support for Lattice Avant devices.

References

- Lattice Avant PLL Module User Guide (FPGA-IPUG-02220)
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Lattice Radiant Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

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