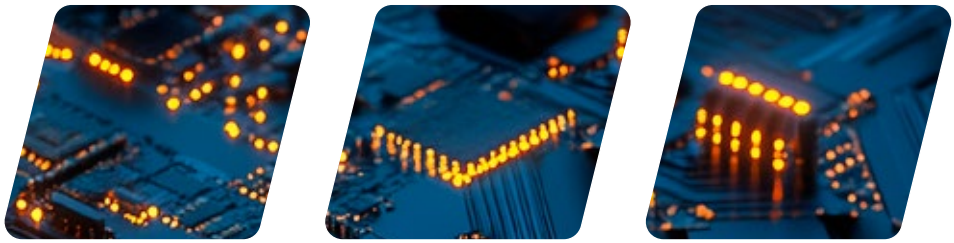
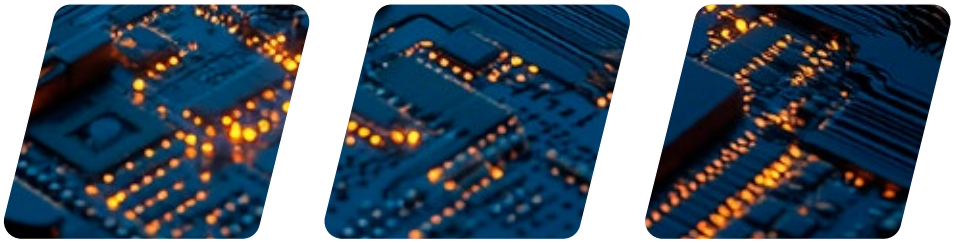


Lattice Nexus™ 2 Platform

Low Power, High Performance Small FPGA



White Paper

Authors:

Peiju Chiang, Product Marketing Manager, Lattice Semiconductor
Steve Hossner, Principal Applications Engineer, Lattice Semiconductor
Jonathan Ley, Applications Technical Project Manager, Lattice Semiconductor
Rohith Sood, Applications Board Development Manager, Lattice Semiconductor

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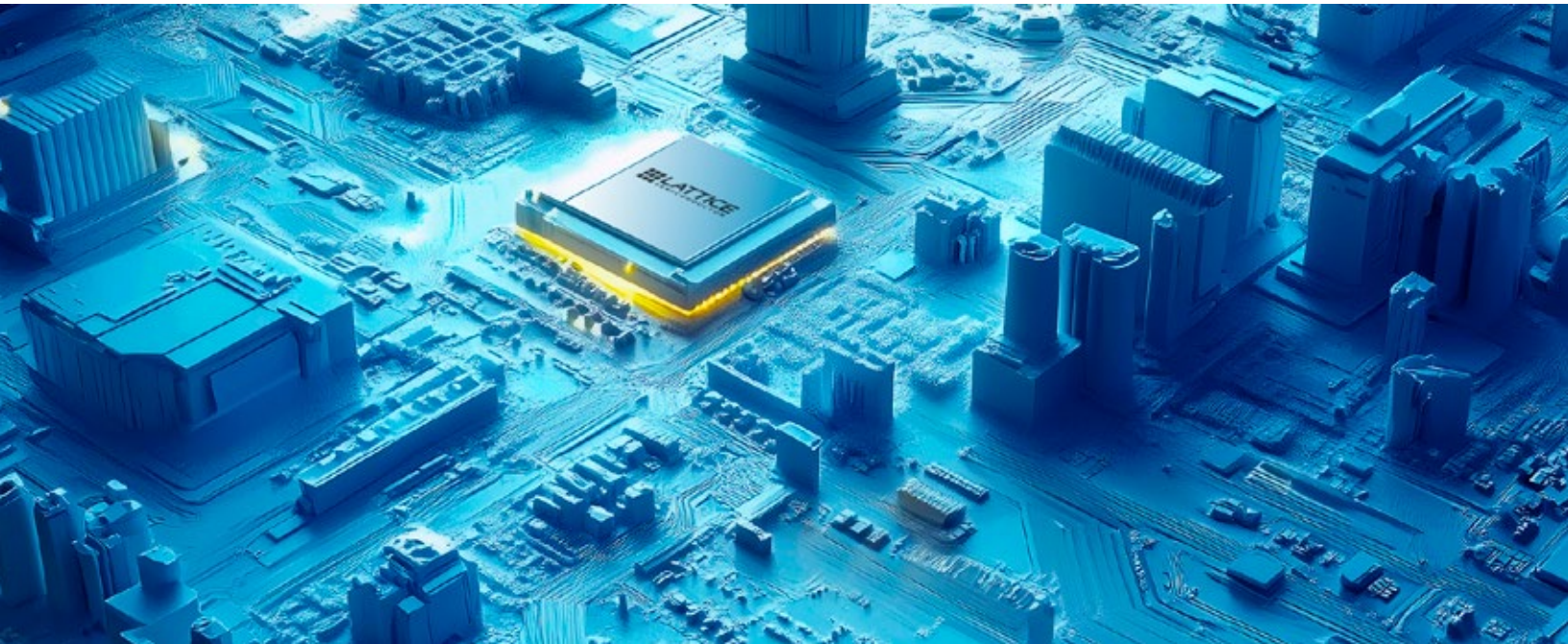
ABSTRACT

A small FPGA platform generally refers to FPGAs with a logic density of under 200k SLC (System Logic Cells), an area where Lattice FPGAs excel. The Lattice Nexus™ 2 FPGA platform is based on the 16 nm process node. This paper presents a comparative analysis of the Lattice Nexus 2 platform against other readily available FPGAs in the same class at the time of its introduction. This analysis covers power consumption, boot time, form factor, and security features. This white paper examines how these factors impact total cost of ownership (TCO) and various applications.



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1. Introduction

Lattice Semiconductor introduced the Lattice Nexus™ platform in 2019, setting a new standard for low power, small size FPGAs. Building on this success, the Lattice Nexus™ 2 platform further enhances these capabilities, offering significant improvements in power efficiency, form factor, boot speed, and security compared to the competition. This white paper explores the key benefits of the Lattice Nexus 2 platform relative to similar competing FPGA devices in the market and highlights applications that benefit from the addition of Lattice Nexus 2 devices to the Lattice small FPGA portfolio.

2. Lattice Nexus 2 Expands Logic and Performance

2.1. LATTICE NEXUS 2 PLATFORM EXPANDED FEATURES

The Lattice Nexus 2 platform complements the original Nexus by expanding its logic density and performance capabilities. In general, Lattice Nexus 2 devices offer close to 2X the logic density, SERDES bandwidth, and external memory interface speed. The following table highlights the differences:

	Lattice Nexus Platform	Lattice Nexus 2 Platform
System Logic Cell Range (KSLC)	21 to 130	65 to 220
Total SERDES Bandwidth	80 Gbps	128 Gbps
Timing Closure	Up to 200 MHz	Up to 350 MHz
MSPI Configuration	Quad SPI Single Data Rate	xSPI Double Data Rate
DSPs	Up to 156	Up to 520
PCI Express	Gen 3	Gen 4
LPDDR4 Data Rate	1066 Mbps	2400 Mbps
Hard MIPI D-PHY Speed	2.5 Gbps	4.5 Gbps
Hard MIPI C-PHY	No	Yes

The Lattice Nexus 2 platform's expanded performance capabilities translate into several tangible benefits:

- **Higher Data Throughput:** Increased SERDES bandwidth and PCI Express support enable faster data transfer rates, crucial for high bandwidth data and video bridging applications.
- **Improved Memory Performance:** Higher LPDDR4 data rates facilitate quicker access to memory, enhancing overall system performance and reduce latency.
- **Faster Flash Configuration:** Doubling the flash interface width from 4 to 8 and improving from single data rate (SDR) to double data rate (DDR) retains instant-on configuration even with increased logic density
- **Enhanced Timing Closure:** Improved timing closure provides greater flexibility in placement and routing, reduced latency, and better resource utilization, supporting more complex applications.
- **More DSPs per Logic:** More DSP blocks allow for more parallel operations on complex algorithms, video processing, and edge AI inferencing and reduce latency to improve real-time application performance.

With these expanded features in the Lattice small FPGA portfolio, developers will have the option to pick the optimal device from the Lattice Nexus or Nexus 2 platforms to meet their design goals.

3. Key Competitive Benefits of Lattice Nexus 2 Platform

Lattice is a leader in small FPGAs. Lattice Nexus FPGA families (Lattice CrossLink™-NX, Lattice Certus™-NX, and Lattice MachXO5™-NX) enable numerous applications that prioritize low power, small size, and reduced total cost of ownership (TCO). The Lattice Nexus 2 platform continues to emphasize these priorities, offering several competitive advantages over its rivals:

- **Up to 20X Faster External Flash Boot:** This improvement ensures fast startup, reduced response time and instant fault recovery, all the important requirements for highly reliable systems.
- **Up to 3X Lower Power Consumption:** The Lattice Nexus 2 platform's optimized architecture can achieve up to 3X lower in power consumption against similar class of FPGAs from the competition.
- **Up to 5X Smaller Form Factor:** Lattice Nexus 2 includes 16 Gbps SERDES in 5X smaller foot-print vs the competition. Developers have more freedom in the placement of components at reduced PCB area.
- **Simplified Power Management:** Lattice Nexus 2 devices use simple power delivery network (PDN) without power sequencing requirement.
- **Best-in-Class Security:** Lattice Nexus 2 incorporates advanced security features to protect against emerging threats, ensuring data integrity and device reliability. Features include AES-GCM, SHA-3, ECDSA, and RSA.

Lattice validated the above from hardware testing and comparing specification in product datasheets and user guides.

3.1. COMPETITIVE COMPARISON AND APPLICATION EXAMPLES

To compare the performance of Lattice Nexus 2 devices against the competition, Lattice selected AMD's Artix™ Ultrascale+ AU20P and Altera's Cyclone® 10GX 220 for a side-by-side comparison with the Lattice Certus-N2 CT20 FPGA. The comparison focused on power consumption, size, configuration time, and total cost of ownership. The results indicated that the Lattice Certus-N2 CT20 FPGA outperforms its competitors in all these categories.

3.2. FAST EXTERNAL FLASH CONFIGURATION

Fast configuration is crucial in any design, especially in safety-critical environments like robotics on a manufacturing floor or in a warehouse. To ensure worker safety, all systems must have instant fault-recovery capabilities. If a system goes down, it needs to recover immediately, which relies on the design's boot-up speed. For instance, if a smart sensor fails, it must resume operation almost instantly to continue monitoring the safety conditions of the manufacturing site.

Similarly, in Automotive zonal gateways, the system must wake up quickly in response to external triggers to ensure the safety of the driver and passengers. A design that supports fast boot-up can remain in a low power state most of the time and react promptly to wake-up signals, enhancing overall efficiency and safety.

3.2.1. COMPARING CONFIGURATION SPEED

The methodology for measuring flash configuration speed is described below

1. All designs are based on RTL (Register Transistor Level). There is no random memory initialization, which increases the configuration file size
2. Configuration image is a plain bitstream without compression
3. No bitstream authentication
4. Devices only use a single configuration flash memory to simulate the lowest BOM
5. Configuration time is measured from the assertion of INIT (excludes the variable power rail ramp-up times) to the assertion of the DONE signal pin

Results are presented in the table below.

	Lattice Certus-N2 CT20	AMD Artix US+ AU20P	Altera Cyclone 10GX 220
Configuration Time	18 ms	261 ms	361 ms
Comparison Factor	1X	14.5X	20X

The measurements indicate that the Lattice Certus-N2 CT20 device is up to 20 times faster than the competition. This is a significant differentiation for the Lattice Nexus 2 Platform.

3.2.2. FACTORS AFFECTING FPGA BOOT TIME

Several factors can impact the configuration time of an FPGA from external flash memory:

1. **Flash Memory Speed:** The read speed of the flash memory directly affects how quickly the configuration data can be transferred to the FPGA.
2. **Clock Frequency:** The clock frequency used for the configuration process affects the data transfer rate.
3. **Interface Type:** The type of interface used between the flash memory and the FPGA (e.g., SPI, parallel, interface width) can significantly impact the data transfer rate.
4. **Configuration Data Size:** Larger bitstreams take longer to transfer and configure.

Let's analyze each factor to understand why Lattice Certus-N2 boots up faster than the competition

3.2.3. HOW DOES LATTICE CERTUS-N2 ACHIEVE FASTER BOOT?

All three FPGAs configure from a similar flash memory structure using their maximum internal configuration clock rate. However, the Lattice Certus-N2 device applies the fastest flash clock frequency amongst the FPGA devices at 160 MHz. Lattice Certus-N2 is followed by the AU20P at 127.5 MHz and the Cyclone 10GX220 at 60 MHz.

The next factor affecting FPGA boot time is the interface type. AMD and Altera FPGAs support the QSPI flash interface (4-bit) and Single Data Rate (SDR). In comparison, the Certus-N2 supports the DDR xSPI flash interface (8-bit), which is four times the bandwidth as the QSPI interface when using the same clock rate.

Lastly the Lattice Certus-N2 device stands out due to the Nexus 2 platform's 4-input LUT architecture, which is known for its optimized area utilization. In contrast, AMD employs a 6-input LUT, and Altera uses the ALM, an 8-input LUT that can be configured as either a LUT4 or LUT6. These larger building blocks necessitate more configuration data. The combination of a smaller bitstream and a faster configuration interface gives the Lattice Certus-N2 a significant performance edge in boot time.

The factors affecting boot time are summarized below. The estimated comparison factor resembles actual measurement.

	Lattice Certus-N2 CT20		AMD Artix US+ AU20P		Altera Cyclone 10GX 220	
Flash Clock Frequency*	160 MHz	1X	127.5 MHz	1.26X	60 MHz	2.67X
Configuration I/F Width**	X8 DDR	1X	X4 SDR	4X	X4 SDR	4X
Configuration Bitstream Size (Mb)	44	1X	123	2.8X	92	2.1X
Est. Comparison Factor	1X		14X		22X	
Actual Comparison Factor	1X		14.5X		20X	

* Flash Clock Frequency generated from internal oscillator

** Single external SPI memory

3.3. COMPARING POWER CONSUMPTION

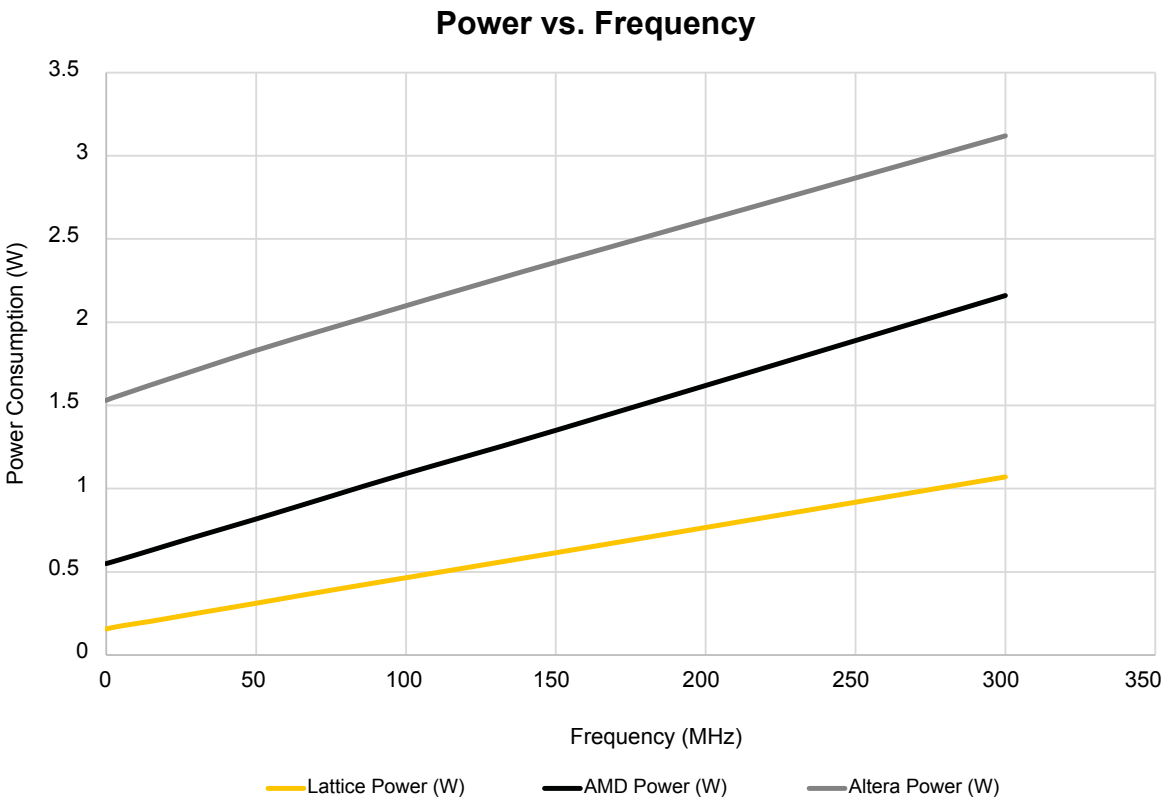
Power consumption is a critical factor in all applications. Minimizing power usage not only enhances system efficiency but also brings several benefits. Lower power consumption leads to longer battery life, simplified thermal management, and improved device longevity and reliability. These advantages collectively contribute to a lower total cost of ownership, making low-power designs highly desirable.

3.3.1. MEASURED POWER CONSUMPTION RESULTS

Here's the methodology for measuring power consumption:

1. The same RTL design is applied to all three FPGAs.
2. The RTL design occupy similar resources in all three FPGAs, taking approximately 107k SLC (61k LUTs and 122k registers.
3. Power is measured with the design at fabric frequencies ranging from 0 MHz to 300 MHz.

Results are plotted below



Our comparison indicates that the Lattice Certus-N2 exhibits lower static and dynamic power across the full range of operating frequencies.

3.3.2. FACTORS AFFECTING POWER CONSUMPTION IN FPGAS

Architectural decision in FPGA platforms is a large contributor to differences in power consumption. The power consumption of LUT4 (4-input Look-Up Table) versus LUT6 (6-input Look-Up Table) in FPGAs can vary based on several factors:

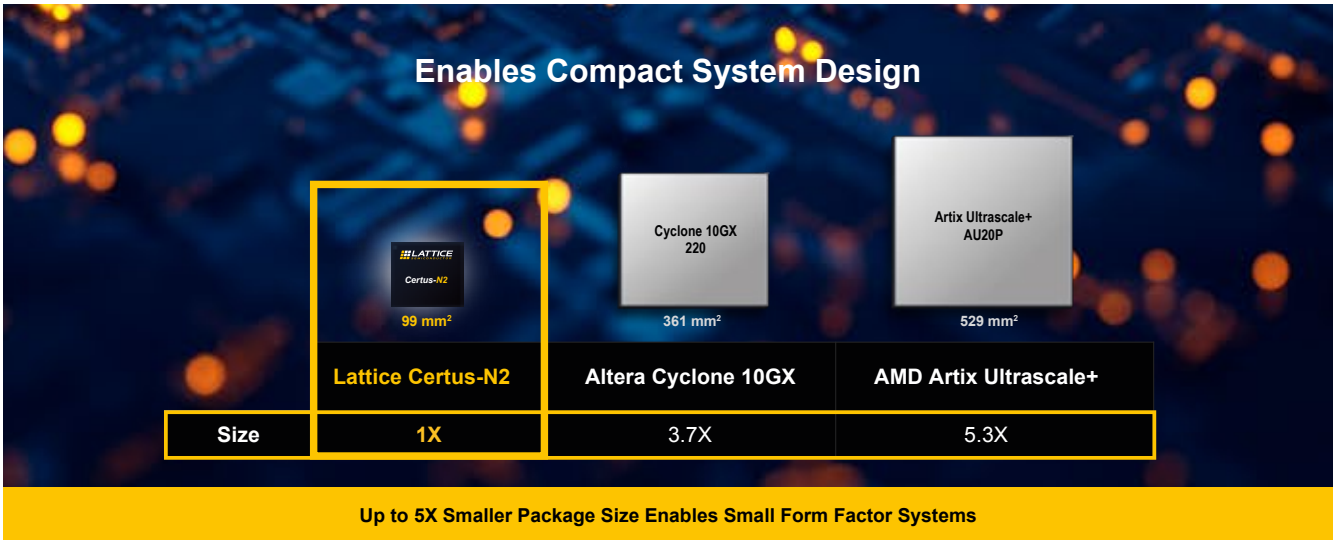
1. **Static Power:** LUT4s generally consume less static power compared to LUT6s because they have fewer configuration bits and smaller area.
2. **Dynamic Power:** LUT6s can potentially reduce dynamic power consumption by minimizing the number of logic levels required to implement a function.
3. **Area Efficiency:** LUT4s are more area-efficient, which can lead to lower static power consumption due to reduced leakage.
4. **Performance/Design choice:** LUT6s typically offer better performance due to their ability to implement more complex functions with fewer logic levels.

In summary, while LUT4s are generally better for static power and area efficiency, LUT6s can offer advantages in performance. In most small FPGA applications, LUT4s provide sufficient performance.

3.4. COMPARING FORM FACTOR

When comparing device sizes, we aim for the smallest form factor that still provides essential features. The Lattice Certus-N2 CT20 is available in an 11 x 9 mm² package with high-speed SERDES. In contrast, similar features are found in the 19 x 19 mm² Altera Cyclone 10GX 220 and the 23 x 23 mm² AMD Artix Ultrascale+ AU20P. This makes the Lattice Certus-N2 CT20 FPGA five times smaller than the smallest AU20P package.

A smaller form factor not only saves PCB area but also simplifies component placement within a system. Additionally, a smaller device typically indicates lower power consumption and cost-effectiveness, making it a suitable choice for various applications.



3.5. COMPARING TOTAL COST OF OWNERSHIP

The total cost of ownership (TCO) of circuit boards includes all expenses associated with designing, manufacturing, operating, and maintaining the boards throughout their lifecycle. We can start by comparing the Bill of Materials (BOM) when designing with these FPGAs.

	Lattice Certus-N2 CT20	AMD Artix US+ AU20P	Altera Cyclone 10GX 220
Minimum Configuration Flash Size	64 Mb	128 Mb	128 Mb
Thermal Management	None	Passive Cooling	Passive Cooling
Power Delivery*	Simple	Complex	Complex

*Considering requirements for power supply sequencing and active power management

Due to their larger configuration bitstreams, the configuration flash required for the AU20P and 10GX220 is at least twice the size of that used by the Lattice Certus-N2, resulting in higher costs. The Lattice Certus-N2's lower power consumption and compact form factor reduce the need for a heat sink or additional PCB size considerations. Additionally, it features a much simpler power delivery design compared to the AU20P and 10GX220, leading to a lower BOM and development cost when designing with Lattice Certus-N2.

When considering the total cost of ownership (TCO), lifecycle maintenance of the systems is crucial. Therefore, the security and reliability of the devices used become critical factors. A system designed with more secure and reliable FPGAs reduces the chance of successful hacking. Lattice Nexus 2 devices support post-quantum safe AES-GCM and SHA-3 algorithms, and industry-proven ECDSA-521 and RSA4K authentication. Even in the event of a disruption, a more reliable FPGA can recover faster and minimize the impact from hackers. The Lattice Certus-N2 recovers quickly with instant-on configuration and keeps the system running without noticeable interruption. The Lattice Nexus 2 devices compare favorably against the competition as shown in the table below.

	Lattice Nexus 2	AMD Artix US+ AU20P	Altera Cyclone 10GX 220
Bitstream Encryption	AES-GCM	AES-GCM	AES
Bitstream Authentication	ECDSA-521, RSA4K, SHA-3/512	RSA2K, SHA-3/384	No
User Cryptography	Supported	Not Supported	Not Supported

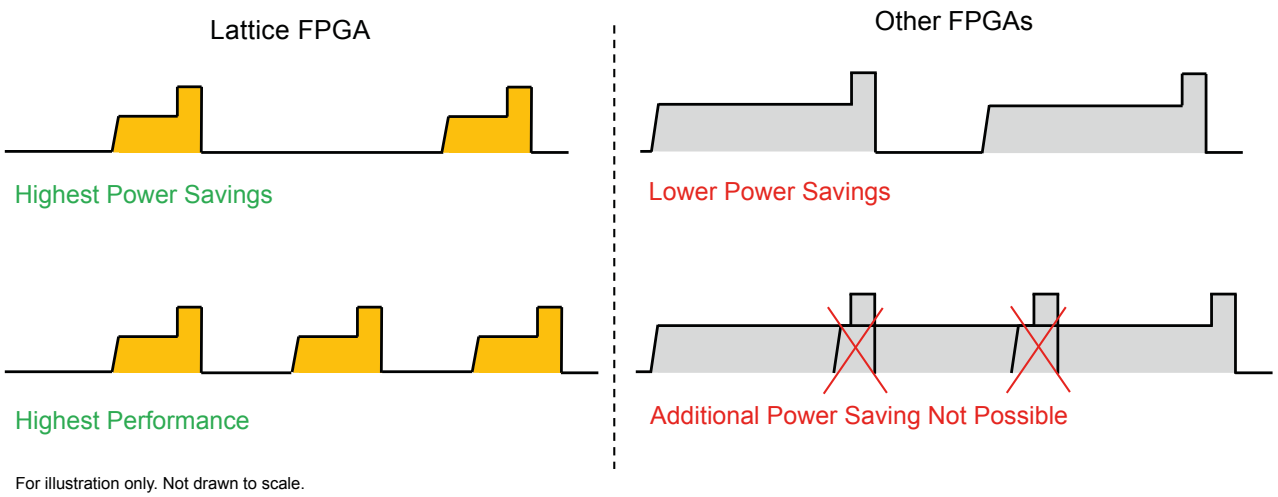
3.6. LATTICE NEXUS 2 APPLICATIONS

In this section, we outline the applications enabled by the key features from the Lattice Nexus 2 Platform.

- **Motor Control Robotics:** Growing presence of automated robotics in the industrial workspace require more protection for workers who interface with machines regularly. Enhanced security and fast fault recovery features ensure safe and reliable operation in industrial settings.
- **Automotive Zonal Gateway:** A key component in modern vehicle electrical and electronic architectures, designed to manage the electronic systems within a vehicle by their physical location. One of the benefits of a zonal gateway is improved efficiency and reduced latency for sensors, actuators, and other devices in the same zone. Using Lattice Nexus 2 devices with instant-on configuration shortens wake time, ensuring timely responses to external triggers.
- **Edge monitoring:** Some applications may require only periodic processing by the FPGA such as human or object presence detection. Traditionally, the FPGA may stay in an idle state if it is not continuously processing edge data. For battery operated systems or applications in thermally challenged outdoor environments, Lattice Nexus 2 FPGAs can power off during idle periods and use instant-on configuration to catch the next processing interval. Enabling power duty-cycle further reduces the average power consumption, lowers thermal stress, and improves the reliability of the system.

Lattice compared the power duty-cycle use case against the competition. The Lattice Certus-N2 average power consumption can be up to 8 times lower than the competition when using power duty-cycling. The AU20P and Cyclone 10GX 220 have long boot-up times in the order of 200–300 ms. To gain any power savings from duty cycling, they can only operate at 1 to 3 Hz intervals before they must stay “on” full-time. See below for an illustration of this concept.

Lattice FPGA Edge Monitoring Advantage



For illustration only. Not drawn to scale.

Comparing the total power (area under the curve), it is evident that Lattice Nexus 2 devices can power duty-cycle while maintaining a high level of performance in edge monitoring applications.

4. Conclusion

The Lattice Nexus 2 platform represents a significant advancement in small FPGA technology, offering unparalleled power efficiency, performance, and security in a compact form factor. With these enhancements, developers can accelerate product development and meet the evolving demands of edge applications. Future Nexus 2 families will introduce additional features, including integrated flash memory, enhanced security, faster D-PHY and hardened C-PHY capabilities, further solidifying Lattice’s position as a leader in low power small FPGAs.

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