



# **System Memory Module**

IP Version: v2.5.0

## **Release Notes**

FPGA-RN-02065-1.3

December 2025

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# 1. Introduction

This document contains the Release Notes for the System Memory Module. For specific details about the IP, refer to the following:

- [System Memory Module User Guide \(FPGA-IPUG-02073\)](#)

## System Memory Module v2.5.0

Software	Software Version	Summary of Changes
Lattice Propel	2025.2	<ul style="list-style-type: none"> <li>• Added the AXI4 atomic access feature.</li> <li>• Added support for MachXO4 devices.</li> </ul>

## System Memory Module v2.4.0

Software	Software Version	Summary of Changes
Lattice Propel	2025.1	<ul style="list-style-type: none"> <li>• Added AXI interface support for ECP5 devices.</li> <li>• Added support for 64-bit data width on the AXI interface.</li> </ul>

## System Memory Module v2.3.1

Software	Software Version	Summary of Changes
Lattice Propel	2024.2.1	Fixed the Memory Address Depth parameter in the graphical user-interface (GUI).

## System Memory Module Earlier Versions

IP Version	Summary of Changes
2.3.1	<ul style="list-style-type: none"> <li>• Fixed memory address depth parameter in graphical user-Interface.</li> </ul>
2.3.0	<ul style="list-style-type: none"> <li>• Added LN2-CT support.</li> <li>• Enhancements with AXI4 performance.</li> <li>• Disabled output register for AXI4.</li> </ul>
2.2.0	<ul style="list-style-type: none"> <li>• Added ECP5 support and other enhancements.</li> </ul>
2.1.0	<ul style="list-style-type: none"> <li>• Support Read Pipeline for timing enhancement.</li> </ul>
2.0.0	<ul style="list-style-type: none"> <li>• Added AXI4 Interface support.</li> </ul>
1.1.2	<ul style="list-style-type: none"> <li>• Support for LAV-AT devices.</li> </ul>
1.1.1	<ul style="list-style-type: none"> <li>• Support for 208 EBRs in CertusPro-NX devices.</li> </ul>
1.1.0	<ul style="list-style-type: none"> <li>• Added support for up to 7 LRAMs in CertusPro-NX devices.</li> </ul>
1.0.4	<ul style="list-style-type: none"> <li>• Support for MachXO2, MachXO3L and improved timing for LRAM implementations.</li> </ul>
1.0.3	<ul style="list-style-type: none"> <li>• Support for Mach-NX.</li> </ul>
1.0.2	<ul style="list-style-type: none"> <li>• Support for CertusPro-NX.</li> </ul>
1.0.1	<ul style="list-style-type: none"> <li>• Support for Crosslink-NX, Certus-NX.</li> </ul>
1.0.0	<ul style="list-style-type: none"> <li>• Initial release.</li> </ul>

## References

- [System Memory Module User Guide \(FPGA-IPUG-02073\)](#)
- [iCE40 UltraPlus](#) web page
- [ECP5 / ECP5-5G](#) web page
- [CrossLink-NX](#) web page
- [Certus-NX](#) web page
- [Certus-N2](#) web page
- [CertusPro-NX](#) web page
- [Mach-NX](#) web page
- [MachXO2](#) web page
- [MachXO3](#) web page
- [MachXO3D](#) web page
- [MachXO4](#) web page
- [MachXO5-NX](#) web page
- [Avant-E](#) web page
- [Avant-G](#) web page
- [Avant-X](#) web page
- [System Memory Module IP Core](#) web page
- [Lattice Radiant Software](#) web page
- [Lattice Propel Design Environment](#) web page
- [Lattice Diamond Software](#) web page
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans

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