

System Memory Module IP

IP Version: v2.4.0

Release Notes

FPGA-RN-02065-1.2

June 2025



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1. Introduction

This document contains the Release Notes for the System Memory IP. For specific details about the IP, refer to the following:

• System Memory Module (FPGA-IPUG-02073)

System Memory Mdoule IP v2.4.0

Software	Software Version	Summary of Changes
Lattice Propel	2025.1	Added AXI interface support for ECP5 devices.
		Added support for 64-bit data width on the AXI interface.

System Memory Module IP v2.3.1

Software	Software Version	Summary of Changes
Lattice Propel	2024.2.1	Fixed the Memory Address Depth parameter in the graphical user-interface (GUI).

System Memory Module IP Earlier Versions

IP Version	Summary of Changes			
2.3.1	Fixed memory address depth parameter in graphical user-Interface.			
	Added LN2-CT support.			
2.3.0	Enhancements with AXI4 performance.			
	Disabled output register for AXI4.			
2.2.0	Added ECP5 support and other enhancements.			
2.1.0	Support Read Pipeline for timing enhancement.			
2.0.0	Added AXI4 Interface support.			
1.1.2	Support for LAV-AT devices.			
1.1.1	Support for 208 EBRs in CertusPro-NX devices.			
1.1.0	Added support for up 7 LRAMs in CertusPro-NX devices.			
1.0.4	Support for MachXO2, MachXO3L and improved timing for LRAM implementations.			
1.0.3	Support for Mach-NX.			
1.0.2	Support for CertusPro-NX.			
1.0.1	Support for Crosslink-NX, Certus-NX.			
1.0.0	Initial release.			



References

- System Memory Module (FPGA-IPUG-02073)
- MachXO2 web page
- MachXO3 web page
- MachXO3D web page
- Mach-NX web page
- Lattice Nexus Platform web page
- Lattice Avant Platform web page
- Certus-N2 web page
- IP Core for Lattice Nexus devices
- IP Core for MachXO2
- IP Core for MachXO3
- IP Core for MachXO3D
- IP Core for Mach-NX
- IP Core for Lattice Avant devices
- Lattice Propel Builder software
- Lattice Insights for Lattice Semiconductor training courses and learning plans



Technical Support Assistance

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