



Pixel-to-Byte Converter IP

IP Version: v1.9.2

Release Notes

FPGA-RN-02020-1.2

December 2025

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1. Introduction

This document contains the Release Notes for the Pixel-to-Byte Converter IP. For specific details about the IP, refer to the following:

- [Pixel-to-Byte Converter IP User Guide \(FPGA-IPUG-02094\)](#)

Pixel-to-Byte Converter IP v1.9.2

Software	Software Version	Summary of Changes
Lattice Radiant	2025.2	<ul style="list-style-type: none"> • Updated plugin script for unsupported configuration. • Applied minor fix for LSE synthesis error. • Removed the IP licensing requirement.

Pixel-to-Byte Converter IP v1.9.1

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1	<ul style="list-style-type: none"> • Added support for LFD2NX-15, LFD2NX-25, LFD2NX-35, and LFD2NX-65 devices. • Added support for LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T devices.

Pixel-to-Byte Converter IP v1.9.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	<ul style="list-style-type: none"> • Added Word Count configurability when Manual Adjust is enabled. • Added support for LFD2NX-9 and LFD2NX-28 devices.

Pixel-to-Byte Converter IP Earlier Versions

IP Version	Summary of Changes
1.8.0	Added support for Certus-N2 devices.
1.7.0	<ul style="list-style-type: none"> • Added support for the Radiant software 2024.1. • Added support for APB. • Added support for AXI4-stream transmitter and receiver interfaces. • Added FIFO configurability to the GUI. • Added optional enabling/disabling line start/end short packets for CSI-2.
1.6.0	<ul style="list-style-type: none"> • Added support for the Radiant software 2023.2. • Added support for the Avant devices
1.4.0	<ul style="list-style-type: none"> • Added support for MachXO5-NX devices. • Added new configurations for 4 pixels per clock input. • Added LIFCL-33 and LFMXO5-25 devices to the list of supported devices.
1.3.0	<ul style="list-style-type: none"> • Added new configurations for 1 and 2 pixels per clock input. • Recoded core modules for different data types.
1.2.0	<ul style="list-style-type: none"> • Added non-burst sync pulses support for DSI data types. • Added RAW14 and RAW16 CSI-2 data types. • Added support for CertusPro-NX devices.
1.1.0	<ul style="list-style-type: none"> • Changed the output width and byte ordering to ordinal sequence. • Added support for Certus-NX devices.
1.0.1	Production release.

IP Version	Summary of Changes
1.0.0	Initial release.

References

- [Pixel-to-Byte Converter IP User Guide \(FPGA-IPUG-02094\)](#)
- [Avant-E](#) web page
- [Avant-G](#) web page
- [Avant-X](#) web page
- [Certus-N2](#) web page
- [Certus-NX](#) web page
- [CertusPro-NX](#) web page
- [CrossLink-NX](#) web page
- [MachXO5-NX](#) web page
- [Pixel-to-Byte Converter IP Core](#) web page
- [Lattice Propel Design Environment](#) web page
- [Lattice Radiant Software](#) web page
- [Lattice Solutions IP Cores](#) web page
- [Lattice Solutions Reference Designs](#) web page
- [Lattice Insights](#) web page for Lattice Semiconductor training courses and learning plans

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Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.



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