

MDIO Leader IP

IP Version: v1.2.0

Release Notes

FPGA-RN-02029-1.1

July 2025



Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.



Contents

ontents	
Introduction	2
MDIO Leader IP v1.2.0	
MDIO Leader IP v1.1.1	
MDIO Leader IP Earlier Versions	
eferences	
echnical Sunnort Assistance	



1. Introduction

This document contains the Release Notes for the MDIO Leader IP. For specific details about the IP, refer to the following:

• MDIO Leader IP User Guide (FPGA-IPUG-02223)

MDIO Leader IP v1.2.0

Software	Software Version	Summary of Changes
Lattice Radiant™	2025.1	 Added LFD2NX-35, LFD2NX-65, LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T device support.
		Minor GUI enhancements.

MDIO Leader IP v1.1.1

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	Added LN2-CT-20 device support.

MDIO Leader IP Earlier Versions

IP Version	Summary of Changes		
1.1.0	 Lattice Nexus™ 2 device support. IP is provided at no additional cost with the Lattice Radiant software. 		
1.0.0	Initial release.		



References

- MDIO Leader IP User Guide (FPGA-IPUG-02223)
- Avant™-E web page
- Avant-G web page
- Avant-X web page
- CertusPro™-NX web page
- Certus™-N2 web page
- MachXO5™-NX web page
- MDIO Leader IP Core web page
- Lattice Solutions IP Cores web page
- Lattice Solutions Reference Designs web page
- Lattice Solutions Boards web page
- Lattice Solutions Demonstrations web page
- Lattice Propel™ Builder software web page
- Lattice Radiant FPGA design software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans



Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport. For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase



www.latticesemi.com