CSI-2/DSI D-PHY Tx IP

IP Version: v2.4.0

Release Notes

FPGA-RN-02041-1.2

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Contents

1. Introduction

This document contains the Release Notes for the CSI-2/DSI D-PHY Tx IP. For specific details about the IP, refer to the following:

- CSI-2/DSI D-PHY Tx IP User Guide (FPGA-IPUG-02080)

CSI-2/DSI D-PHY Tx IP v2.4.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.2	• Enabled dynamic reconfiguration for additional configurations. For details, refer to the user guide. • Updated *Target TX Line Rate (Mbps per Lane)* minimum value for Gear 16 configurations. For details, refer to the user guide. • Added new attribute *Show TX Timing Parameter Actual RTL Value* in GUI. For details, refer to the user guide. • Enhanced timing parameter and actual RTL value calculation. • Enhanced IP package testbench checker with sample LMMI access. • Enhanced example design to include additional checks and support for dynamic lane reconfiguration. • Other general IP enhancements and general bug fixes. • Removed IP license requirement.

CSI-2/DSI D-PHY Tx IP v2.3.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1	• Added support for LFD2NX-15, LFD2NX-25, LFD2NX-35, and LFD2NX-65 devices. • Added support for LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T devices. • Enabled dynamic reconfiguration for specific configurations. For details, refer to the user guide. • Added new attribute *Enable Manual Control of D-PHY Clock* in GUI to support D-PHY clock lane control in specific configurations. For details, refer to the user guide. • Other minor IP enhancements and general bug fixes.

CSI-2/DSI D-PHY Tx IP v2.2.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	• Added internal reset synchronizer to byte_clk_o clock domain. • Removed the requirement to have output byte clock (byte_clk_o) active when accessing CSR. • Updated maximum data rate to be consistent with the Lattice device datasheet. • Added an example design. • Added support for Certus-N2 devices. • Added support for LFD2NX-9 and LFD2NX-28 devices. • Other minor IP enhancements.

CSI-2/DSI D-PHY Tx IP Earlier Versions

IP Version	Summary of Changes
2.1.0	Added support for Certus-N2 devices (for early access).

IP Version	Summary of Changes
2.0.0	• Fixed functional bugs found in the last release. • Added option to enable or disable the Edge Clock Synchronizer and Divider blocks. • Enhanced constraint generation and implementation using the new IP constraint propagation method by the software. • Fixed issues with testbench. • Fixed issues related to internal LMMI signal initializations and access. • Corrected default setting of some of hard DPHY parameters. • Updated port list and names. • Other minor GUI fixes.
1.9.2	Fixed minor bug in GUI.
1.9.1	Added timing constraint *.pdc* automation.
1.9.0	• Fixed the data lane going to hs-0 before going to LP-11 during HS-TRAIL state. • Fixed reduced LP00 and LP01 duration when t_LPX and t_HS_PREPARE are set to 2. • Removed Hard D-PHY option in LIFCL-33U devices. • Added support for the Lattice Propel software.
1.8.1	• Revised timing protocol parameter values. New GUI values reflect the behavior in simulation. • Added a new clock port pll_clkos_i for Nexus Soft D-PHY for a more stable 90-degree phase between clock and data lane. • Added support for extended virtual ID. Testbench is not updated for this feature in this version.
1.8.0	Added support for Avant devices.
1.7.2	Added checking of device, package, and speed grade to determine the maximum line rate.
1.7.1	Updated the testbench to match the IPUG and RTL AXI-4 stream mapping of word count and virtual channel ID.
1.7.0	• Added support for LFMXO5 devices. • Cleaned up data width warnings. • Updated timing constraints.
1.6.0	• Reverted synchronization of reset_n_i to the byteclock domain (added in IP v1.5). • Fixed VCS compilation error. • Fixed AXI-4 mapping of packet fields.
1.5.0	• Fixed 1.2 V offset on the clock N-channel when using the Soft PHY implementation. • Synchronized reset_n_i in the byteclock domain.
1.4.0	Fixed Skew Calibration timing-related entries in GUI.
1.3.0	• Fixed counter bit width reset issue in TX Global Controller. • Fixed Skew Calibration timing entries in GUI. • Fixed LP RX issue in Soft D-PHY configuration. • Fixed rounding error of reference clock in testbench.
1.2.0	Added support for CertusPro-NX devices.
1.1.5	Fixed combinational loop in the skew calibration signals.
1.1.4	• Code enhancements to fix timing issues at data rates above 2,000 Mbps. • Captured the updated GPLL Module v1.2.2 with the DIV_DEL parameter.
1.1.3	• DPHY packet enable bug fix. • Fixed c2d_ready_o behaviour, where the assertion of this signal waits for tinit_done_o. • Fixed the initial deskew calibration timing.
1.1.2	• Added initial deskew calibration for data rates above 1.5 Gbps. • Added support for optional periodic skew calibration. • Changed the implementation of the DSI FIFO within the Packet Formatter module to EBR. • Added the actual data rate and the deviation from the target data rate in the configuration window.
1.1.1	Updated testbench for the Lattice Radiant software version 2.2 compatibility.
1.1.0	• Added support for ordinal data sequence. Previous versions of the IP require input data to be lane interleaved.

IP Version	Summary of Changes
	• Added testbench support for 3-lane configuration when packet formatter is disabled. • Added support for CIL-enabled configuration. • Code enhancements to remove output glitches. • Provided external clock option for Hard D-PHY. • Added option for Soft PHY implementation. • Added support for Certus-NX devices.
1.0.1	Updated for SP1 release.
1.0.0	Initial release.

References

- CSI-2/DSI D-PHY Tx IP User Guide (FPGA-IPUG-02080)
- Certus-NX web page
- Certus-N2 web page
- CertusPro-NX web page
- CrossLink-NX web page
- MachXO5-NX web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- CSI-2/DSI D-PHY Transmitter IP Core web page
- Lattice Propel Builder software
- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

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