CSI-2/DSI D-PHY Rx IP

IP Version: v2.1.0

Release Notes

FPGA-RN-02040-1.2

December 2025

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

1. Introduction

This document contains the Release Notes for the CSI-2/DSI D-PHY Rx IP. For specific details about the IP, refer to the following:

- CSI-2/DSI D-PHY Rx IP User Guide (FPGA-IPUG-02081)

CSI-2/DSI D-PHY Rx IP v2.1.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.2	• Enabled dynamic reconfiguration for additional configurations. For details, refer to the user guide. • Improved internal ECLK and SCLK synchronization in Nexus devices for enhanced robustness. • Enhanced IP package testbench checker with sample LMMI access and CRC/ECC flag checking. • Enhanced example design to include additional checks and support for dynamic lane reconfiguration. • Other general IP improvements and bug fixes. • Removed IP license requirement.

CSI-2/DSI D-PHY Rx IP v2.0.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1	• Added support for LFD2NX-15, LFD2NX-25, LFD2NX-35, and LFD2NX-65 devices. • Added support for LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T devices. • Implemented CRC checking support for additional configurations. For details, refer to the user guide. • Enabled dynamic reconfiguration for additional configurations. For details, refer to the user guide. • Replaced the *Enable Lane/Gear Dynamic Reconfiguration* attribute in GUI with the *CRC Check Mode* attribute. • Added support for data rates up to 1.8 Gbps for Lattice Avant devices. • Added support for Deskew Calibration Detection for soft D-PHY. • Other minor IP enhancements and general bug fixes.

CSI-2/DSI D-PHY Rx IP v1.9.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	• Removed the requirement to have free running byte clock (clk_byte_fr_i) active when accessing CSR. • Updated maximum data rate to be consistent with the Lattice device datasheet. • Enabled IMONDELAY logic for data rate 1,000 Mbps and above for Lattice Avant devices. • Added an example design. • Added support for Certus-N2 devices. • Added support for LFD2NX-9 and LFD2NX-28 devices. • Other minor IP enhancements and general bug fixes.

CSI-2/DSI D-PHY Rx IP Earlier Versions

IP Version	Summary of Changes
1.8.0	Added support for Certus-N2 devices (for early access).
1.7.0	• Fixed functional bugs found in the last release. • Fixed issues with testbench. • Fixed issues related to internal LMMI signal initializations. • Corrected default setting of some hard DPHY parameters. • Enhanced constraint generation and implementation using the new IP constraint propagation method by the software. • Added support for the Lattice Propel software. • Updated port list and names. • Other minor GUI fixes.
1.6.1	• Fixed an issue related to setting small word count. • Fixed issues in testbench. • Other IP GUI fixes and enhancements.
1.6.0	• Added Soft D-PHY delay cell settings in the GUI. • Added support for CSI-2 Extended Virtual Channel ID. • Added header ECC error check and correction. • Added support for dynamic late rate reconfiguration (Hard D-PHY CIL-Enabled). • Added support for LFMXO5-55T, LFMXO5-100T, and LAV-AT devices.
1.5.0	Added support for LAV-AT-E devices.
1.4.3	• Removed partial encryption of the dphy_rx_wrap module; no RTL source code change. • Added checking of speed grade to determine the maximum supported data rate.
1.4.2	• Added clarity in the partially encrypted RTL to resolve syntax error getting flagged when the Reveal Analyzer is disabled in IP v1.4.1; no RTL source code change. • Added checking of package type to determine the maximum supported data rate.
1.4.1	Unencrypted the hard D-PHY primitive instantiation to support the Reveal Analyzer insertion.

1.4.0	• Fixed clock constraints in the .ldc file.
	• Fixed the following VCS compilation errors:
	  • Error-[IRIBS] Illegal range in bit-select
	  • Error-[MEAFFS] No argument for format specification
	• Added support for LFMXO5-25 devices.

1.3.0	Fixed issue found in non-continuous clock mode (HS to LP transition detection).
1.2.0	Added support for CertusPro-NX devices.
1.1.2	Updated INIT value of CLK_DESKEW_DLYCAL when data rate is less than or equal to 1.5 Gbps.
1.1.1	• Added deskew calibration support. • Adjusted Soft D-PHY HS-SETTLE parameter count. • Hid RX_FIFO parameters in the GUI when CIL is enabled.
1.1.0	• Added support for RX lane = 3 in the Verilog testbench. • Fixed hs-settle timing for Soft D-PHY. • Fixed ports when LMMI is enabled. • Added support for Certus-NX devices.
1.0.1	Production release.
1.0.0	Initial release.

References

- CSI-2/DSI D-PHY Rx IP User Guide (FPGA-IPUG-02081)
- Certus-NX web page
- Certus-N2 web page
- CertusPro-NX web page
- CrossLink-NX web page
- MachXO5-NX web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- CSI-2/DSI D-PHY Receiver IP Core web page
- Lattice Propel Builder software
- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

www.latticesemi.com