

Byte-to-Pixel Converter IP

IP Version: v1.9.1

Release Notes

FPGA-RN-02019-1.1

June 2025



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Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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1. Introduction

This document contains the Release Notes for the Byte-to-Pixel Converter IP. For specific details about the IP, refer to the following:

• Byte-to-Pixel Converter IP User Guide (FPGA-IPUG-02079)

Byte-to-Pixel Converter IP v1.9.1

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1	 Added support for LFD2NX-15, LFD2NX-25, LFD2NX-35, and LFD2NX-65 devices. Added support for LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T devices.
		 Removed axis_vid_aresetn_i and axis_vid_aclk_i ports when Unified Video Streaming Tx Interface is enabled. Updated the constraint file and fixed bugs.

Byte-to-Pixel Converter IP v1.9.0

Software	Software Version	Summary of Changes
	2024.2	Added support for Certus-N2 devices.
		Added support for the AXI4-Lite interface protocol.
		Added support for the AXI4-Stream protocol through Unified Video Streaming Tx interface.
Lattice Radiant		 Added the RGB remapping support to pd_red_o, pd_green_o, and pd_blue_o ports for DSI and CSI-2 RGB data types.
		Added the Enable Byte Swap per Pixel attribute in the GUI.
		Fixed the pd_o pixel output for RAW14 and YCbCr data types for MIPI
		compliance.

Byte-to-Pixel Converter IP Earlier Versions

IP Version	Summary of Changes		
1.8.0	Added support for Certus-N2 devices (for early access).		
	Made quality enhancement.		
1.7.0	Made other bug fixes.		
	Made minor GUI enhancements.		
	Fixed timing issue encountered in DSI configurations.		
	Fixed output issue encountered when AXI4-Stream Transmitter Interface is enabled.		
1.6.1	Updated constraint file.		
1.0.1	Added support for 4 output pixel lanes for RAW12 data type.		
	Made other bug fixes.		
	Made minor GUI enhancements.		
	Added support for Lattice Avant devices.		
1.6.0	Separated RTL per data type under CSI-2 configurations.		
	Updated constraint file.		
1.5.0	Added support for MachXO5-NX devices.		
1.4.0	Added DSI Sync Packet Delay attribute.		
1.4.0	Fixed unintended early read from the FIFO even when the GUI threshold is manually adjusted.		
1.3.0	Fixed lp_av_en issue encountered in DSI configurations.		
1.5.0	Fixed synthesis issue encountered in Synplify Pro.		

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IP Version	Summary of Changes		
	Updated constraint file.		
1.2.0	Added support for CertusPro-NX devices.		
1.1.1	 Added support for RAW12, RAW14 and RAW16 data types. Fixed wire declaration of ports (multicycle nets). 		
1.1.0	 Updated RTL to optimize FIFO instance. Added Rx and Tx data rates (read-only). Updated IP to work correctly for YUV420_8 and YUV420_10 data types. Removed Odd/Even attribute from YUV data types. Fixed threshold calculation issue for small word counts. 		
1.0.3	Added support for Certus-NX devices.		
1.0.2	Updated for Radiant 2.0 Service Pack 1.		
1.0.1	Production release.		
1.0.0	Initial release.		



References

- Byte-to-Pixel Converter IP User Guide (FPGA-IPUG-02079)
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Certus-N2 web page
- Certus-NX web page
- CertusPro-NX web page
- CrossLink-NX web page
- MachXO5-NX web page
- Byte-to-Pixel Converter IP Core web page
- Lattice Propel Design Environment web page
- Lattice Radiant Software web page
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

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