

# **AXI4 Interconnect Module**

IP Version: v2.2.0

# **Release Notes**

FPGA-RN-02045-1.1

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# **Contents**

| Contents                                  |  |
|---|--|
| 1. Introduction                           |  |
| AXI4 Interconnect Module v2.2.0           |  |
| AXI4 Interconnect Module v2.1.0           |  |
| AXI4 Interconnect Module Earlier Versions |  |
| References                                |  |
| Technical Sunnort Assistance              |  |



## 1. Introduction

This document contains the Release Notes for the AXI4 Interconnect Module. For specific details about the IP, refer to the following:

AXI4 Interconnect Module User Guide (FPGA-IPUG-02196)

### **AXI4 Interconnect Module v2.2.0**

| Software       | Software Version  | Summary of Changes  |
|----------------|---|---|
|                |   | Removed the Full Address Decoding up to 4 kB attribute.                     |
|                |   | Added the Memory Type of Large FIFOs attribute.                             |
| Builder 2025.1 | 2025 1  | Added support for LFD2NX-15, LFD2NX-25, LFD2NX-35, and LFD2NX-65 devices.   |
|                | 2025.1  | Added support for LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T devices. |
|                | Documented the changes for earlier IP versions in the IP Release Notes. |   |

### **AXI4 Interconnect Module v2.1.0**

| Software                  | Software Version | Summary of Changes  |
|---------------------------|------------------|---|
| Lattice Propel<br>Builder | 2024.2           | Added support for Certus-N2, LatticeECP3, and ECP5 devices. |

### **AXI4 Interconnect Module Earlier Versions**

| IP Version | Summary of Changes   |  |  |  |
|------------|--|--|--|--|
| 2.0.1      | <ul> <li>Fixed an issue where a series of write address transactions that hit the maximum outstanding<br/>transactions may cause missing transactions.</li> </ul>                            |  |  |  |
|            | <ul> <li>Fixed an issue where malfunctions may occur when the configured IP has the following attributes:</li> <li>Data width upsizing</li> </ul>  |  |  |  |
|            | Data width downsizing  |  |  |  |
|            | <ul> <li>AXI Manager Max Data Width does not equal to AXI Subordinate Max Data Width</li> </ul>  |  |  |  |
|            | • Fixed an issue where malfunctions may occur in out-of-order read responses of transactions involving data width upsizing.  |  |  |  |
|            | <ul> <li>Eliminated an incorrect dependency where the WVALID signal on the external subordinate interface<br/>may not assert because of the AWREADY signal on the said interface.</li> </ul> |  |  |  |
|            | Extended support to all Nexus devices.   |  |  |  |
| 2.0.0      | <ul> <li>Revamped the width conversion methodology for better throughput performance, higher operating<br/>frequency, and better resource utilization.</li> </ul>                            |  |  |  |
| 1.2.2      | Removed the clock-gating logic.  |  |  |  |
| 1.2.1      | Increased the maximum of External Subordinate <n> Fragment Cnt from 8 to 16.</n>   |  |  |  |
|            | Updated new default values for the following IP settings:  |  |  |  |
|            | AXI User Width   |  |  |  |
| 1.2.0      | AXI Manager Max no. of ID supports   |  |  |  |
|            | • External Manager No. of IDs <n></n>  |  |  |  |
|            | External Manager Write Accept <n></n>  |  |  |  |
|            | External Manager Read Accept <n></n>   |  |  |  |
|            | External Subordinate Write Issue <n></n>   |  |  |  |
|            | External Subordinate Read Issue <n></n>  |  |  |  |
| 1.1.0      | Added support for Avant devices.   |  |  |  |
| 1.0.0      | Initial release.   |  |  |  |



## References

- AXI4 Interconnect Module User Guide (FPGA-IPUG-02196)
- LatticeECP3 web page
- ECP5 web page
- CrossLink-NX web page
- CertusPro-NX web page
- Certus-NX web page
- Certus-N2 web page
- MachXO5-NX web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- AXI4 Interconnect Module web page
- Lattice Propel Builder software
- Lattice Radiant FPGA design software
- Lattice Diamond Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans



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