AXI Register Slice IP

IP Version: v1.2.0

Release Notes

FPGA-RN-02049-1.1

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1. Introduction

This document contains the Release Notes for the AXI Register Slice IP. For specific details about the IP, refer to the following:

- AXI Register Slice IP User Guide (FPGA-IPUG-02235)

AXI Register Slice IP v1.2.0

Software	Software Version	Summary of Changes
Lattice Propel Builder	2025.1	• Updated the minimum supported values of *Address ID Width* and *User Width*. • Added support for LFD2NX-15, LFD2NX-25, LFD2NX-35, and LFD2NX-65 devices. • Added support for LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T devices. • Documented the changes for earlier IP versions in the IP Release Notes.

AXI Register Slice IP v1.1.0

Software	Software Version	Summary of Changes
Lattice Propel Builder	2024.2	Added support for Certus-N2, LatticeECP3, and ECP5 devices.

AXI Register Slice IP Earlier Versions

IP Version	Summary of Changes
1.0.0	Initial release.

References

- AXI Register Slice IP User Guide (FPGA-IPUG-02235)
- LatticeECP3 web page
- ECP5 web page
- CertusPro-NX web page
- Certus-N2 web page
- Certus-NX web page
- CrossLink-NX web page
- MachXO5-NX web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- AXI Register Slice IP Core web page
- Lattice Propel Builder software
- Lattice Radiant FPGA design software
- Lattice Diamond Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

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For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

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