Tri-Speed Ethernet IP

IP Version: v2.2.0

Release Notes

FPGA-RN-02036-1.3

December 2025

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

1. Introduction

This document contains the Release Notes for the Tri-Speed Ethernet IP. For specific details about the IP, refer to the following:

- Tri-Speed Ethernet IP User Guide (FPGA-IPUG-02084)
- Tri-Speed Ethernet Driver API Reference (FPGA-TN-02341)

Tri-Speed Ethernet IP v2.2.0

Software	Software Version	Summary of Changes
Lattice Radiant™	2025.2	• Added Avant™ G/X30 and Certus™-N2 device support. • Removed MDIO interface. • Parameterized Half Duplex mode and AXIS FIFO mode for LUT-reduced design implementations. • Enhanced timing and LUT optimization.

Tri-Speed Ethernet IP v2.1.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1.1	• Added SGMII (SERDES) and MAC + SGMII (SERDES) support for Avant devices. • Sampled AXIS (tvalid_o and tready_o) signals with clock enable signal for easier integration of 10M/100M support. • Fixed the reference clock selection in the SGMII (SERDES) example design for CertusPro™-NX devices. • Enhanced LUT optimization. • Enabled SDC flow and updated timing constraints for easier integration by replacing set_clock_groups with set_false_paths.

Tri-Speed Ethernet IP v2.0.0

Software	Software Version	Summary of Changes

Lattice Radiant	2025.1	• Renamed IP from *Tri-Speed Ethernet MAC* to *Tri-Speed Ethernet*.
		• Renamed MAC + MPCS to MAC + SGMII (SERDES) option for CertusPro-NX devices.
		• Renamed MAC + SGMII to MAC + SGMII (LVDS) option for all supported devices.
		• Enabled MAC + SGMII (LVDS) for all Nexus-based devices.
		• Enabled RGMII support for all Nexus-based devices.
		• Enhanced RGMII support for all devices with reduced clock sources.
		• Enabled SGMII (SERDES) only mode and example design support for CertusPro-NX devices.
		• Added 10M/100M support for MAC + SGMII (SERDES) and SGMII (SERDES) only options.
		• Added LFD2NX-15/25/35/65 + LFMXO5-35/35T/65/65T device support.
		• Deprecated non-simplified clock source implementation.
		• Added more reference clock source inputs for the MAC + SGMII (SERDES) and SGMII (SERDES) for CertusPro-NX devices.
		• Driver updates:
		  • Added GMII control interface functionality.
		  • Added functions to enable/disable TX and RX MAC separately.
		  • Added functions to enable/disable interrupts.
		  • Added functions to get/clear interrupt status.
		  • Removed the *ethernet_packet_handle* function.

Tri-Speed Ethernet IP Earlier Versions

IP Version	Summary of Changes
1.7.1	• LUT optimization for Avant devices. • Added Nexus™ 2 device support. • Reduced clock sources required for IP adoption. • Added support for standalone SGMII PHY-only option with a new example design. • Added enhancements for improved signal integrity on the SGMII PHY IP for Avant device support. • Enhanced the statistic counter by adding a counter for cumulative number of bytes transmitted or received.
1.6.0	• Added MAC+MPCS mode for CertusPro-NX devices. • Added RMII mode, under mac_only configuration. • Added RGMII hardware example design. • Added low frequency support for system clock. • Added Statistic Counter lite mode. • Removed Classic mode, under mac_only configuration. It is not fully compliant to IEEE specification.
1.5.1	• Added LAV-AT-E30 support. • Reverted AXIS FIFO update for hardware validation bug fix.
1.5.0	• Added Avant-AT-G/X device support. • Added MII/GMII mode, under mac_only configuration. • Added 10M/100M support for RGMII mode. • Updated AXIS FIFO.
1.4.2	Updated driver files.
1.4.1	Updated for Propel™ software support.
1.4.0	Added Stat Counters.
1.3.0	• Added Avant device support. • Added MAC+PHY mode for Avant devices. • Added AXI4L host interface. • Updated CSR memory width from 8 bits to 32 bits.
1.2.0	Added LFMXO5 device support.
1.1.0	• Added LFCPNX device support. • Added RGMII interface.
1.0.1	• Added LFD2NX device support. • Added AXI4-stream interface.
1.0.0	Initial release.

References

- Tri-Speed Ethernet IP User Guide (FPGA-IPUG-02084)
- Tri-Speed Ethernet Driver API Reference (FPGA-TN-02341)
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Certus-NX web page
- CertusPro-NX web page
- CrossLink-NX web page
- MachXO5-NX web page
- Lattice Solutions IP Cores web page
- Lattice Solutions Reference Designs web page
- Lattice Solutions Boards web page
- Lattice Solutions Demonstrations web page
- Lattice Propel Builder software web page
- Lattice Radiant Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase

www.latticesemi.com