Lattice Nexus 2 Power User Guide

Preliminary Technical Note

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This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Figures

Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AF%	Activity Factor Percentage
ADC	Analog Digital Converter
AP	Application Processor
DPM	Dynamic Power Multiplier
EBR	Embedded Block RAM
FDSOI	Fully Depleted Silicon on Insulator
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input/Output
HDL	Hardware Description Language
HP	High Performance
I/O	Input Output
JEDEC	Joint Electron Device Engineering Council
LFM	Linear Feet per Minute
LMMI	Lattice Memory Mapped Interface
LP	Low Power
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor Interface
LRAM	Large RAM
LUT	Look-Up Table
LVDS	Low Voltage Differential Signaling
OSC	Oscillator
PAR	Place and Route
PCB	Printed Circuit Board
PFU	Programmable Functional Unit
PLL	Phase Locked Loop
T_J, T_A, T_B, T_C	Junction, Ambient, Board and Case Temperatures
TR	Toggle Rate
TWR	Trace Report
UDB	Unified Design Database
USR	User Interface
VCD	Value Change Dump
VCO	Voltage Controlled Oscillator

1. Introduction

Lattice Nexus™ 2 FPGA devices are architected and designed for low power consumption. Power supply levels, process technology, device configuration, circuit topologies, and integration methods have all been chosen with the goal of providing the lowest possible power while satisfying performance needs. Low power techniques are either designed into the FPGA device itself or implemented automatically without user input needed.

This technical note serves as a usage guide for managing and determining the power consumption of Nexus 2 devices. The document details the conceptual and functional descriptions along with a guide to utilize the power saving functions. Analyzing power consumption in your design using the Lattice Radiant® software power calculator tool is also described.

2. Power Consumption and Calculation

The Lattice Radiant software includes the power calculator tool that can determine the power consumption of the Nexus 2 devices. The power calculator offers two modes: Estimation mode for what-if analysis, and Calculation mode for the more accurate application-specific power consumption by importing post-PAR UDB design files.

When running the power calculator tool in Estimation mode, you can provide estimates of the utilization of various components and the tool provides an estimate of the power consumption. This is a good start, especially for what-if analyses and device selection. The Estimation mode does not require a synthesized pattern in the Radiant software and can be run as a stand-alone tool.

The Calculation mode is a more accurate approach, where you can import the actual device utilization by importing the post-PAR netlist design file, or the UDB file. Additionally, the power calculator supports features like Trace Report or Trace Report (TWR) import, to get the clock frequencies for various clocks. The Trace Report feature only includes frequencies of the clocks nets that are constrained in the Preference file. You are still required to provide frequencies of the clocks that are not included in the Preference file and Trace Report.

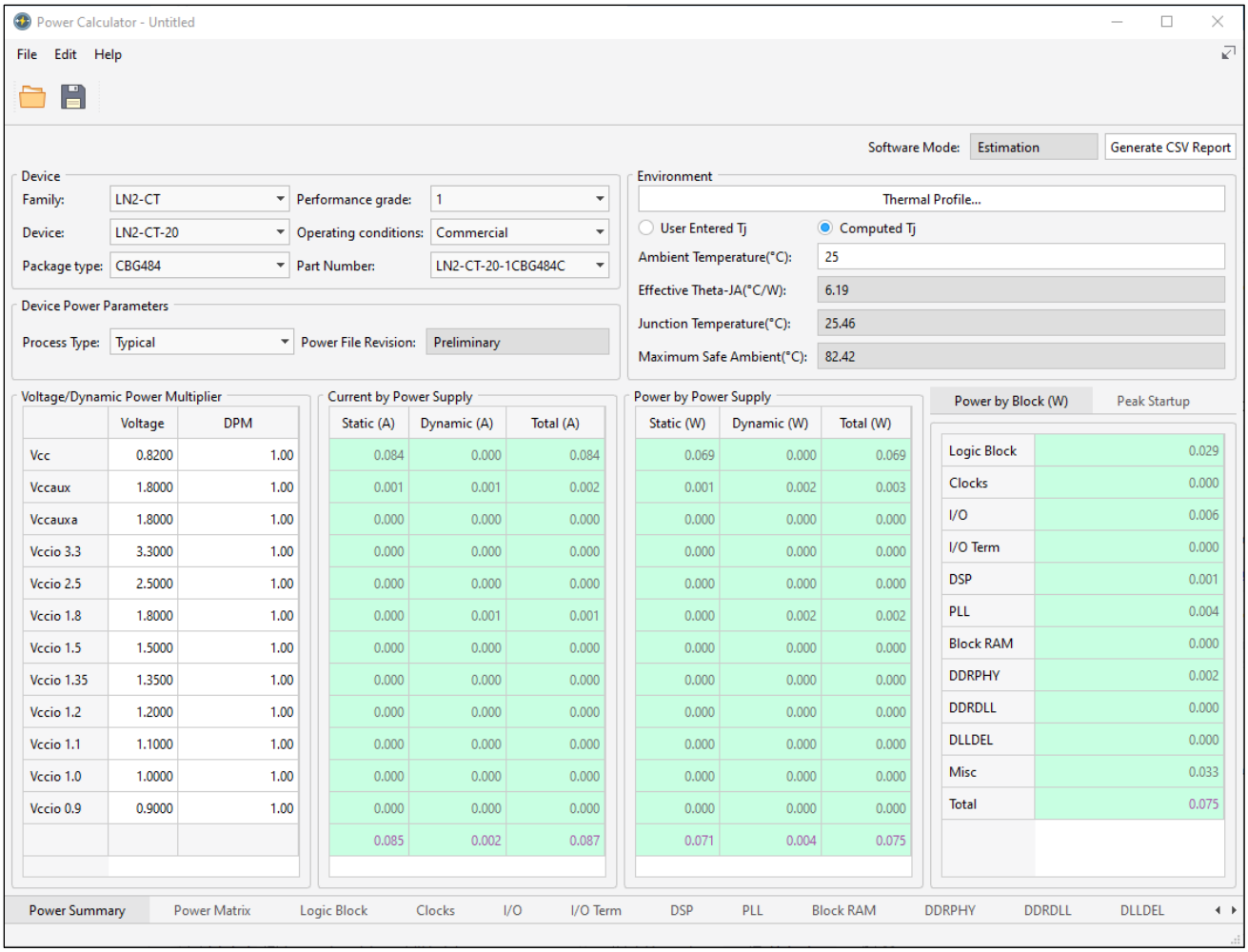
The default Activity Factor Percentage (AF%) for dynamic power calculation is set to 10% in the power calculator. You can change the default AF% for the entire project or for each clock net individually. The AF % is discussed in detail in the Activity Factor Calculation section.

2.1. Power Calculator

To start the power calculator from the Lattice Radiant software Tools menu or toolbar:

1. Open a project or create a new one.
2. Choose **Tools > Power Calculator**.

The power calculator main window opens in the Estimation mode or Calculation mode, depending on the design stage, and displays the Power Summary page as shown in Figure 2.1.



	Voltage	DPM
Vcc	0.8200	1.00
Vccaux	1.8000	1.00
Vccauxa	1.8000	1.00
Vccio 3.3	3.3000	1.00
Vccio 2.5	2.5000	1.00
Vccio 1.8	1.8000	1.00
Vccio 1.5	1.5000	1.00
Vccio 1.35	1.3500	1.00
Vccio 1.2	1.2000	1.00
Vccio 1.1	1.1000	1.00
Vccio 1.0	1.0000	1.00
Vccio 0.9	0.9000	1.00

Static (A)	Dynamic (A)	Total (A)
0.084	0.000	0.084
0.001	0.001	0.002
0.000	0.000	0.000
0.000	0.000	0.000
0.000	0.000	0.000
0.000	0.001	0.001
0.000	0.000	0.000
0.000	0.000	0.000
0.000	0.000	0.000
0.000	0.000	0.000
0.000	0.000	0.000
0.000	0.000	0.000
0.085	0.002	0.087

Static (W)	Dynamic (W)	Total (W)
0.069	0.000	0.069
0.001	0.002	0.003
0.000	0.000	0.000
0.000	0.000	0.000
0.000	0.000	0.000
0.000	0.002	0.002
0.000	0.000	0.000
0.000	0.000	0.000
0.000	0.000	0.000
0.000	0.000	0.000
0.000	0.000	0.000
0.000	0.000	0.000
0.071	0.004	0.075

Logic Block	0.029
Clocks	0.000
I/O	0.006
I/O Term	0.000
DSP	0.001
PLL	0.004
Block RAM	0.000
DDRPHY	0.002
DDRDLL	0.000
DLLDEL	0.000
Misc	0.033
Total	0.075

Figure 2.1. Power Calculator (Summary Tab for Nexus 2 Devices)

It is important to understand how the options available in power calculator affect the power. For example, if the ambient temperature is changed, the junction temperature is affected according to the following equation:

$$T_J = T_A + \theta_{JA\_EFFECTIVE} \times P$$

where T_J and T_A are the junction and ambient temperatures, respectively, and P is the power.

$\theta_{JA\_EFFECTIVE}$ is the effective thermal impedance between the die and its environment.

The junction temperature is directly dependent on the ambient temperature. An increase in T_A increases T_J and results in an increase in the static leakage component.

The Power can be affected by the *Process Type* selection or the frequency at which the application runs. The process primarily changes the static leakage or static power. The frequency changes the dynamic power. Increasing the frequency of toggling increases the dynamic component of power.

2.1.1. Typical and Worst Case Process

Process variation is a naturally occurring variation in the attributes of transistors such as length, widths, and oxide thickness, when integrated circuits are fabricated. Process variation causes measurable and predictable variance in the output performance of all circuits.

The Lattice Radiant software power calculator provides the option to select the *Typical* process type such as the mean current/power of distribution, and the *Worst Case* process type such as the maximum current/power of distribution, as a result of the variation. Process variation primarily affects the static leakage component of the device. The *Worst Case* power multiplier is derived from statistically correlated measurements of the manufacturing process.

The *Process Type* selection in power calculator allows you to understand the current and power variation of the devices and predicts accurate results that are application specific. These can be used for power supply design, battery capacity design, and thermal management for each application.

2.1.2. Junction Temperature

Junction temperature is the temperature of the die during operation. It is one of the most important factors that affects the device power. For a fixed junction temperature, voltage and device package combination, static power is fixed. The higher the junction temperature, the closer the part is to having thermal issues.

Ambient temperature affects the junction temperature. Devices operating in a high-temperature environment have higher leakage since their junction temperature is higher. The power calculator models the interdependence of ambient and junction temperatures. When you provide an ambient temperature, it is rolled into an algorithm that calculates the junction temperature and power through an iterative process to find the thermal equilibrium of the system as defined in the Lattice Radiant software with respect to its thermal environment such as T_A and heat dissipation, heat sink and/or airflow.

Thermal Impedance plays an important role in determining the devices behavior, and the tool takes it into account to calculate the maximum safe ambient temperature. See the Thermal Management section for details on how the power calculator uses thermal impedances.

2.1.3. Maximum Safe Ambient Temperature

Maximum safe ambient temperature is one of the most important numbers displayed in the *Summary* tab of the power calculator. This is the maximum ambient temperature at which the device application can run without violating the junction temperature limits for the grade of the device, commercial or industrial. The lower the maximum safe ambient temperature, the closer the part is to having thermal issues.

The power calculator uses an algorithm to accurately predict this temperature. The algorithm adjusts itself as you change options such as voltage, process, frequency, AF%, thermal impedance and so on, or any factor that may affect the power dissipation of the device.

Thus it becomes extremely important to provide more accurate inputs to the tool for more accurate predicted results.

2.1.4. Operating Temperature Range

When designing a system, make sure a device operates at specified temperatures within the system environment. This is particularly important to consider before a system is designed. With the power calculator, you can predict device thermodynamics and estimate the dynamic power budget. The ability to estimate device operating temperature prior to board design also allows you to better plan for power budgeting and thermal management.

Although total power, ambient temperature, thermal resistance, and heat dissipation contribute to device thermodynamics, the junction temperature as specified in Operating Conditions in the Lattice Nexus 2 Platform - Specifications Data Sheet (FPGA-DS-02121) is the key to device operation.

The allowed junction temperature range is 0 °C to 85 °C for commercial grade devices and –40 °C to 100 °C for industrial grade devices. If the junction temperature of the die is not within these temperature ranges, the performance, reliability, and functionality can be affected.

2.1.5. Dynamic Power Multiplier (DPM)

In general, for semiconductors devices, the dynamic power consumption is independent of the variation in process and temperature. The power calculator follows this rule, and hence any change to either process or temperature does not change the dynamic current or power.

To provide an option to add some safeguards, the power calculator includes the Dynamic Power Multiplier (DPM) or DPM column right next to the voltage supplies on the *Summary* tab. DPM allows you to add a multiplier to the dynamic current for each individual power supplies. This multiplier is included in the dynamic current equation.

DPM has a default value 1 that means the dynamic power is what is predicted by the power calculator. If you want to add 20%, additional dynamic power, the DPM can be set to 1.2 (1 + 20%) and it can be placed against the appropriate power supply. This increases the dynamic power for that supply by 20% and provides you with some guard band.

2.1.6. Peak Startup Current

The bottom right panel of the *Summary* tab in Lattice Radiant software power calculator includes the *Peak Startup* tab. This tab provides an important piece of information, especially for designing the capacity for power supply or batteries.

The *Peak Startup Current* tab provides the current that the Nexus 2 device pulls on each power supply when it is powered on. This includes device configuration when applicable. This tab also includes the time period for which this current lasts.

2.1.7. Power Budgeting

Both the Peak Startup current and the operational current of the device should be considered when budgeting for power supply or battery capacity. It is recommended that the higher of the two numbers be used as reference for capacity calculations.

2.1.8. Device Operational Limits

The power calculator provides the power dissipation of a design under a given set of conditions. It also predicts the junction temperature (T_J) for the design. Any time this junction temperature is outside the limits specified in Lattice Nexus 2 Platform - Specifications Data Sheet (FPGA-DS-02121), the viability of operating the device at this junction temperature must be re-evaluated.

A commercial device is likely to show speed degradation with a junction temperature above 85 °C and an industrial device at a junction temperature degrades above 100 °C. It is required that the die temperature be kept below these limits to achieve the guaranteed speed operation.

Operating a device at a higher temperature also means a higher static current and hence power. The difference between static current and total current is that both static and dynamic currents, at a given temperature, provide the power budget available. This is also very useful in power supply or battery capacity designs.

If the device runs at a current higher than this budget, the total current is also higher. This causes the die temperature to rise above the specified operating conditions. The four factors of power, ambient temperature, thermal resistance, and heat dissipation, can also be varied and controlled to reduce the junction temperature of the device. The power calculator is a powerful tool to help system designers manage FPGA power usage to improve overall system reliability.

The power calculator clearly indicates when the application is running power higher than recommended. If the junction temperature goes beyond the grade limits, the box turns red in the *Summary* tab. The junction temperature calculations are provided up to 125 °C, which is also the reliability limit for the Nexus 2 devices. If the junction temperature is beyond 125 °C under the conditions provided, the tool indicates it by 125+. This shows that the device achieves thermal equilibrium beyond 125 °C.

In certain cases, the thermal equilibrium cannot be achieved by the application under given conditions. In such situation, the device can continue to generate and not dissipate heat. The power calculator has a built-in algorithm to determine such situations. This is indicated with 125++ under junction temperature calculation. This situation should be avoided under all circumstances, as this can cause permanent damage to the device.

2.1.9. Activity Factor Calculation

The Activity Factor % (AF%) is defined as the percentage of frequency or time that a signal is active or toggling the output. Most resources associated with a clock domain are running or toggling at some percentage of the frequency at which the clock is running. You must provide this value as a percentage under the AF% column in the power calculator tool.

Another term for I/O is the I/O Toggle Rate. The AF% is applicable to the PFU, Routing, and Memory Read Write Ports, and so on. The activity of I/O is determined by the signals you provided in the case of inputs, or as an output of the design in the case of outputs. The rates at which the I/O toggles define their activity. The I/O Toggle Rate or the I/O Toggle Frequency is a better measure of their activity.

The Toggle Rate (TR) in MHz of the output is defined in the following equation:

$$\text{Toggle Rate (MHz)} = 1/2 \times f \times \text{AF\%}$$

You are required to provide the TR (MHz) value for the I/O instead of providing the frequency and AF% for other resources. AF% can be calculated for each routing resource, output or PFU. However, this involves long calculations. The general recommendation for a design occupying roughly 30% to 70% of the device is an AF% between 15% and 25%. This is an average value. The accurate value of an AF% depends upon clock frequency, stimulus to the design and the final output.

The power calculator allows you to import a Value Change Dump (VCD) file from the simulation to accurately assess the AF% of the design (*Edit > Open Simulation File*). The VCD file is based on post-PAR simulation, and it is an ASCII file generated by the simulator. Check the simulation tool document on how to generate a VCD file. The AF% calculated from the VCD file is based on how accurate the test-bench or stimulus is for the simulation.

2.1.10. Power Calculator Assumptions

The following are the assumptions made by the power calculator:

- The power calculator tool uses default ambient temperature of 25°C which is the room temperature. This default temperature can be changed.
- You can define the ambient temperature (TA) for device junction temperature (TJ) calculation based on the power estimation. TJ is calculated from the user-entered TA and the power calculation of typical room temperature.
- I/O power consumption is based on an output loading of 5 pF. You can change this capacitive loading.
- You can estimate power dissipation and current for each type of power supply, VCC and VCCIO.
- The nominal VCC is used by default to calculate power consumption. A lower or higher VCC can be chosen from a list of available values.
- θ_{JA} can be changed to better estimate the operating system manually or by entering Airflow in linear feet per minute (LFM) along with a heat sink options.
- The AF% is defined as the toggle rate of the registered output. For example, assuming that the input of a flip-flop is changing at every clock cycle, 100% AF% of the flip-flop running at 100 MHz, is 50 MHz.
- The default AF% for logic is 10%.
- You can import the VCD file from the simulation to get AF% based on the simulation. It is to be noted that the AF% from VCD is as good as the coverage in the simulation. Refer to Radiant Help or the Lattice Semiconductor website for more details on this process, which can significantly improve correlation between the power calculator and silicon.
- Unused I/O are configured as LVCMOS Inputs with weak internal pull ups.
- You can import the frequency from a trace report (TWR).

- The operating junction temperature range for commercial grade devices is 0°C to 85°C, and for industrial grade devices is –40°C to 100°C. For details, refer to the DC Electrical Characteristics section of Lattice Nexus 2 Platform - Specifications Data Sheet (FPGA-DS-02121).
- For thermal impedance, The power calculator default value is based on a medium size board (6" × 6", 6 layers), with no heatsink and 200 LFM airflow. This can be changed as needed under Thermal Profile section in the tool.

3. Thermal Management

To improve reliability and prevent device failure, all electronic devices are required to dissipate the heat generated while running. Thermal management refers to the techniques used to improve heat dissipation. The methods include the use of heatsinks, fans for air cooling, and also other forms of cooling like liquid cooling in modern computers.

Nexus 2 devices are designed to be low power. By combining power reduction techniques and low power design, the average power consumption and heat generated can be reduced. This section covers the understanding and ways to improve thermal management for applications using the Nexus 2 devices.

3.1. Thermal Impedance and Airflow

A common method for characterizing a packaged device thermal performance is with thermal impedance, represented by θ. For a semiconductor device, thermal resistance indicates the steady state temperature rise of the die junction above a given reference for each watt of power (heat) dissipated at the die surface. Its unit is degree Celsius per Watt (°C/W).

The most common examples are:

- θ_{JA}, Thermal Resistance Junction-to-Ambient (in °C/W)
- θ_{JC}, Thermal Resistance Junction-to-Case (in °C/W)
- θ_{JB}, Thermal Resistance Junction-to-Board (in °C/W)

Knowing the reference temperature such as the ambient, case, or board temperature, the power, P, and the relevant θ value, the junction temperature can be calculated per following equations:

- $T_J = T_A + \theta_{JA} * P$
- $T_J = T_C + \theta_{JC} * P$
- $T_J = T_B + \theta_{JB} * P$

where T_J, T_A, T_C, and T_B are the junction, ambient, case/package, and board temperatures (in °C), respectively. P is the total power dissipation of the device.

θ_{JA} is commonly used with natural and forced convection air-cooled systems. θ_{JC} is useful when the package has a high conductivity case mounted directly to a PCB or heatsink. θ_{JB} applies when the board temperature adjacent to the package is known.

To improve airflow effectiveness, it is important to maximize the amount of air that flows over the device or the surface area of the heat sink. The airflow around the device can be increased by providing an additional fan or increasing the output of the existing fan. If this is not possible, baffling the airflow to direct it across the device may help. This means the addition of sheet metal or objects to provide the mechanical airflow guides that direct air to the target device. Often the addition of simple baffles can eliminate the need for an extra fan. In addition, the order in which air passes over devices can impact the amount of heat dissipated.

3.2. Thermal Management in Power Calculator

Lattice Radiant software power calculator utilizes the ambient temperature (°C) to calculate the junction temperature (°C) based on θ_{JA} for the targeted device. You can also provide the airflow values to obtain a more accurate junction temperature value. The airflow values are measured in linear feet per minute (LFM), which is the same as cubic feet per minute.

Thermal Environment options in the power calculators provide a thermal impedances for JEDEC (4”x 4”, 2S2P), small (6”x 6”, 6 layered board), medium (8”x8”, 8 layered board), and large (10”x10”, or larger board). There are also options to select copper heatsinks of different sized fins. These impedances and options are provided as guidance. You also have the option to provide your own thermal impedance.

As each application board can be different, it is recommended to provide accurate thermal impedance. This can be obtained by measuring in a thermal lab or by using a thermal simulation software.

3.3. DELPHI Models

DELPHI models are thermo-mechanical models that can be used to simulate thermal behavior of the electronic devices in a system. These tools can simulate the thermal behavior of the system and predict the thermal impedance for each component. The thermal impedance obtained using simulation methods can be entered in the Thermal Environment in the power calculator.

DELPHI Models for the Nexus 2 device can be downloaded from the web, and they are compatible with Mentor Graphics® FloTHERM® and Ansys Icepak tools.

4. Conclusion

The Nexus 2 devices are designed in hardware and software to the lowest possible power at expected performance metrics. The power calculator tool allows you to predict static and dynamic power and determine which IP blocks are contributing to the total power.

By utilizing the user-friendly interface to access these features in the Lattice Radiant software, applications can utilize these features to the maximum extent and have predictable and reliable device performance.

References

- Certus-N2 web page

A variety of technical notes for the Lattice Nexus 2 platform are available.

- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Lattice Nexus 2 Embedded Memory User Guide (FPGA-TN-02366)
- Lattice Nexus 2 Hardware Checklist (FPGA-TN-02317)
- Lattice Nexus 2 High-Speed I/O and External Memory Interface (FPGA-TN-02372)
- Lattice Nexus 2 sysCLOCK PLL Design and User Guide (FPGA-TN-02364)
- Lattice Nexus 2 sysDSP User Guide (FPGA-TN-02362)
- Lattice Nexus 2 sysCONFIG User Guide (FPGA-TN-02370)
- Lattice Nexus 2 sysI/O User Guide (FPGA-TN-02365)
- Lattice Nexus 2 SED/SEC User Guide (FPGA-TN-02380)
- Lattice Nexus 2 Power User Guide (FPGA-TN-02381)
- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)
- sub-LVDS Signaling Using Lattice Devices (FPGA-TN-02028)
- Thermal Management (FPGA-TN-02044)
- Using TraceID (FPGA-TN-02084)

For more information on Lattice Nexus 2-related IP, reference designs, and board documents, refer to the following pages:

- SGMII and Gb Ethernet PCS IP Core – Lattice Radiant Software (FPGA-IPUG-02077)
- IP and Reference Designs for Lattice Nexus 2
- Development Kits and Boards for Lattice Nexus 2

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL) – www.jedec.org
- PCI – www.pcisig.com

Other references:

- Lattice Insights for Lattice Semiconductor training courses and learning plans
- Lattice Radiant FPGA design software

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 0.80, December 2024

Section	Change Summary
All	Preliminary release.

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