Lattice Nexus 2 SED/SEC User Guide

Preliminary Technical Note

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
CRC	Cyclic Redundancy Check
CRAM	Configuration Random Access Memory
EBR	Embedded Block RAM
ECC	Error Correction Code
IP	Intellectual Property
PLD	Programmable Logic Device
SEC	Soft Error Correction
SED	Soft Error Detection
SEDC	Soft Error Detection/Correction
SEI	Soft Error Injection
SEU	Single Event Upset
SRAM	Static Random Access Memory

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1. Introduction

This document describes the hard-logic soft error detection (SED) and soft error correction (SEC) implemented in the Lattice Nexus™ 2 device platform. When a soft error is detected, the Nexus 2 devices provide an easy way to optionally perform SEC without affecting the functionality of the device.

Memory errors can occur when high-energy charged particles alter the stored charge in a memory cell in an electronic circuit. The phenomenon first became an issue in Configuration Random Access Memory (CRAM), requiring error detection and correction for large memory systems in high-reliability applications. As device geometries continue to shrink, the probability of memory errors in Static Random Access Memory (SRAM) becomes significant for some systems.

SRAM-based programmable logic devices (PLDs) store logic configuration data in SRAM cells. As the number and density of SRAM cells in a PLD increase, the probability that a memory error alters the programmed logical behavior of the system increases. Most traditional approaches that are taken to address this issue involve soft intellectual property (IP) cores that you instantiate in your design. Such approaches utilize valuable resources, possibly affecting design performance.

The Nexus 2 devices have an improved hardware-implemented SEDC circuit that can be used to detect and correct SRAM errors. There are two layers of SED/SEC, error correction code (ECC) logic to detect and correct single bit error per data frame and detect two-bit errors and cyclic redundancy check (CRC) logic to detect multi-bit errors in the device.

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2. Overview of the SEDC IP

The Soft Error Detection/Correction (SEDC) IP offers the following enhanced features:

- Frame-by-frame SED check
- Multiple regions run in parallel for fast SED and SEC performance
- Single-bit and multi-bit error detection
- ECC to correct single bit error at the frame level
- Programmable SEDC clock
- Force error capability for system-level simulation

The SEDC module is part of the sysCONFIG block in the Nexus 2 devices. The configuration data is divided into frames in multiple regions. The SED hardware reads data from the FPGA's configuration memory frame-by-frame in the background while the device is in user function mode and performs ECC calculation on every frame of configuration data (see Figure 2.1). When a single-bit error is detected, a single event upset (SEU) notification is generated and the SED resumes operation after the single-bit error is corrected. Single-bit errors are corrected when SEC is enabled. The corrected value is rewritten to the frame using ECC information. If more than one bit errors are detected within one frame of configuration data, an error message is generated. In parallel, CRC is calculated for the entire CRAM contents along with ECC. After the ECC is calculated on all frames of configuration data, CRC is calculated for the configuration data in the entire device. Full-chip CRC and frame-by-frame ECC calculations do not include Embedded Block RAM (EBR). EBRs provide a separate and optional ECC for SED/SEC of the EBR content. Distributed RAM data stored in the CRAM are masked during SED/SEC because RAM content may change during user operation and hence cannot be covered by the SEDC IP without generating false SEDC errors. The distributed RAM enable bit set in CRAM is covered during SED/SEC.

The SEDC IP is part of the sysCONFIG block in the Nexus 2 devices. Figure 2.1 shows the system-level view of the SEDC IP.

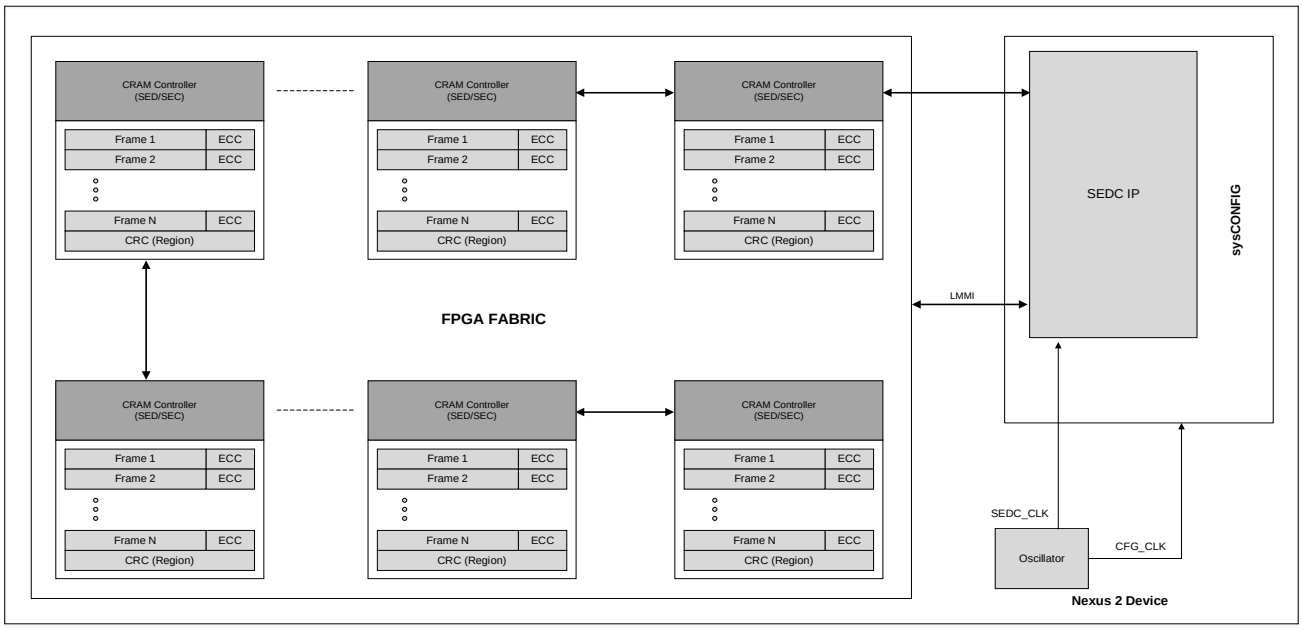

Figure 2.1. SEDC System Block Diagram

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2.1. SEDC IP Clock and Reset

The SEDC circuitry is driven by the FPGA's internal oscillator.

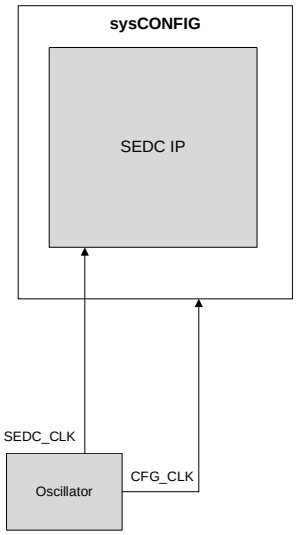

Figure 2.2. SEDC IP Clock and Reset

The default oscillator frequency is 200 MHz. You can set the SEDCLK_divider setting in the SEDC IP from the Lattice Radiant™ software IP catalog anywhere between 2 to 256 in integer increments resulting in a frequency range from 200 MHz to 1.56 MHz (SEDC oscillator frequency = 400 MHz / SEDCLK_divider).

Table 2.1. SEDC Internal Oscillator Divider Settings

Divider Setting	SEDCLK_Divider	SEDC Clock Frequency (MHz)
Divide by 2	2	200
Divide by 3	3	133.33
…	…	…
Divide by 256	256	1.56

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3. SEDC Flow

This section describes the SEDC flow. The SEDC flow is executed once V_{CC} reaches the data sheet V_{CC} minimum recommended level and SEDC is started.

The Nexus 2 devices have an advanced SEDC flow with two levels of SEDC checks. In the first level of SED check, the CRAM content is read one frame at a time and the SED check is performed on a frame-by-frame basis. After all the frames of the device CRAM content are read, the SEDC module performs a CRC of the entire CRAM contents (second-level SED) to check for any multi-bit errors which were not detected by ECC.

The Nexus 2 devices are built to support real-time SEC in which a single-bit soft error can be corrected using ECC at the frame level. A multi-bit soft error detected within a frame is non-correctable. Figure 3.1 shows the SEC flow in the Nexus 2 devices.

The Nexus 2 devices perform a one-time scan of all frames and can detect single-bit (1 bit) and multi-bit (2 bits or more) soft errors. When a single-bit soft error is detected, the hardware halts, notifies the user about the error, and waits for the instruction to proceed. Once the instruction to resume scanning is set, the hardware corrects the 1-bit error, rescans the region where the corrected frame is located, and resumes scanning the remaining frames. When a multi-bit soft error is detected, the hardware notifies the user about the error and continues scanning the remaining frames because a multi-bit soft error is non-correctable.

The following are the bit error reporting schemes:

- When a single-bit soft error is detected, the SEDC IP reports the following:
  - An error indicator with error type of 1-bit error
  - Error bit location
  - Error frame location
  - Error region location
- When a multi-bit soft error is detected, the SEDC IP reports the following:
  - An error indicator with error type of multi-bit (uncorrectable) error
  - Error frame location
  - Error region location
- After a complete scan of the CRAM content, if any soft error was detected, the SEDC IP reports the following:
  - An error indicator with error type of full-chip CRC

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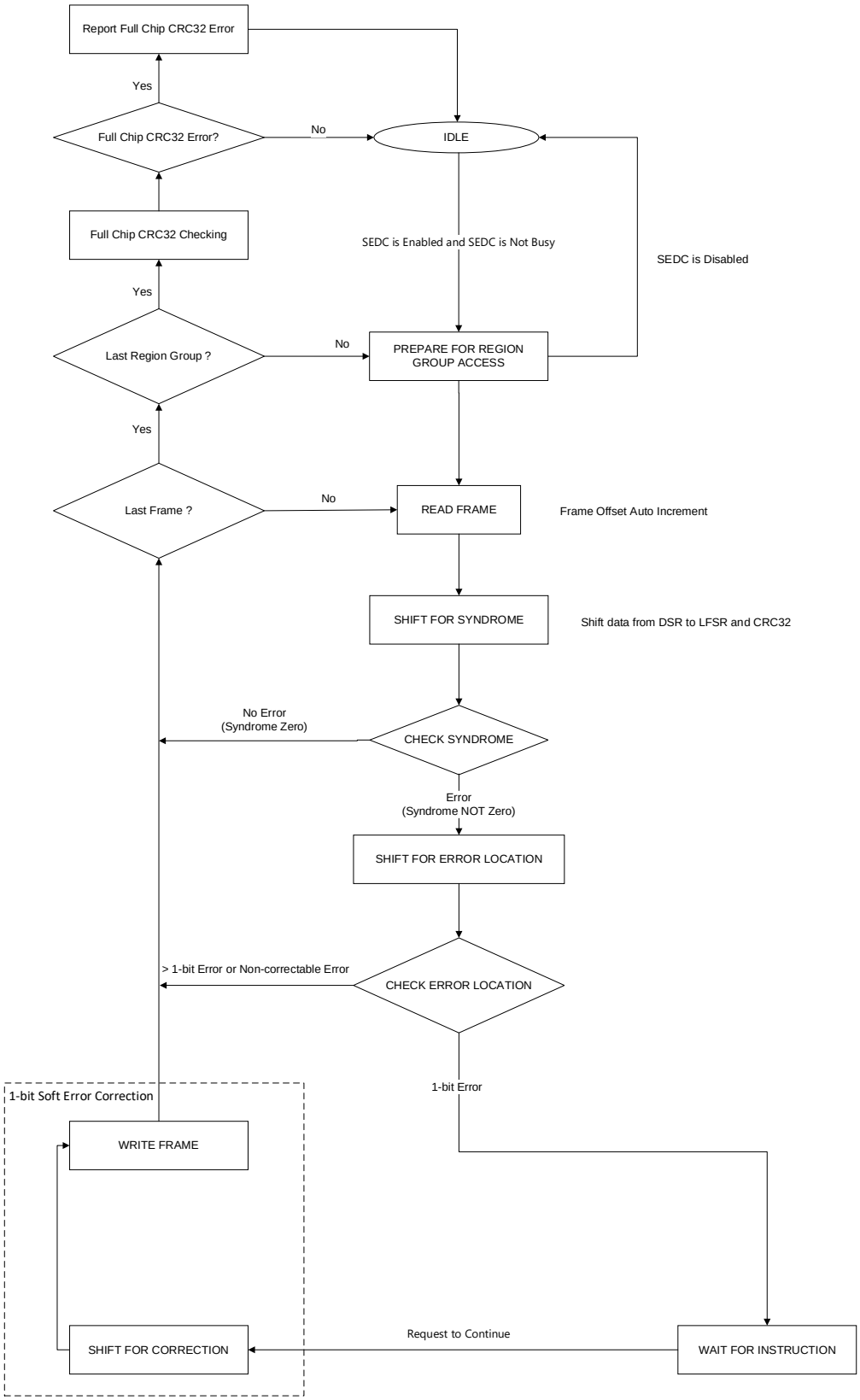

Figure 3.1. SEDC Flow

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4. Soft Error Injection

The Radiant soft error injection (SEI) tool offers an easy and economical way to emulate soft error impact on the overall system. This tool allows the user to randomly generate and program one or multiple soft errors into the device in background mode without affecting device function. The Radiant SEI tool for the Nexus 2 devices will be supported in the Lattice Radiant software.

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5. Important Note

- SEDC operation will be interrupted once any PROG_QUALIFY target configuration command is clocked into the device. It is recommended that the SEDC operation be stopped before sending a PROG_QUALIFY target configuration command and restarted after the command is completed.

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References

- Certus-N2 web page
- Lattice Radiant Software web page
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

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Revision History

Revision 0.80, December 2024

Section	Change Summary
All	Initial preliminary release.

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