Rapid Prototype Work Flow with HDL Coder

5G OFDM and Single Tone Modulation Use Case

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Abstract

This paper presents key technologies in many communication systems including a novel Orthogonal Frequency Division Multiplexing (OFDM) and Single Tone modulation implementation in FPGAs. The design, developed through the integration of RTLs generated by HDL Coder™ and hand-coded RTLs, can switch between OFDM and single tone patterns. This is particularly useful for wireless link testing.

This paper addresses a common problem encountered during the initial bring-up of a wireless link on FPGA- the unavailability of a host controller to feed OFDM patterns into the FPGA. The OFDM and Single tone modulator allows testing of the JESD204 link to analog front end without any dependency on the host, significantly improving the efficiency of the testing process.

The design can be implemented directly in the Lattice FPGA core, saving cost and reducing development turn-around-time. It was also verified through RTL and gate-level simulation in ModelSim as well as hardware testing on the Lattice CertusPro™-NX (CPNX) FPGA development kit.

In conclusion, this paper presents a novel OFDM and single tone modulator design for Lattice FPGA devices, simplifying the process of wireless link validation and reducing both the cost and time required.

Disclaimers

Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Introduction

Orthogonal Frequency Division Multiplexing (OFDM) and Single Tone modulation are key technologies used in many wireless and wired communication systems especially 5G and Wi-Fi 4/5/6/7 standards. OFDM is known for its high spectral efficiency, robustness to channel fading, and flexibility. Single Tone testing, on the other hand, is a simpler form of signal generation often used for basic system verification and troubleshooting.

This paper introduces a novel solution to a common problem encountered in these systems - the need for complex test patterns that can be difficult to generate without a host controller. The design and implementation of a OFDM and Single Tone modulator that can switch between OFDM and single tone patterns is presented in this paper. The design was developed through the integration of RTLs generated by HDL Coder and hand-coded RTLs.

Dependency on host for OFDM patterns would necessitate the bring up of matching interface between FPGA and host, such as PCIe, as well as host software required to perform the test before the wireless link test can commence. This process is not only time-consuming and inefficient, but also challenging to debug when issues arise.

The OFDM and Single Tone modulator can be directly connected with the JESD204B IP in FPGA, sending OFDM and single tone patterns to validate the JESD204B link. With the introduction of the OFDM and Single Tone modulator, we can now validate the wireless link without any dependency on the host, significantly improving the efficiency of the testing process.

OFDM and Single Tone Modulator Design

Design Details

As the name indicates, this design supports two types of pattern generation - OFDM pattern and single tone pattern. Users can switch between these patterns in real-time using a single control signal. The high-level block diagram of the design shows two data paths - the top path for OFDM pattern generation and the bottom path for single tone pattern generation.

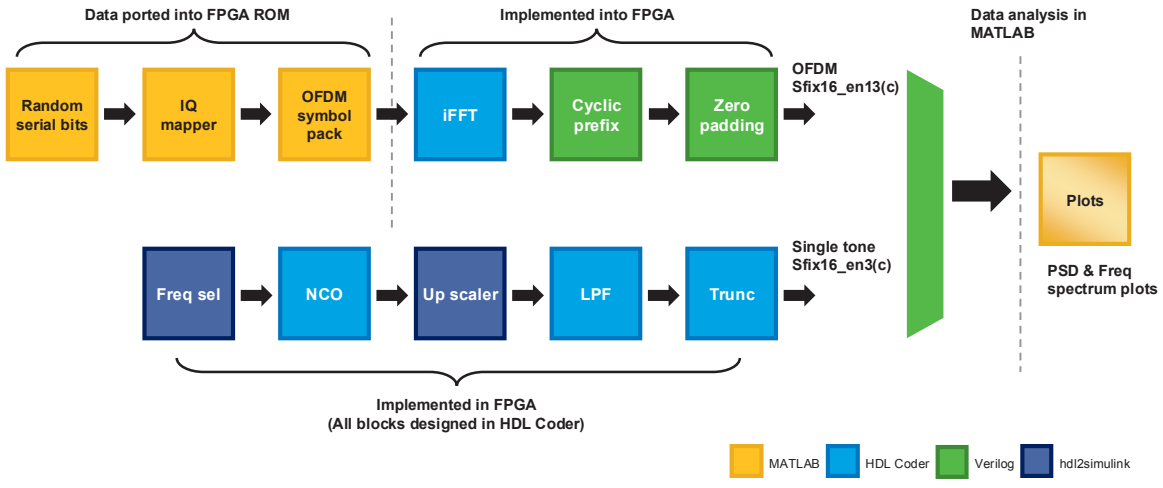

Figure 1. Block diagram of the OFDM and Single Tone modulator design

The design leverages various design techniques and tools, including MATLAB®, Simulink®, HDL Coder, and hand-coded RTL. The color coding in the Figure 1 differentiates the implementation methods:

- **Yellow:** Blocks implemented with MATLAB
- **Blue:** Blocks implemented with HDL Coder
- **Green:** Blocks implemented with hand-coded Verilog
- **Purple:** Blocks imported from hand-coded Verilog to Simulink

OFDM Pattern Generation

The OFDM pattern generator continuously repeats and outputs the same OFDM symbol with its cyclic prefix. In the OFDM data path, random modulation symbols are pre-generated in MATLAB and stored in a FPGA ROM. These symbols then go through the IFFT, cyclic prefix, and zero padding blocks to form the OFDM pattern and generates IQ data to feed to the RF Front End.

The following table shows the OFDM pattern system parameters used in the design.

Parameter	Value
FFT Size (Total number of Subcarriers)	1024
Number of Data Subcarriers	800
Number of Guard Subcarriers	224
Subcarrier Spacing	30 KHz
Modulation	64QAM
Number of OFDM Symbols	1
FIR	No
DAC Number of Input bits	16

Table 1. OFDM pattern system parameters

Single Tone Pattern Generation

The single tone pattern generator consists of an NCO with real-time configurable frequencies of 1 MHz, 2 MHz, 3 MHz, 4 MHz, and 5 MHz. In the single tone data path, a multi-frequency NCO generates sinusoidal signals at different frequencies. The frequency selector block allows users to switch among these supported frequencies through 3-bit input signals. The output from the NCO goes through upscalers to boost the amplitude. The low pass filters smooths the signals and removes noise. Finally, the FIR output is truncated to 16-bit complex signals to form the single tone test pattern.

Unique Features and Advantages

- Real-time Switching: The design allows real-time switching between OFDM and single tone patterns using a single control signal.
- Integrated Design: Users can implement this design directly in the FPGA core without the need for external equipment.
- Cost and Time Efficiency: This design reduces the cost and time associated with purchasing or loaning external equipment and setting up complex systems.
- Comprehensive Verification: Users can hook up with the JESD204B IP or similar interfaces in the FPGA and perform verification from functional simulation to hardware validation on development kits.

Design Process

This section discusses the design process for the OFDM and Single Tone modulator design, starting from MATLAB model implementation to Lattice FPGA implementation.

Development Flow

The development flow for the OFDM and Single Tone modulator design in Lattice FPGA begins with model implementation in MATLAB. This model is then translated to Simulink model using the HDL Coder and DSP HDL Toolbox™ libraries. Simulation results from Simulink is verified against the initial MATLAB model. Next, HDL code generation takes place where RTL files are generated through HDL Coder. These RTL files are then integrated with hand-coded RTL to form the complete design. RTL and gate-level simulations are conducted in Modelsim to verify functionality, with results compared against Simulink simulations. Finally, the design is implemented on a Lattice FPGA development kit, and hardware output results are checked against RTL and gate-level simulations. Any discrepancy observed during verification prompts debugging and revisiting previous stages for updates.

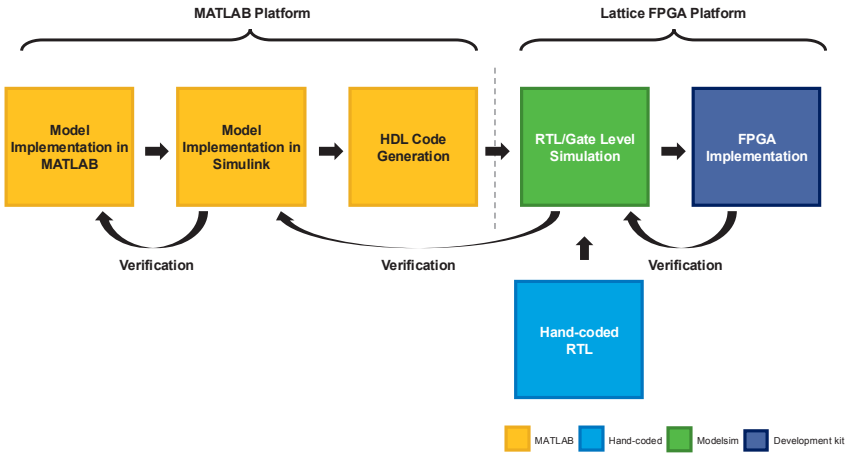

Figure 2. Development flow for the OFDM and Single Tone modulator design

HDL Generation with HDL Coder

The following shows the typical steps to generate HDL files from HDL Coder using the single tone pattern generator as an example.

- Instantiate the required blocks from the HDL Coder and DSP HDL Toolbox libraries in Simulink
- Configure the block parameters for your target requirement
- Configure the Data Type of the input and output ports
- Connect the blocks and ports to create a subsystem
- Add test benches to validate the subsystem in Simulink
- Configure the HDL generation settings at Settings -> HDL Code Generation Settings menu.
- Specify required parameters such as Language (VHDL/Verilog/SystemVerilog)
- Generate the HDL files using the “Generate HDL Code” icon

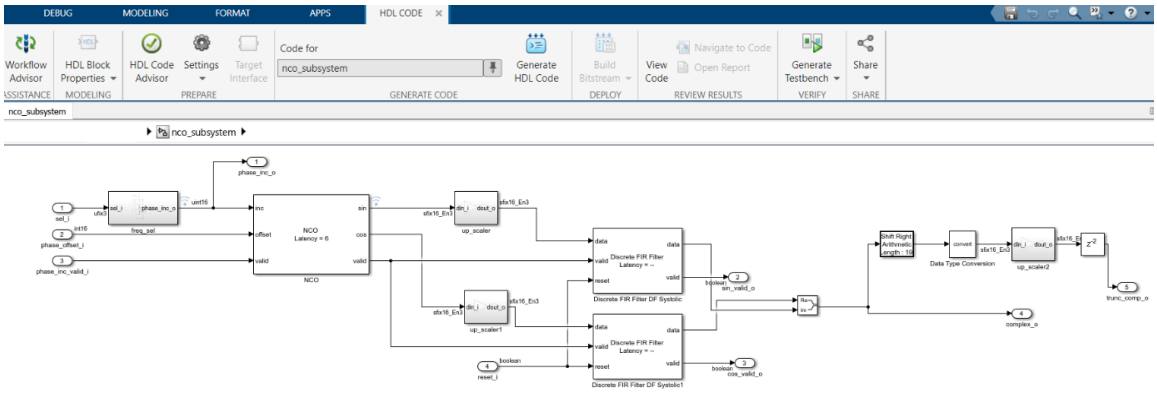

Figure 3. Block diagram of the Single Tone pattern generator design in Simulink

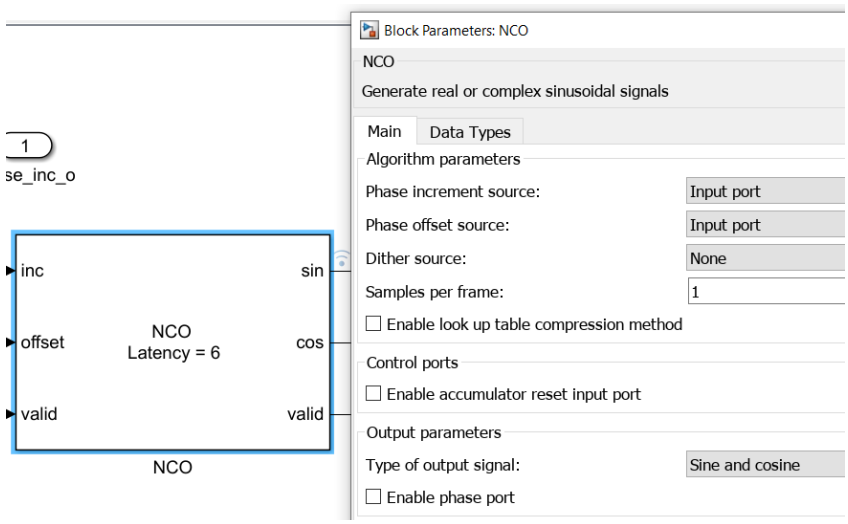

Figure 4. Example of NCO block parameters configuration

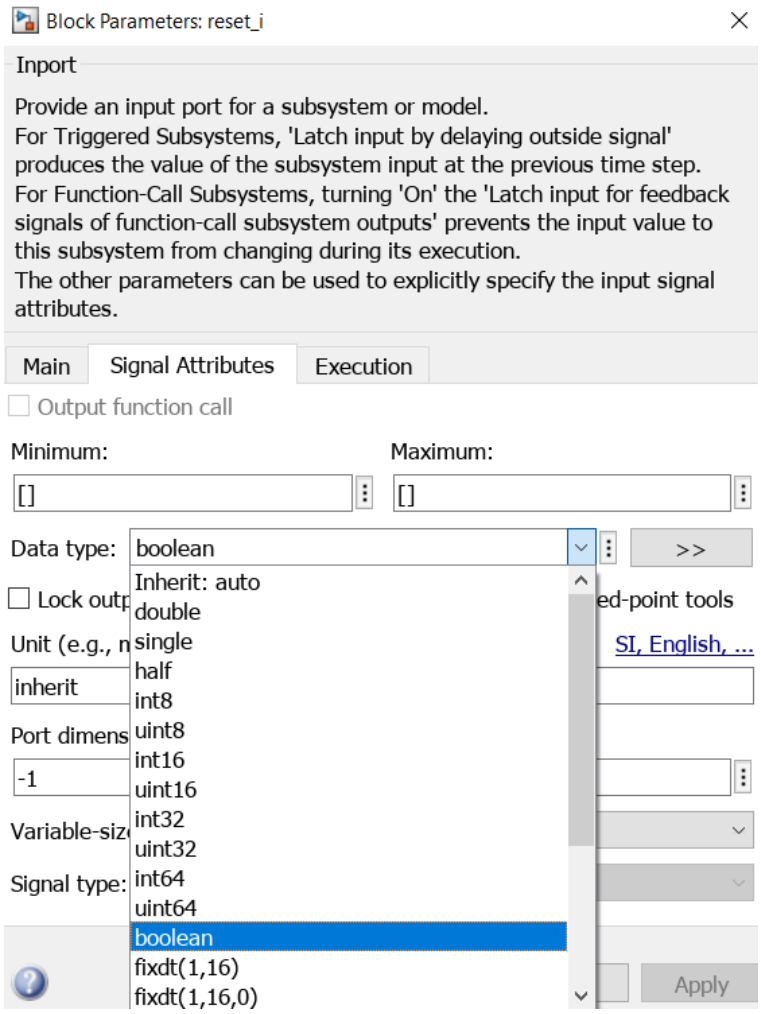

Figure 5. Example of Data Type for input and output ports

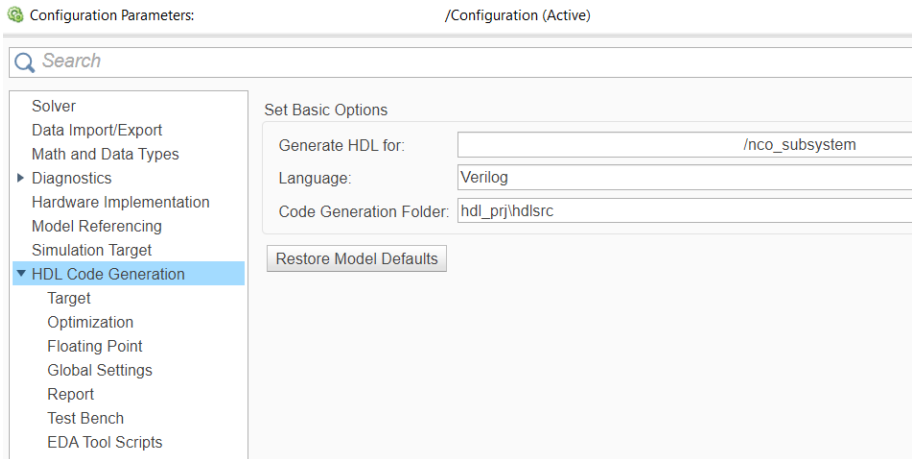

Figure 6. Example of HDL Code Generation Settings

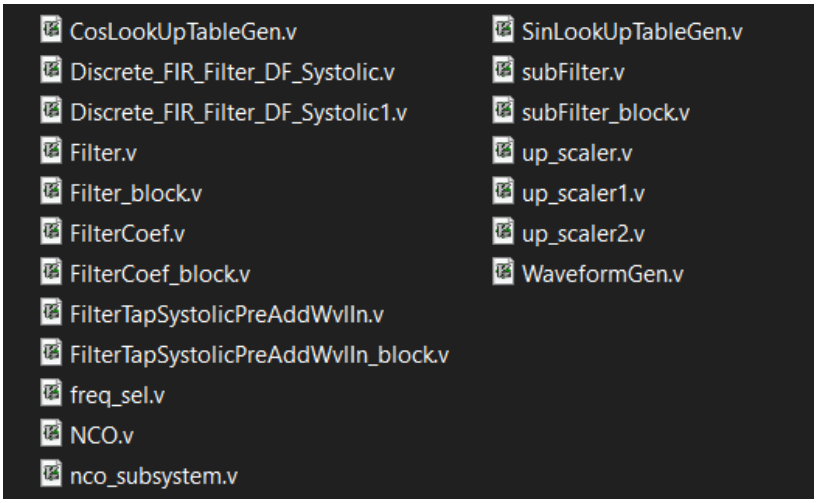

Figure 7. Example of Verilog HDL files generated

Implementation

The design was implemented on the CertusPro-NX (CPNX) device using the CertusPro-NX PCIe Bridge Board. The design runs on a 122.88 MHz clock generated from a Phase-Locked Loop (PLL) with a single-ended reference clock of 125 MHz available on-board.

Software and Hardware Used

The software and hardware used in this design are as follows:

Software:

- MATLAB R2023b
- Simulink
- HDL Coder
- DSP HDL Toolbox
- Communication Toolbox™
- Lattice Radiant™ Software Version 2023.2.0.38.1
- ModelSim Lattice FPGA Edition 2023.3
- Fixed-Point Designer™

Hardware:

- Lattice CertusPro-NX FPGA (Package LFCPNX-100-9LFG672I)
- CertusPro-NX PCIe Bridge Board

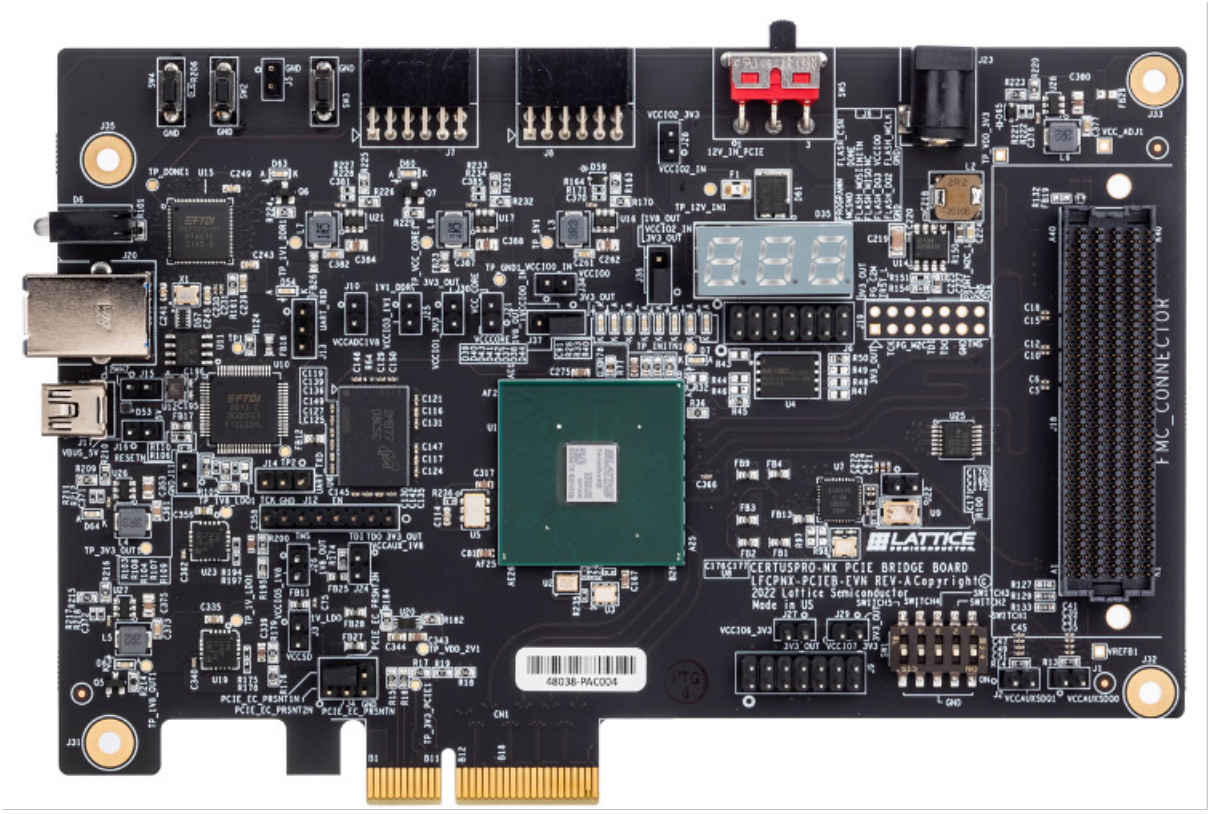

Figure 8. Top view of the CertusPro-NX PCIe Bridge Board

Pin Assignments

Pin Name	Pin Location	Description
clk_i	P24	Single ended global clock
resetn_i	J21	Dip switch, Active low system reset
sel_i[2:0]	[J25, K24, K20]	Dip switches, NCO frequency selection (3'b001: 1 MHz, 3'b010: 2 MHz, 3'b011: 3 MHz, 3'b100: 4 MHz, 3'b101: 5 MHz, Default: 5 MHz)
pat_sel_i	H26	Select between OFDM and single tone test pattern (1'b0: Single tone, 1'b1: OFDM)

Table 2. Pin assignment for the design in the CertusPro-NX PCIe Bridge Board

Design Verification

This design was verified through RTL and gate-level simulation in Modelsim as well as hardware tested on the CertusPro-NX development kit. This comprehensive verification process ensures the robustness and reliability of the design implementation. The following sections describe the test methodologies used.

Modelsim Simulation

- Simulated signal waveform is visually inspected
- Test bench printed OFDM and single tone output data is compared with reference data from Simulink
- The same output data is also used to plot Power Spectral Density (PSD) and frequency spectrum in MATLAB for further analysis.
- The above steps are repeated for gate-level simulated data

Hardware Testing on CertusPro-NX PCIe Bridge Board

- OFDM and single tone output data is captured using Reveal Analyzer
- The captured data is ported into Modelsim for visual inspection
- The data is also ported into MATLAB for PSD and frequency spectrum plotting

Results and Discussion

RTL Simulation Results

The RTL and gate-level simulation waveforms for both the single tone signals at 5 MHz and OFDM signals were captured.

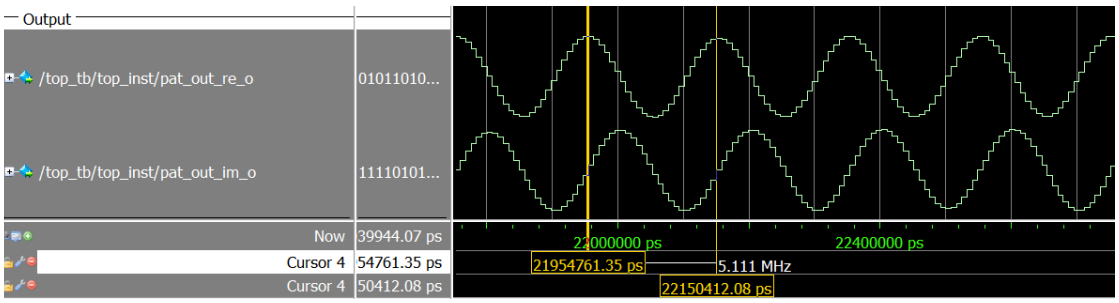

Figure 9. Complex single tone 5 MHz sinusoidal output in RTL simulation

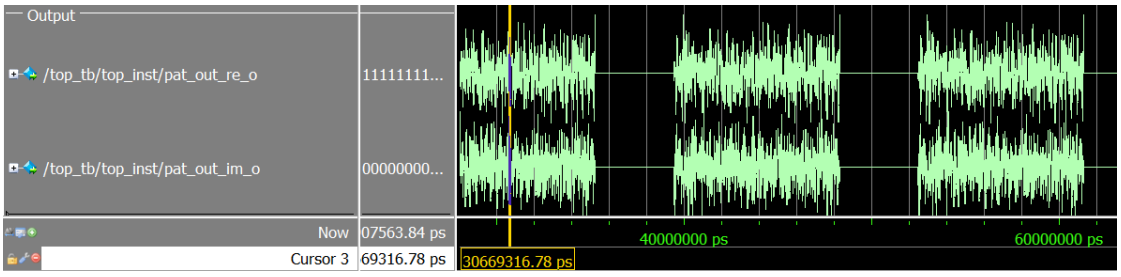

Figure 10. Complex time-domain OFDM output in RTL simulation

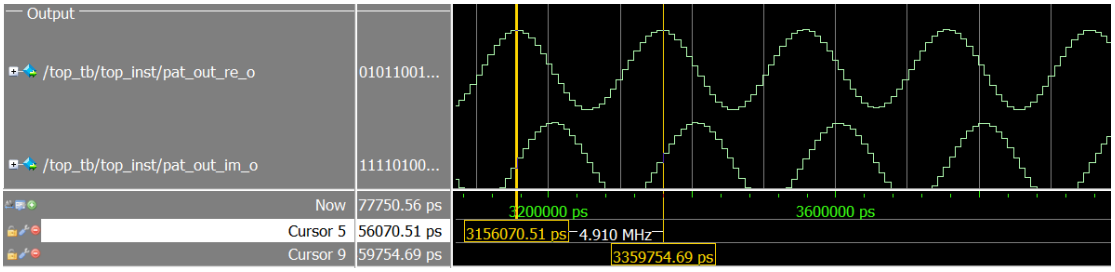

Figure 11. Complex single tone 5 MHz sinusoidal output in gate-level simulation

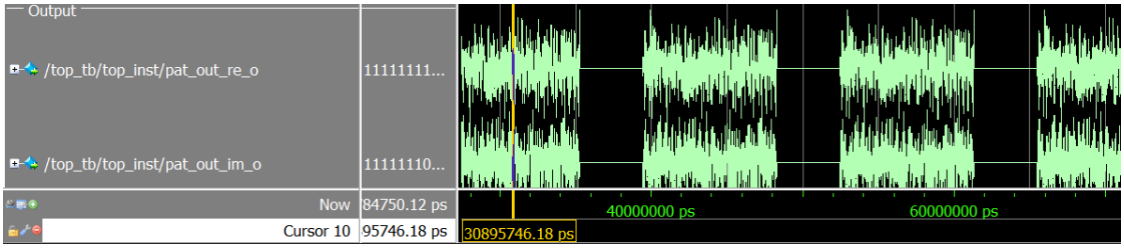

Figure 12. Complex time-domain OFDM output in gate-level simulation

The key observations from the simulation results are:

- The single tone signals are of the expected sinusoidal shape and with correct frequency from the Modelsim measurement.
- The OFDM signals match the expected burst pattern.
- The test bench printed simulated output data of the single tone and OFDM signals is matching RTL simulation and gate-level simulation.
- The printed data is also verified to match the reference values from Simulink simulation.

Hardware Testing on CertusPro-NX PCIe Bridge Board

The Reveal Analyzer output data was ported into Modelsim for single tone signals at 5 MHz and OFDM signal.

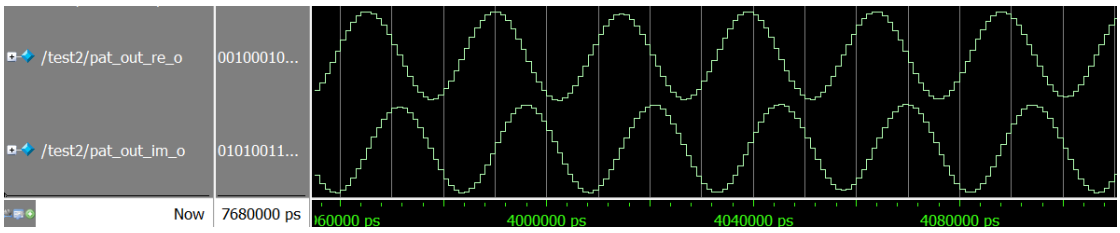

Figure 13. Complex single tone 5 MHz sinusoidal output captured by Reveal Analyzer

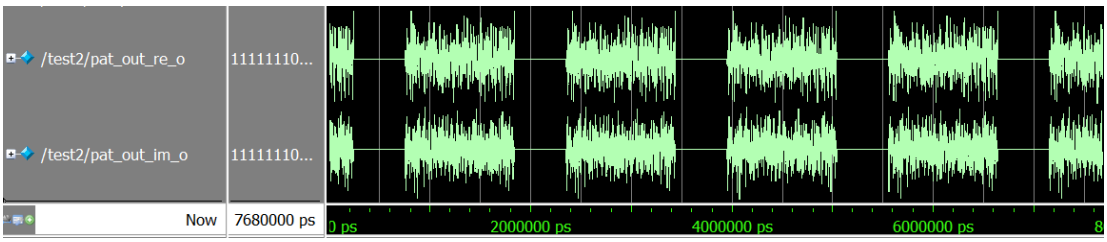

Figure 14. Complex time-domain OFDM output captured by Reveal Analyzer

The key observations from the hardware testing results are:

- The single tone signals are of the expected sinusoidal shape.
- The OFDM signals are of the expected burst pattern.
- Note that each sample was translated into a 1ns step in Modelsim.

Analysis and Interpretation of These Results

The frequency spectrum and PSD of the gate-level simulation and hardware testing results were plotted in MATLAB for further analysis.

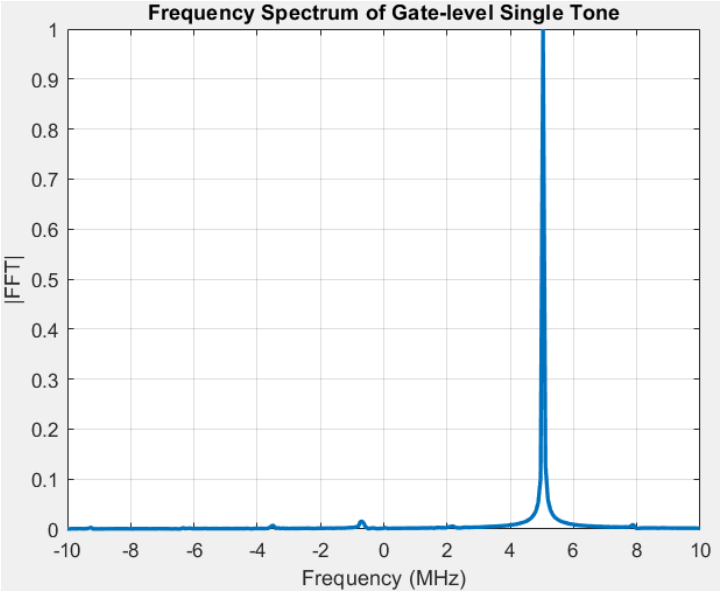

Figure 15. Frequency spectrum plot of complex single tone 5 MHz sinusoidal output from gate-level simulation

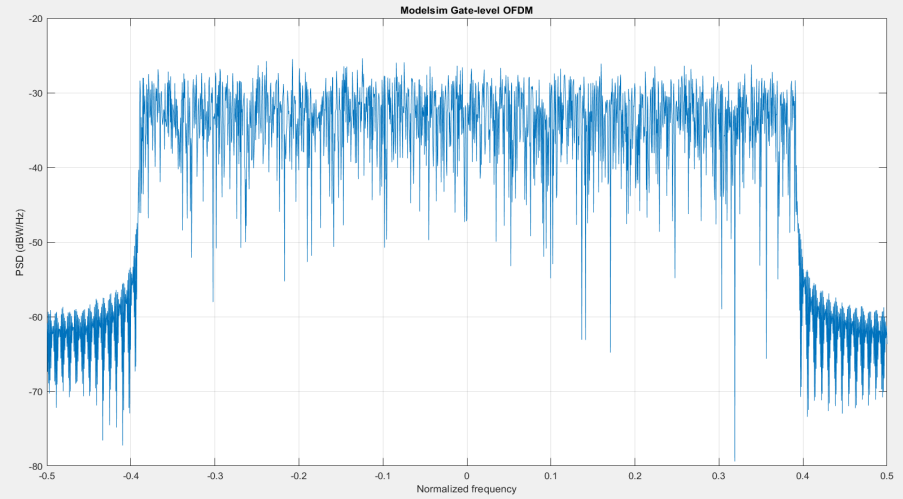

Figure 16. PSD plot of OFDM output from gate-level simulation

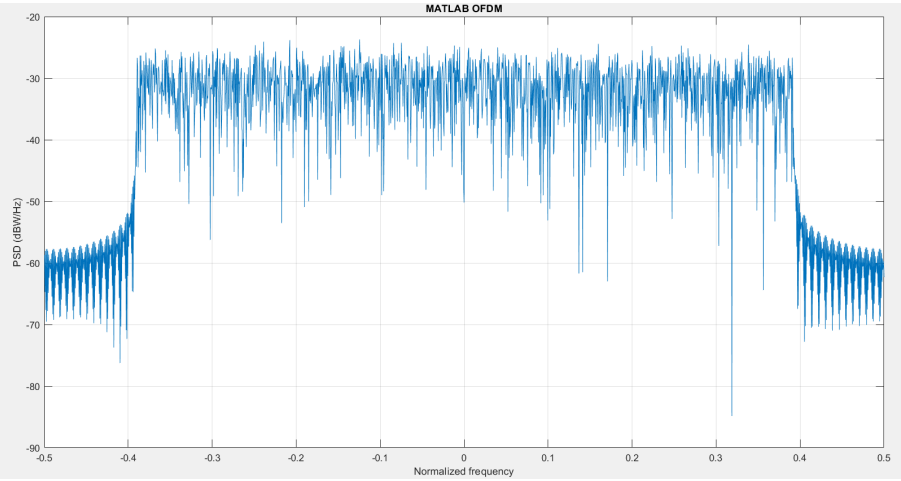

Figure 17. PSD plot of OFDM output from MATLAB model

The key observations on the plots from gate-level simulation are:

- The frequency spectrum plot of the single tone simulated values shows the expected frequency peak at 5 MHz.
- The PSD plots of OFDM output are similar between MATLAB model and gate-level simulation.

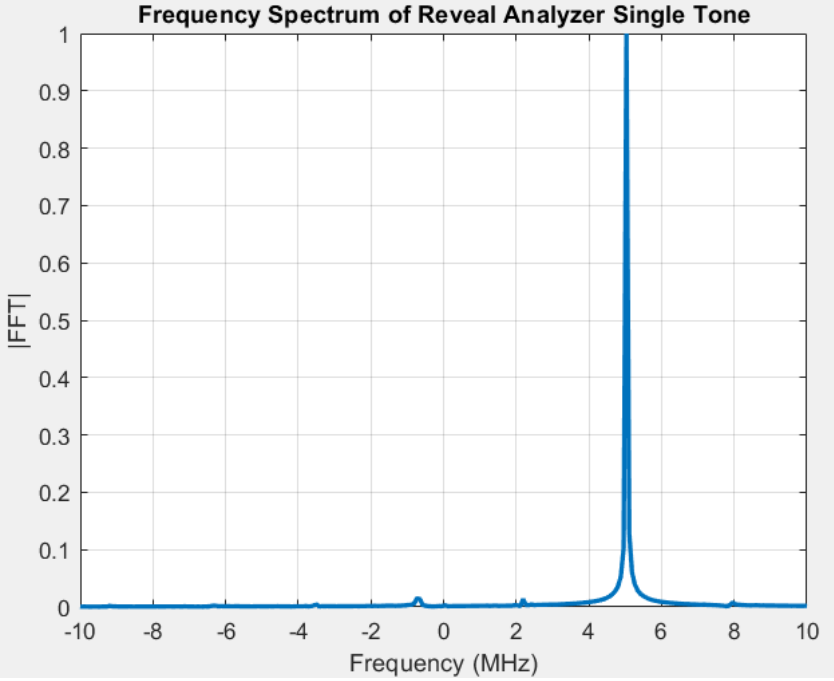

Figure 18. Frequency spectrum plot of complex single tone 5 MHz sinusoidal output from Reveal Analyzer

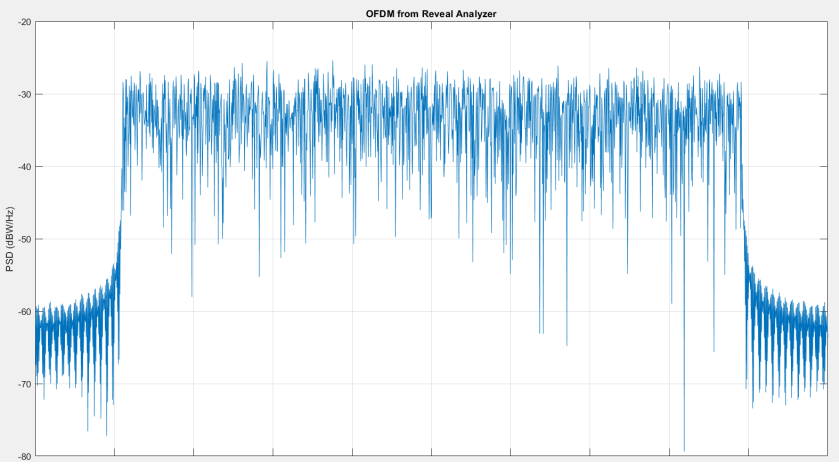

Figure 19. PSD plot of OFDM output from Reveal Analyzer

The key observations from the plots with Reveal Analyzer are:

- The frequency spectrum plot of the single tone from Reveal Analyzer shows the expected frequency peak at 5MHz.
- The PSD plots of the OFDM output are similar among MATLAB model, gate-level simulation, and Reveal Analyzer.

Conclusion

Summary of Evaluation and Findings

This paper presented the design and implementation of a OFDM and Single Tone modulator through the integration of RTLs generated by HDL Coder and hand-coded RTLs. The results obtained from the RTL and gate-level simulations, as well as hardware testing on the CertusPro-NX development kit, demonstrated the robustness and reliability of the design. Furthermore, the matching results between RTL simulation and gate-level simulation, as well as the hardware testing results, validate the functionality of the design.

Suggestions for Future Research

Future research could focus on the following areas:

- Integration with JESD204B IP: The modulator could be integrated with JESD204B IP to bring up the link. This would allow for more comprehensive testing and validation of the design.
- Porting to Lattice Avant™ device and adding sinc FIR: The modulator could be ported to Lattice Avant device and a sinc FIR could be added to improve the spectral efficiency of the OFDM signal. This would enhance the performance of the design.
- Further verification and BER measurement with external analog chipset and JESD204 integration

References

- CertusPro-NX PCIe Bridge Board web page
- HDL Coder web page
- DSP HDL Toolbox web page

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