



2.5G, 10G, and 25G Ethernet Driver API Reference

Technical Note

FPGA-TN-02375-1.1

June 2025

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Contents	3
Abbreviations in This Document.....	6
1. Introduction	7
1.1. Purpose	7
1.2. Audience	7
1.3. Driver Version	7
1.4. Driver and IP Compatibility	7
2. API Description	8
2.1. xxv_xethernet_init()	8
2.2. xxv_xethernet_start().....	8
2.3. xxv_xethernet_stop()	8
2.4. xxv_xethernet_reset().....	8
2.5. xxv_xethernet_set_mac_options()	9
2.6. xxv_xethernet_clear_mac_options()	9
2.7. xxv_xethernet_set_max_packet_length()	9
2.8. xxv_xethernet_set_mac_address().....	9
2.9. xxv_xethernet_get_mac_address().....	10
2.10. xxv_xethernet_conv_mac_to_crc().....	10
2.11. xxv_xethernet_multicast_bit_modify().....	10
2.12. xxv_xethernet_set_multicast_filter().....	10
2.13. xxv_xethernet_clear_multicast_filter().....	11
2.14. xxv_xethernet_get_rx_vlan_tag()	11
2.15. xxv_xethernet_get_rx_idle().....	11
2.16. xxv_xethernet_get_tx_idle()	11
2.17. xxv_xethernet_set_flow_control().....	12
2.18. xxv_xethernet_set_rx_pause_en()	12
2.19. xxv_xethernet_set_pause_tm()	12
2.20. xxv_xethernet_tx_pause_frm().....	12
2.21. xxv_xethernet_set_ipg_val().....	12
2.22. xxv_xethernet_ipg_stretch_mode()	13
2.23. xxv_xethernet_enable_interrupt().....	13
2.24. xxv_xethernet_disable_interrupt()	13
2.25. xxv_xethernet_clear_interrupt_status()	13
2.26. xxv_xethernet_get_interrupt_status().....	14
2.27. xxv_xethernet_trigger_interrupt().....	14
2.28. xxv_xethernet_get_statistic_counter()	14
2.29. xxv_xethernet_print_statistic_counter()	14
3. Function Call Flow Diagrams.....	15
3.1. xxv_xethernet_init()	15
3.2. xxv_xethernet_start().....	16
3.3. xxv_xethernet_stop()	17
3.4. xxv_xethernet_reset().....	18
3.5. xxv_xethernet_set_mac_options()	19
3.6. xxv_xethernet_clear_mac_options()	20
3.7. xxv_xethernet_set_max_packet_length()	21
3.8. xxv_xethernet_set_mac_address().....	22
3.9. xxv_xethernet_get_mac_address().....	23
3.10. xxv_xethernet_conv_mac_to_crc().....	24
3.11. xxv_xethernet_multicast_bit_modify().....	25
3.12. xxv_xethernet_set_multicast_filter().....	26
3.13. xxv_xethernet_clear_multicast_filter().....	27
3.14. xxv_xethernet_get_rx_vlan_tag()	28

3.15.	xxv_xethernet_get_rx_idle()	28
3.16.	xxv_xethernet_get_tx_idle()	29
3.17.	xxv_xethernet_set_flow_control()	29
3.18.	xxv_xethernet_set_rx_pause_en()	30
3.19.	xxv_xethernet_set_pause_tm()	31
3.20.	xxv_xethernet_tx_pause_frm()	32
3.21.	xxv_xethernet_set_ipg_val()	33
3.22.	xxv_xethernet_set_ipg_stretch_mode()	34
3.23.	xxv_xethernet_enable_interrupt()	34
3.24.	xxv_xethernet_disable_interrupt()	35
3.25.	xxv_xethernet_clear_interrupt_status()	35
3.26.	xxv_xethernet_get_interrupt_status()	36
3.27.	xxv_xethernet_trigger_interrupt()	36
3.28.	xxv_xethernet_get_statistic_counter()	37
3.29.	xxv_xethernet_print_statistic_counter()	38
4.	API Data Structures	39
4.1.	struct xxv_xethernet_config	39
4.2.	struct xxv_xethernet_instance	39
5.	API Macros	40
	References	43
	Technical Support Assistance	44
	Revision History	45

Figures

Figure 3.1.	int xxv_xethernet_init()	15
Figure 3.2.	int xxv_xethernet_start()	16
Figure 3.3.	int xxv_xethernet_stop()	17
Figure 3.4.	int xxv_xethernet_reset()	18
Figure 3.5.	int xxv_xethernet_set_mac_options()	19
Figure 3.6.	int xxv_xethernet_clear_mac_options()	20
Figure 3.7.	int xxv_xethernet_set_max_packet_length()	21
Figure 3.8.	int xxv_xethernet_set_mac_address()	22
Figure 3.9.	int xxv_xethernet_get_mac_address()	23
Figure 3.10.	int xxv_xethernet_conv_mac_to_crc()	24
Figure 3.11.	int xxv_xethernet_multicast_bit_modify()	25
Figure 3.12.	int xxv_xethernet_set_multicast_filter()	26
Figure 3.13.	int xxv_xethernet_clear_multicast_filter()	27
Figure 3.14.	int xxv_xethernet_get_rx_vlan_tag()	28
Figure 3.15.	int xxv_xethernet_get_rx_idle()	28
Figure 3.16.	int xxv_xethernet_get_tx_idle()	29
Figure 3.17.	int xxv_xethernet_set_flow_control()	29
Figure 3.18.	int xxv_xethernet_set_rx_pause_en()	30
Figure 3.19.	int xxv_xethernet_set_pause_tm()	31
Figure 3.20.	int xxv_xethernet_tx_pause_frm()	32
Figure 3.21.	int xxv_xethernet_set_ipg_val()	33
Figure 3.22.	int xxv_xethernet_set_ipg_stretch_mode()	34
Figure 3.23.	int xxv_xethernet_enable_interrupt()	34
Figure 3.24.	int xxv_xethernet_disable_interrupt()	35
Figure 3.25.	int xxv_xethernet_clear_interrupt_status()	35
Figure 3.26.	int xxv_xethernet_get_interrupt_status()	36
Figure 3.27.	int xxv_xethernet_trigger_interrupt()	36
Figure 3.28.	int xxv_xethernet_get_statistic_counter()	37

Figure 3.29. int xxv_xethernet_print_statistic_counter().....38

Tables

Table 1.1. Driver and IP Compatibility7
Table 1.2. Quick Facts on Driver Test Environment.....7
Table 4.1. xxv_xethernet_config Parameters39
Table 4.2. xxv_xethernet_instance Parameters39
Table 5.1. XXV_XETHERNET API Macros Description.....40
Table 5.2. XXV_XETHERNET_HW API Macros Description.....41

Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviations	Definition
AHB	Advance High-Performance Bus
APB	Advanced Peripheral Bus
AXI	Advanced eXtensible Interface
CRC	Cyclic Redundancy Check
IEEE	Institute of Electrical and Electronics Engineers
MAC	Media Access Controller
RX	Receive
TX	Transmit

1. Introduction

The 2.5G, 10G, and 25Gb Ethernet Media Access Controller IP core is a complex core containing all the necessary logic and interfacing and clocking infrastructures to integrate an external industry-standard Ethernet PHY with an internal processor efficiently with minimal overhead.

The 2.5G, 10G, and 25G MAC IP core supports the ability to transmit and receive data between standard interfaces such as APB, AHB-Lite or AXI4-Lite, and an Ethernet network. The main function of the 2.5G, 10G, and 25G Ethernet IP is to ensure that the media access rules specified in the IEEE 802.3-2012 standard are met while transmitting a frame of data over the Ethernet. On the receiving side, the 2.5G, 10G, and 25G MAC extracts different components of a frame and transfers them to higher applications through the AXI4-Stream interface.

For more information about the IP core, refer to the following user guides:

- [2.5G Ethernet MAC + PHY IP User Guide \(FPGA-IPUG-02293\)](#).
- [10G Ethernet MAC + PHY IP User Guide \(FPGA-IPUG-02245\)](#).
- [25G Ethernet MAC + PHY IP User Guide \(FPGA-IPUG-02249\)](#).

1.1. Purpose

The 2.5G, 10G, and 25G MAC and its SDK is a set of application programming interfaces (APIs) that provide access to specific Lattice hardware and software capabilities. This document is a reference guide for developers that provides details of the C language driver APIs and function call flows.

1.2. Audience

The intended audience for this document includes embedded system designers and embedded software developers using CertusPro™-NX (2.5G and 10G) and Lattice Avant™ devices (10G and 25G). This technical guide assumes that you have expertise in embedded systems and FPGA technologies.

1.3. Driver Version

XXV_XETHERNET_CONTROLLER 25.01.00.

1.4. Driver and IP Compatibility

Table 1.1. Driver and IP Compatibility

Driver Version	IP Version
25.01.00	2.5G: 1.0.0 10G: 3.3.0 25G: 2.2.0

Refer to the following release notes for more information on the driver and IP versions:

- [2.5G Ethernet MAC + PHY IP Release Notes \(FPGA-RN-02083\)](#)
- [10G Ethernet MAC + PHY IP Release Notes \(FPGA-RN-02031\)](#)
- [25G Ethernet MAC + PHY IP Release Notes \(FPGA-RN-02034\)](#)

Table 1.2. Quick Facts on Driver Test Environment

Hardware Device	Tool Version
Avant-X Versa Board (LAV-AT-X70ES) – tested with 10G and 25G	Lattice Propel™ Builder 2025.1
	Lattice Propel SDK 2025.1
CertusPro-NX Versa Board (LFPCPX-100-9LFG6721) – tested with 2.5G and 10G	Lattice Radiant™ software 2025.1
	Radiant Programmer 2025.1

2. API Description

This section describes the APIs for the 2.5G, 10G, and 25G Ethernet IP core. Note that this driver supports multiple instances of 2.5G, 10G, and 25G Ips within the system. You must initialize additional copies of the variables `xxv_xethernet_instance` and `xxv_xethernet_config` for each instance.

2.1. `xxv_xethernet_init()`

This API is used to initialize the base address of the 2.5G, 10G, or 25G Ethernet IP base address and pass the IP capabilities configuration for the driver.

```
int xxv_xethernet_init(xxv_xethernet_instance *this_xxv_xethernet, xxv_xethernet_config *config)
```

In/Out	Parameter	Description	Returns
In	<code>this_xxv_xethernet</code>	A handle that stores information in the <code>xxv_xethernet_instance</code> structure.	0: success 1: failure
In	<code>config</code>	Base address and IP capabilities, which are configured in the Lattice Propel™ Builder software is assigned to the controller.	

2.2. `xxv_xethernet_start()`

This API is used to activate the TX MAC and RX MAC functionalities for the Ethernet IP core.

```
int xxv_xethernet_start(xxv_xethernet_instance *this_xxv_xethernet)
```

In/Out	Parameter	Description	Returns
In	<code>this_xxv_xethernet</code>	A handle that stores information in the <code>xxv_xethernet_instance</code> structure.	0: success 1: failure

2.3. `xxv_xethernet_stop()`

This API is used to deactivate the TX MAC and RX MAC functionalities for the Ethernet IP core.

```
int xxv_xethernet_stop(xxv_xethernet_instance *this_xxv_xethernet)
```

In/Out	Parameter	Description	Returns
In	<code>this_xxv_xethernet</code>	A handle that stores information in the <code>xxv_xethernet_instance</code> structure.	0: success 1: failure

2.4. `xxv_xethernet_reset()`

This API is used to deactivate the TX MAC and RX MAC of the Ethernet IP core and reinitialize the `xxv_xethernet_instance` parameter with new `xxv_xethernet_config`.

```
int xxv_xethernet_reset(xxv_xethernet_instance *this_xxv_xethernet, xxv_xethernet_config *config)
```

In/Out	Parameter	Description	Returns
In	<code>this_xxv_xethernet</code>	A handle that stores information in the <code>xxv_xethernet_instance</code> structure.	0: success 1: failure
In	<code>config</code>	Base address and IP capabilities, which are configured in	

In/Out	Parameter	Description	Returns
		the Propel Builder software are assigned to the controller.	

2.5. xxv_xethernet_set_mac_options()

This API is used to enable the TX and RX functionalities of the Ethernet IP control option and the mac_cfg_options.

```
int xxv_xethernet_set_mac_options(xxv_xethernet_instance *this_xxv_xethernet, unsigned int options)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
In	options	TX control options and RX control options.	

2.6. xxv_xethernet_clear_mac_options()

This API is used to disable the TX and RX functionalities of the Ethernet IP control option and the mac_cfg_options.

```
int xxv_xethernet_clear_mac_options(xxv_xethernet_instance *this_xxv_xethernet, unsigned int options)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
In	options	TX control options and RX control options.	

2.7. xxv_xethernet_set_max_packet_length()

This API is used to set the max packet length for statistic counter TX_STAT_LNG_PKT purpose.

```
int xxv_xethernet_set_max_packet_length(xxv_xethernet_instance *this_xxv_xethernet, unsigned int max_packet_length)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
In	max_packet_length	Represents a value used for maximum packet length.	

2.8. xxv_xethernet_set_mac_address()

This API is used to set the MAC address of the Ethernet IP core.

```
int xxv_xethernet_set_mac_address(xxv_xethernet_instance *this_xxv_xethernet, char *mac_address)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
In	mac_address	MAC address in char[6] format. For example: if the MAC address is AC-DE-48-00-00-80, arrange it in char mac_address = {AC, DE, 48, 00, 00, 80};	

2.9. xxv_xethernet_get_mac_address()

This API is used to get the MAC address of the Ethernet IP core.

```
int xxv_xethernet_get_mac_address(xxv_xethernet_instance *this_xxv_xethernet, char *mac_address)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
Out	mac_address	MAC address in char[6] format. For example: if the obtained mac_address = {AC, DE, 48, 00, 00, 80}, it is equivalent to AC-DE-48-00-00-80.	

2.10. xxv_xethernet_conv_mac_to_crc()

This API is used to calculate cyclic redundancy check (CRC) from the MAC address.

```
int xxv_xethernet_conv_mac_to_crc(char *mac_address)
```

In/Out	Parameter	Description	Returns
In	mac_address	MAC address in char[6] format. For example: if the MAC address is AC-DE-48-00-00-80, arrange it in char mac_address = {AC, DE, 48, 00, 00, 80};	CRC

2.11. xxv_xethernet_multicast_bit_modify()

This API is used to set or clear multicast filter based on CRC value.

```
int xxv_xethernet_multicast_bit_modify(xxv_xethernet_instance *this_xxv_xethernet, unsigned int crc, unsigned char isSet)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
In	crc	Calculated CRC value after calling xxv_xethernet_conv_mac_to_crc.	
In	isSet	To set the multicast table, pass in the value 1. To clear the multicast table, pass in the value 0.	

2.12. xxv_xethernet_set_multicast_filter()

This API is used to set multicast filter based on the MAC address.

```
int xxv_xethernet_set_multicast_filter(xxv_xethernet_instance *this_xxv_xethernet, char *mac_address)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
In	mac_address	MAC address in char[6] format. For example: if the MAC address is AC-DE-48-00-00-80, arrange it in char mac_address = {AC, DE, 48, 00, 00, 80};	

2.13. xxv_xethernet_clear_multicast_filter()

This API is used to clear the multicast filter based on the MAC address.

```
int xxv_xethernet_clear_multicast_filter(xxv_xethernet_instance *this_xxv_xethernet,
char *mac_address)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
In	mac_address	MAC address in char[6] format. For example: if the MAC address is AC-DE-48-00-00-80, arrange it in char mac_address = {AC, DE, 48, 00, 00, 80};	

2.14. xxv_xethernet_get_rx_vlan_tag()

This API is used to get the RX VLAN tag field of the most recent tagged frame that was received.

```
int xxv_xethernet_get_rx_vlan_tag(xxv_xethernet_instance *this_xxv_xethernet, unsigned
int *vlan_tag)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
Out	vlan_tag	VLAN tag ID of the most recent tagged frame.	

2.15. xxv_xethernet_get_rx_idle()

This API is used to get the status of the RX MAC.

```
int xxv_xethernet_get_rx_idle(xxv_xethernet_instance *this_xxv_xethernet, unsigned char
*rx_idle)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
Out	rx_idle	Status of the RX MAC. Active: 0 Inactive: 1	

2.16. xxv_xethernet_get_tx_idle()

This API is used to get the status of the TX MAC.

```
int xxv_xethernet_get_tx_idle(xxv_xethernet_instance *this_xxv_xethernet, unsigned char
*tx_idle)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
Out	tx_idle	Status of the TX MAC. Active: 0 Inactive: 1	

2.17. xxv_xethernet_set_flow_control()

This API is used to enable the flow control functionality of the TX MAC.

```
int xxv_xethernet_set_flow_control(xxv_xethernet_instance *this_xxv_xethernet)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure

2.18. xxv_xethernet_set_rx_pause_en()

This API is used to enable the RX MAC to receive PAUSE frame.

```
int xxv_xethernet_set_rx_pause_en(xxv_xethernet_instance *this_xxv_xethernet)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure

2.19. xxv_xethernet_set_pause_tm()

This API is used to configure the pause time for a flow control packet (sourced by the TX MAC).

```
int xxv_xethernet_set_pause_tm(xxv_xethernet_instance *this_xxv_xethernet, int pause_time)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
In	pause_time	Represents a 16-bits value used for flow control packet.	

2.20. xxv_xethernet_tx_pause_frm()

This API is used to enable TX MAC to transmit a PAUSE frame.

```
int xxv_xethernet_tx_pause_frm(xxv_xethernet_instance *this_xxv_xethernet)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure

2.21. xxv_xethernet_set_ipg_val()

This API is used to configure the IPG value to be used by the TX MAC.

```
int xxv_xethernet_set_ipg_val(xxv_xethernet_instance *this_xxv_xethernet, int ipg_val)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
In	ipg_value	Represents a 5-bit value used for inter-frame gap.	

2.22. xxv_xethernet_ipg_stretch_mode()

This API is used to configure the TX MAC to operate in the IFG stretch mode to match the data rates of OC-192.

```
int xxv_xethernet_set_ipg_stretch_mode(xxv_xethernet_instance *this_xxv_xethernet)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure

2.23. xxv_xethernet_enable_interrupt()

This API is used to enable the MAC interrupt.

Note: This API is not applicable to 2.5G Ethernet IP.

```
int xxv_xethernet_enable_interrupt(xxv_xethernet_instance *this_xxv_xethernet, unsigned int interrupt_mask)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
In	interrupt_mask	Represents the bitmask of interrupts to be enabled.	

2.24. xxv_xethernet_disable_interrupt()

This API is used to disable the MAC interrupt.

Note: This API is not applicable to 2.5G Ethernet IP.

```
int xxv_xethernet_disable_interrupt(xxv_xethernet_instance *this_xxv_xethernet, unsigned int interrupt_mask)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
In	interrupt_mask	Represents the bitmask of interrupts to be disabled.	

2.25. xxv_xethernet_clear_interrupt_status()

This API is used to clear the interrupt status of the MAC.

Note: This API is not applicable to 2.5G Ethernet IP.

```
int xxv_xethernet_clear_interrupt_status(xxv_xethernet_instance *this_xxv_xethernet, unsigned int interrupt_mask)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
In	interrupt_mask	Represents the specified interrupt status bits to be cleared.	

2.26. xxv_xethernet_get_interrupt_status()

This API get the interrupt status of the MAC.

Note: This API is not applicable to 2.5G Ethernet IP.

```
int xxv_xethernet_get_interrupt_status(xxv_xethernet_instance *this_xxv_xethernet,
unsigned int *int_status)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
Out	int_status	Represents the read value from the interrupt status register.	

2.27. xxv_xethernet_trigger_interrupt()

This API triggers the specified interrupt(s) for the MAC.

Note: This API is not applicable to 2.5G Ethernet IP.

```
int xxv_xethernet_trigger_interrupt
(xxv_xethernet_instance *this_xxv_xethernet, unsigned int interrupt_mask)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
In	interrupt_mask	Represents the interrupt(s) to be triggered.	

2.28. xxv_xethernet_get_statistic_counter()

This API is used to read a value from specific statistic counter register.

```
int xxv_xethernet_get_statistic_counters(xxv_xethernet_instance *this_xxv_xethernet,
unsigned int reg_offset, unsigned long long *counter_val)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
In	reg_offset	Statistic counter register offset.	
Out	counter_val	Value of statistic counter.	

2.29. xxv_xethernet_print_statistic_counter()

This API is used to print the name of the statistic counter register string, along with its corresponding register value.

```
int xxv_xethernet_print_statistic_counter(xxv_xethernet_instance *this_xxv_xethernet,
unsigned int reg_offset)
```

In/Out	Parameter	Description	Returns
In	this_xxv_xethernet	A handle that stores information in the xxv_xethernet_instance structure.	0: success 1: failure
In	reg_offset	Statistic counter register offset.	

3. Function Call Flow Diagrams

This section shows the function call flow diagrams for the Ethernet IP core.

3.1. xxv_xethernet_init()

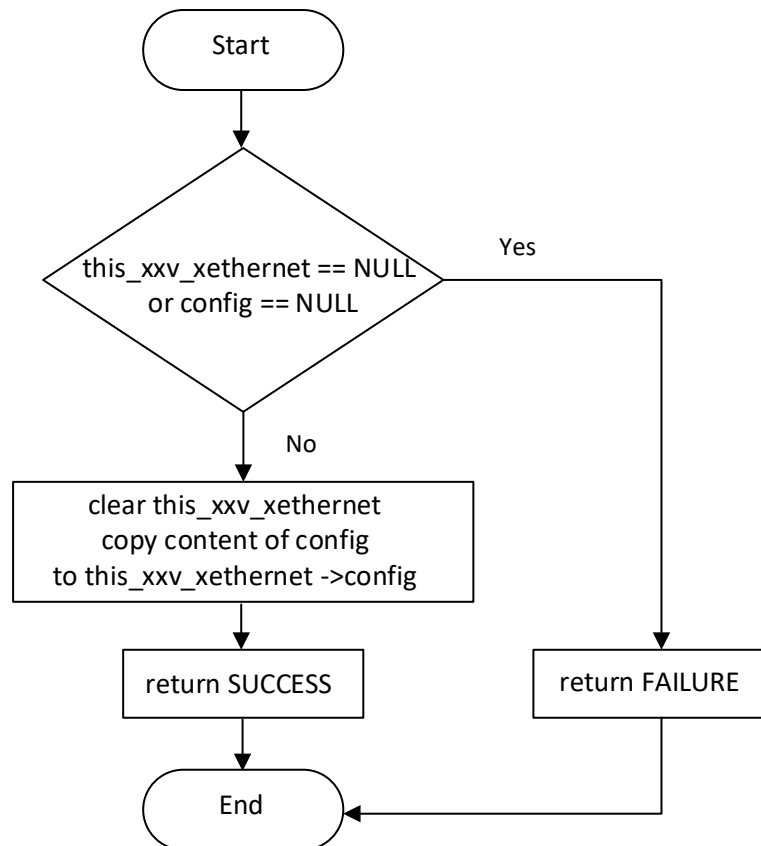


Figure 3.1. int xxv_xethernet_init()

3.2. xxv_xethernet_start()

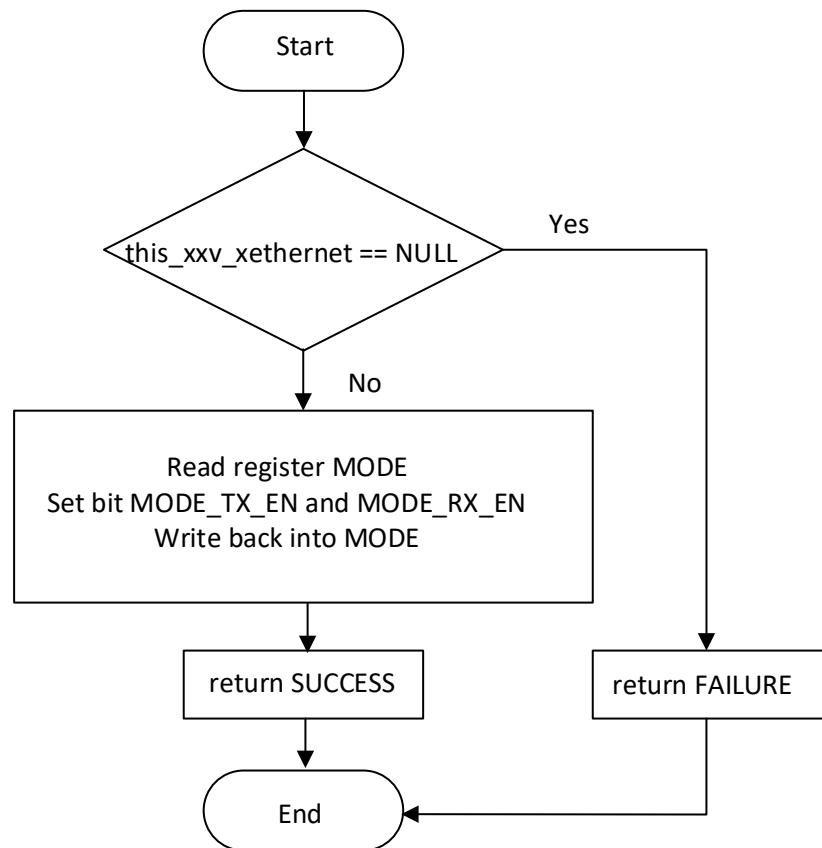


Figure 3.2. int xxv_xethernet_start()

3.3. xxv_xethernet_stop()

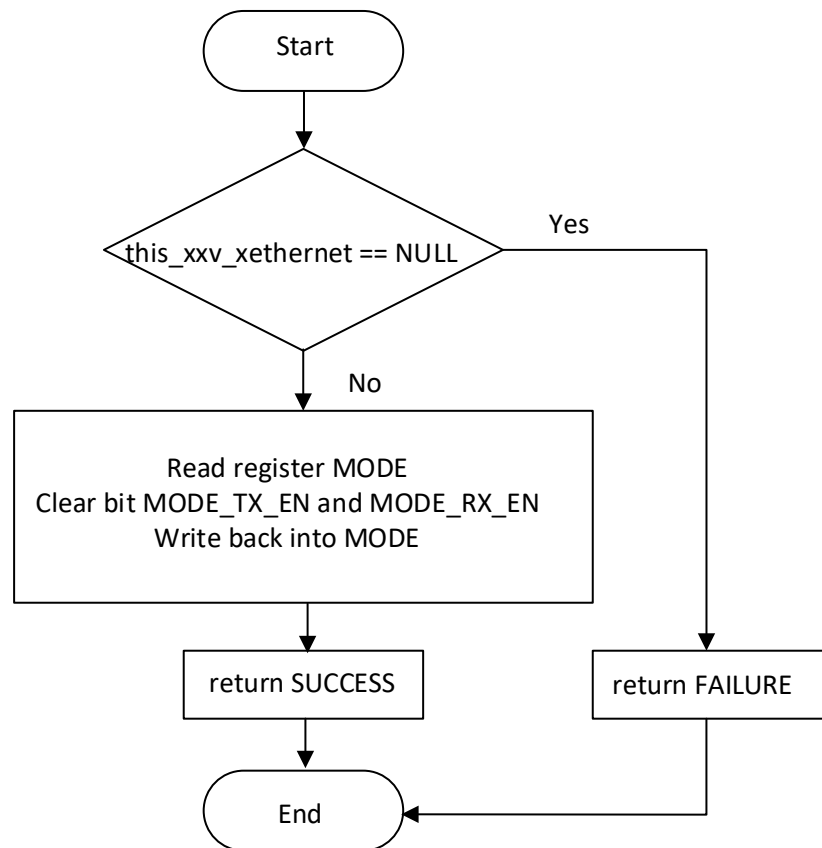


Figure 3.3. int xxv_xethernet_stop()

3.4. xxv_xethernet_reset()

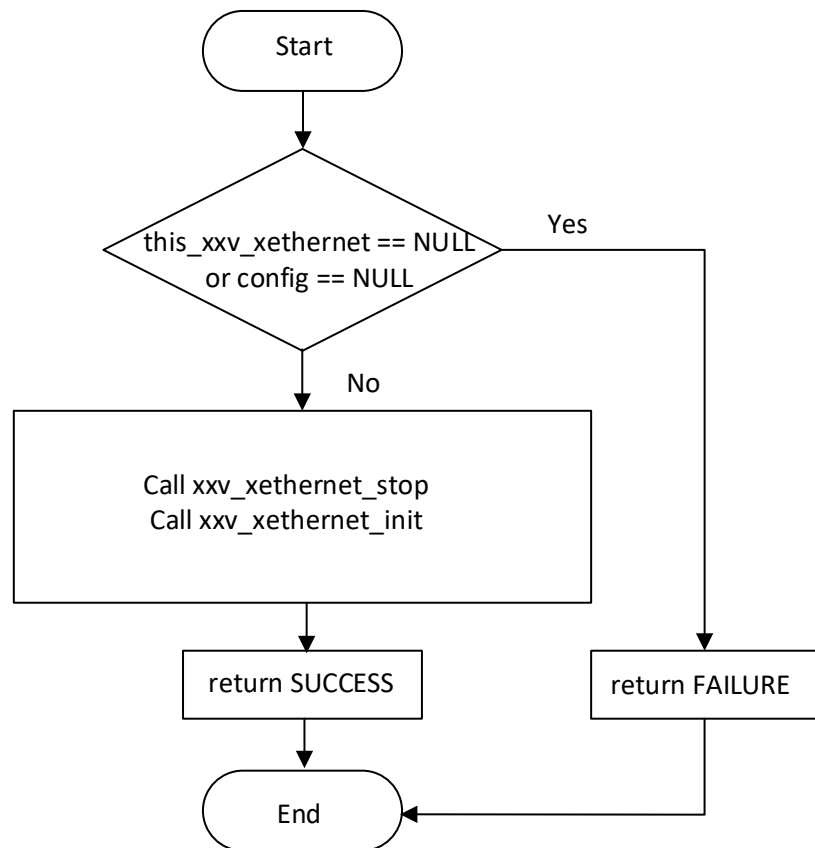


Figure 3.4. int xxv_xethernet_reset()

3.5. xxv_xethernet_set_mac_options()

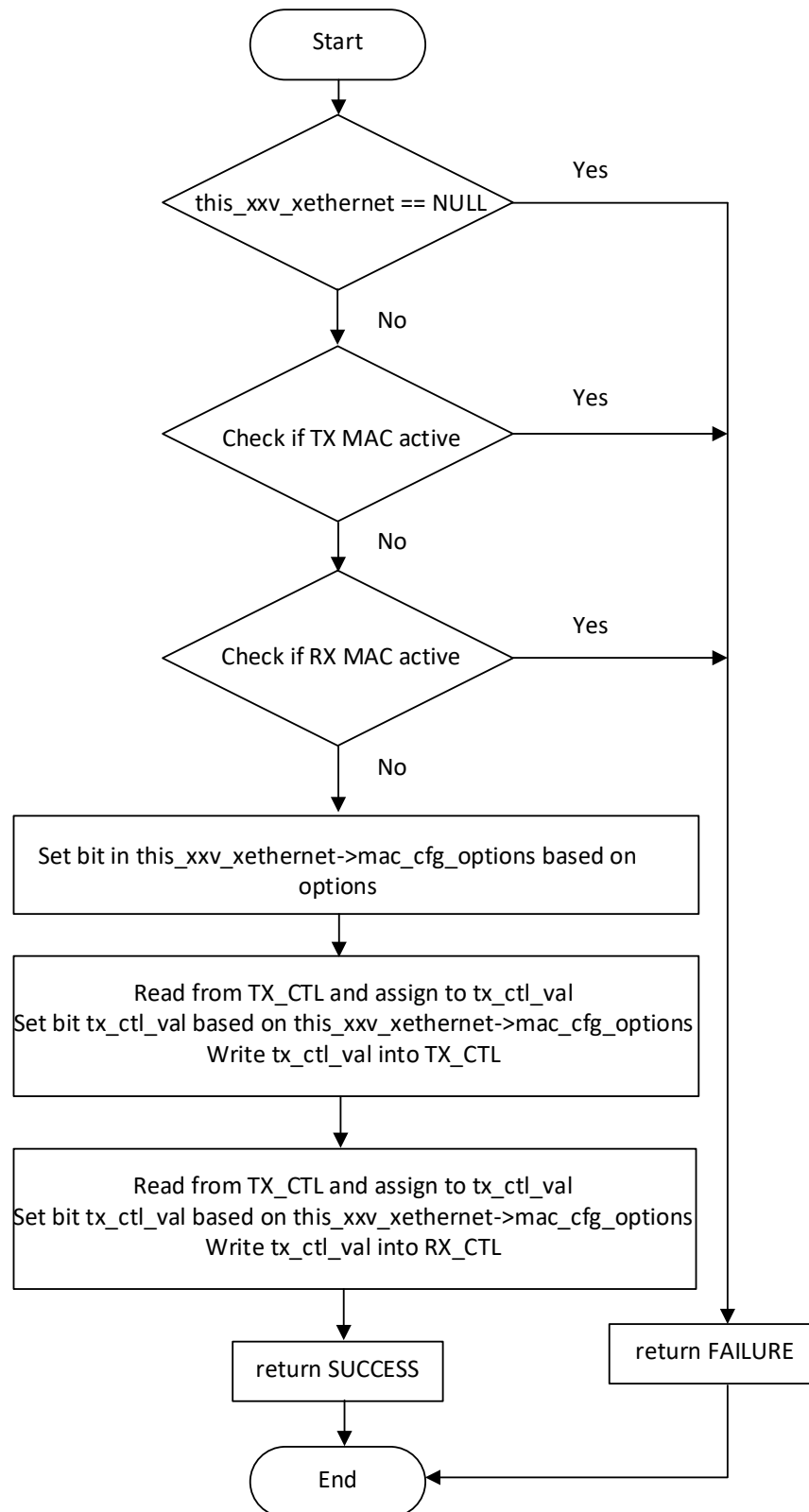


Figure 3.5. int xxv_xethernet_set_mac_options()

3.6. xxv_xethernet_clear_mac_options()

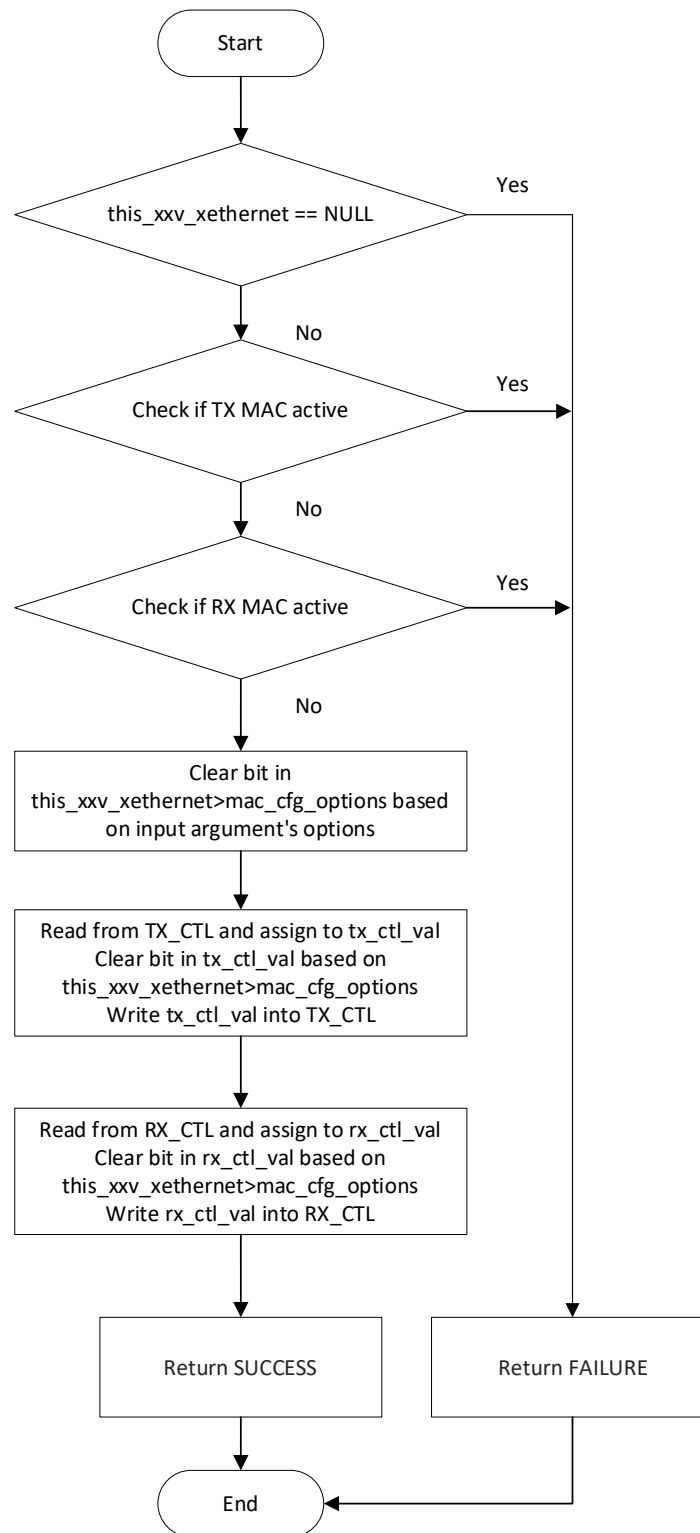


Figure 3.6. int xxv_xethernet_clear_mac_options()

3.7. xxv_xethernet_set_max_packet_length()

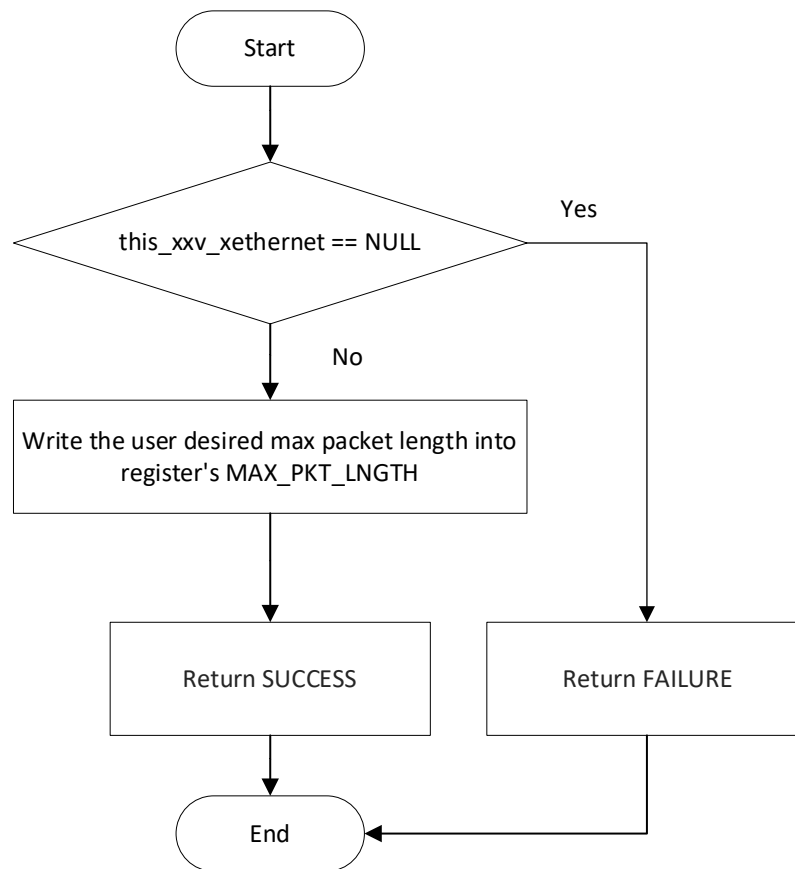


Figure 3.7. int xxv_xethernet_set_max_packet_length()

3.8. xxv_xethernet_set_mac_address()

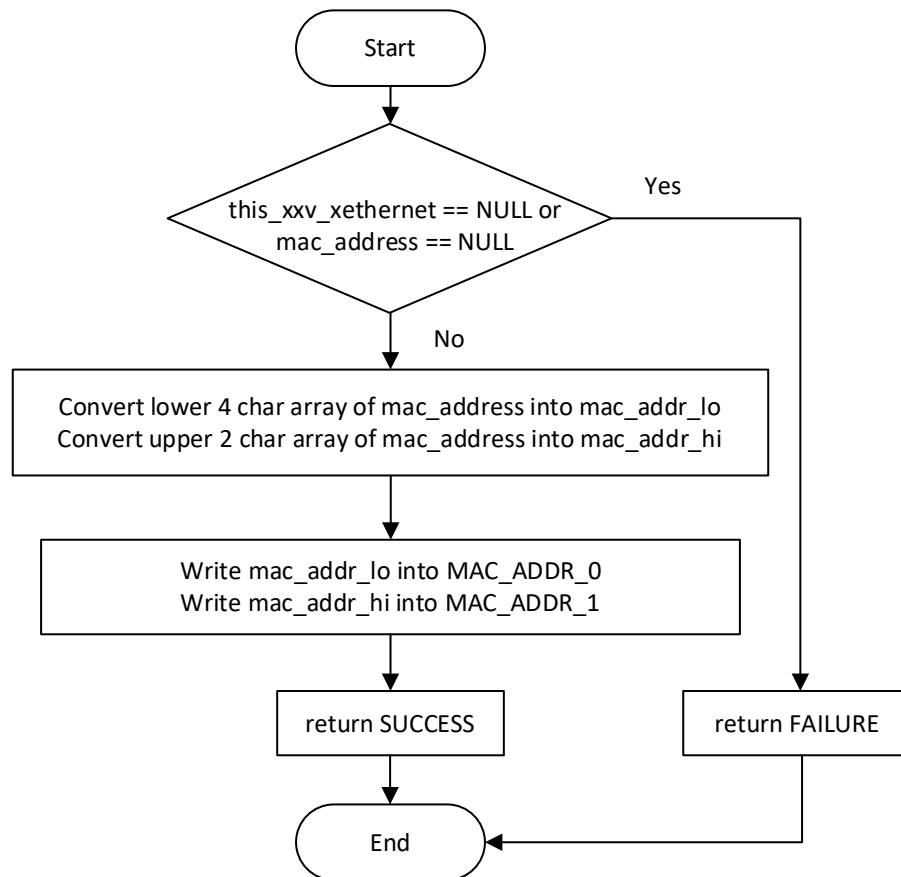


Figure 3.8. int xxv_xethernet_set_mac_address()

3.9. xxv_xethernet_get_mac_address()

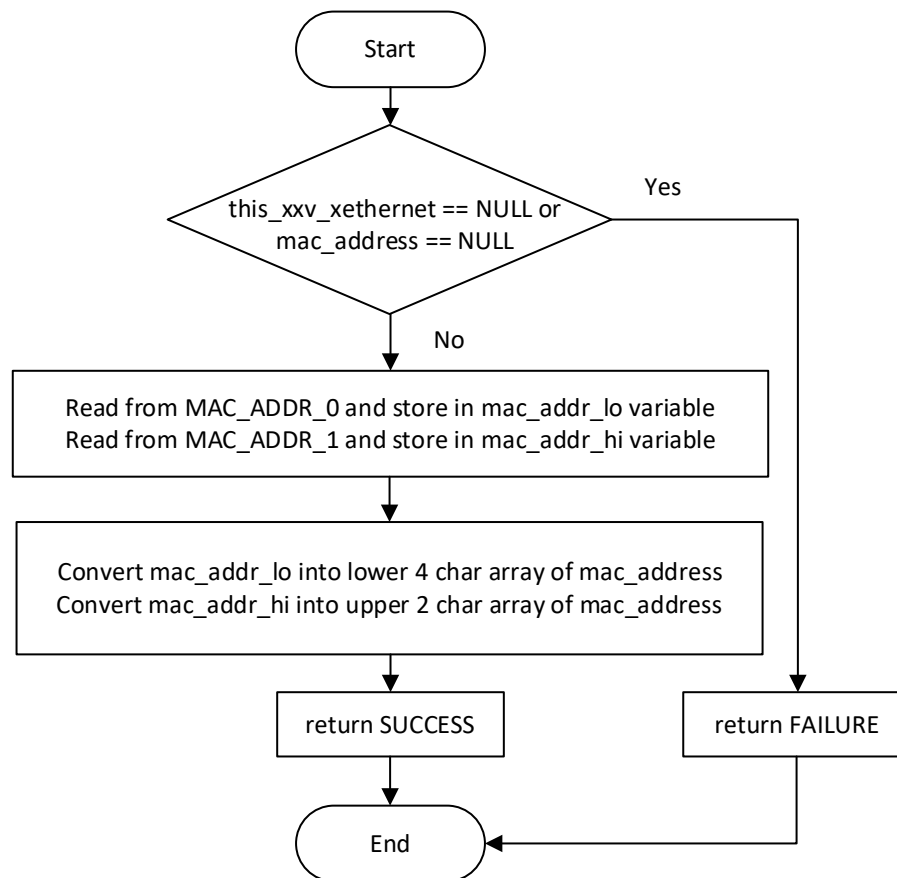


Figure 3.9. int xxv_xethernet_get_mac_address()

3.10. xxv_xethernet_conv_mac_to_crc()

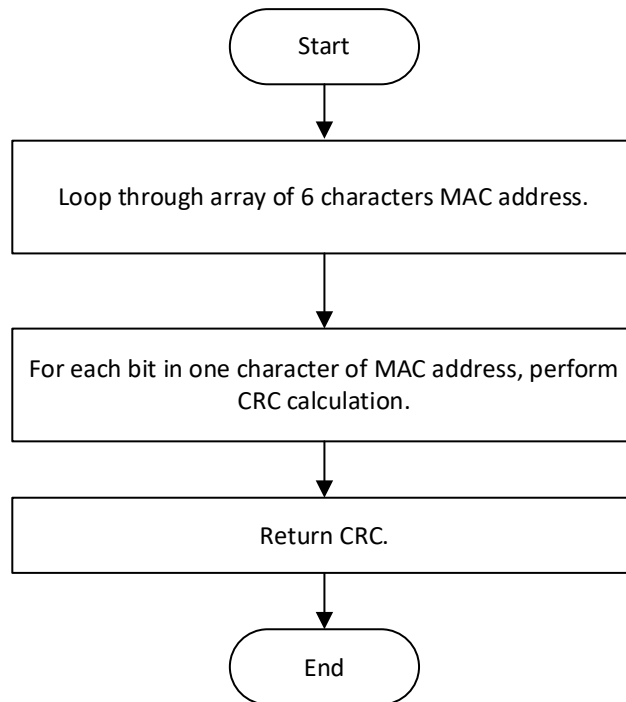


Figure 3.10. int xxv_xethernet_conv_mac_to_crc()

3.11. xxv_xethernet_multicast_bit_modify()

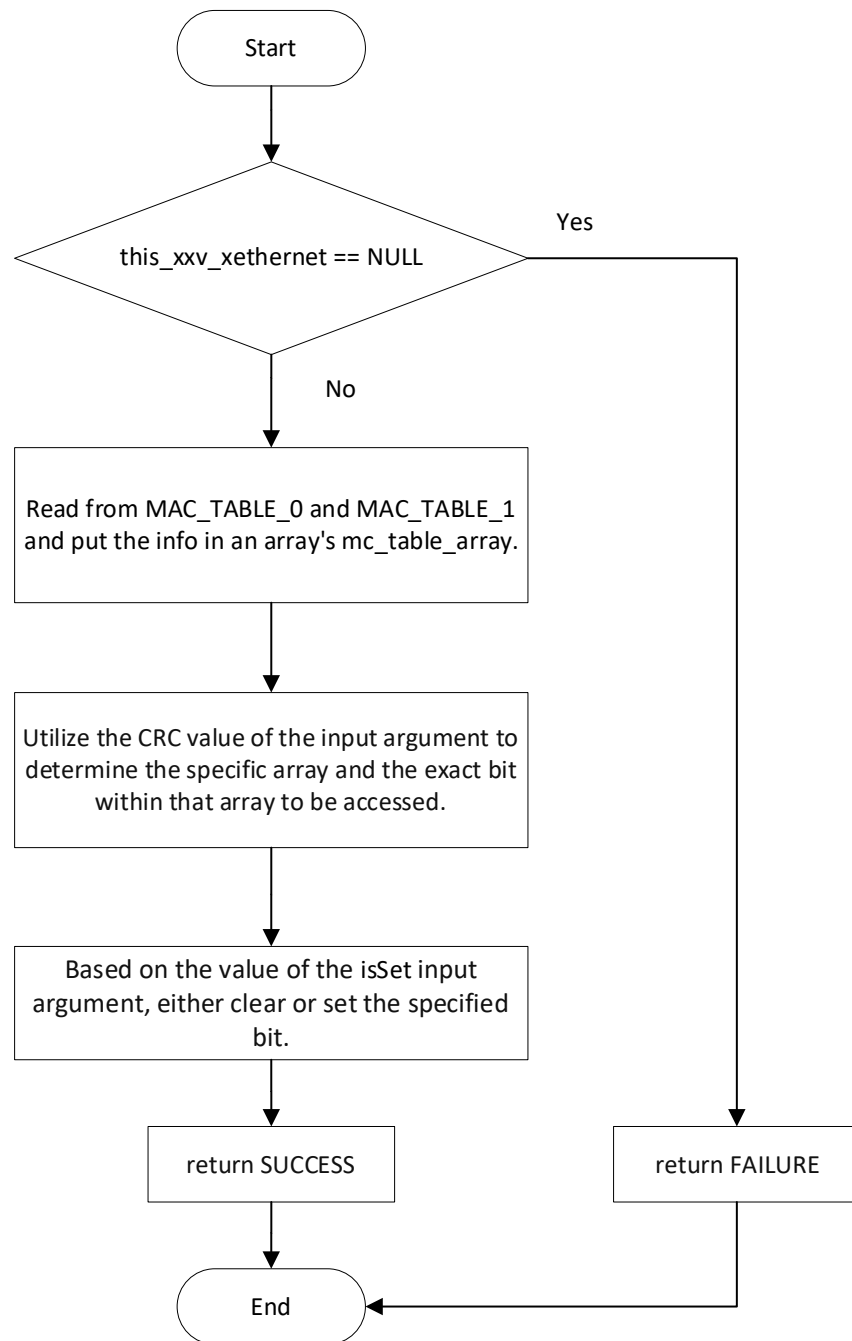


Figure 3.11. `int xxv_xethernet_multicast_bit_modify()`

3.12. xxv_xethernet_set_multicast_filter()

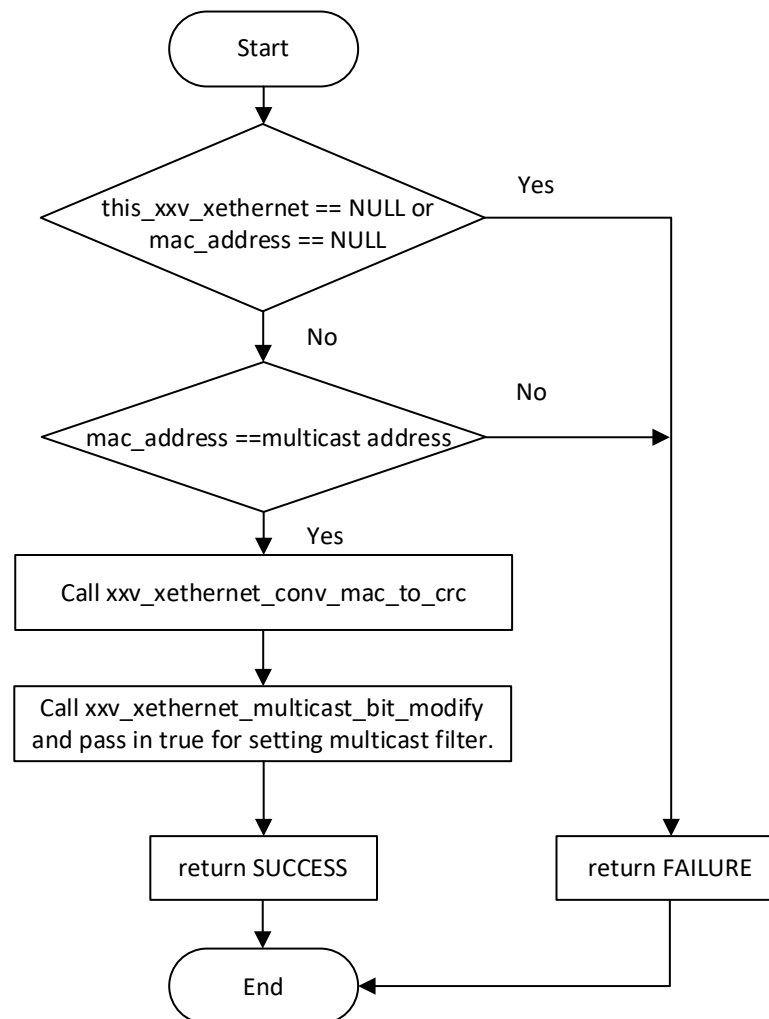


Figure 3.12. `int xxv_xethernet_set_multicast_filter()`

3.13. xxv_xethernet_clear_multicast_filter()

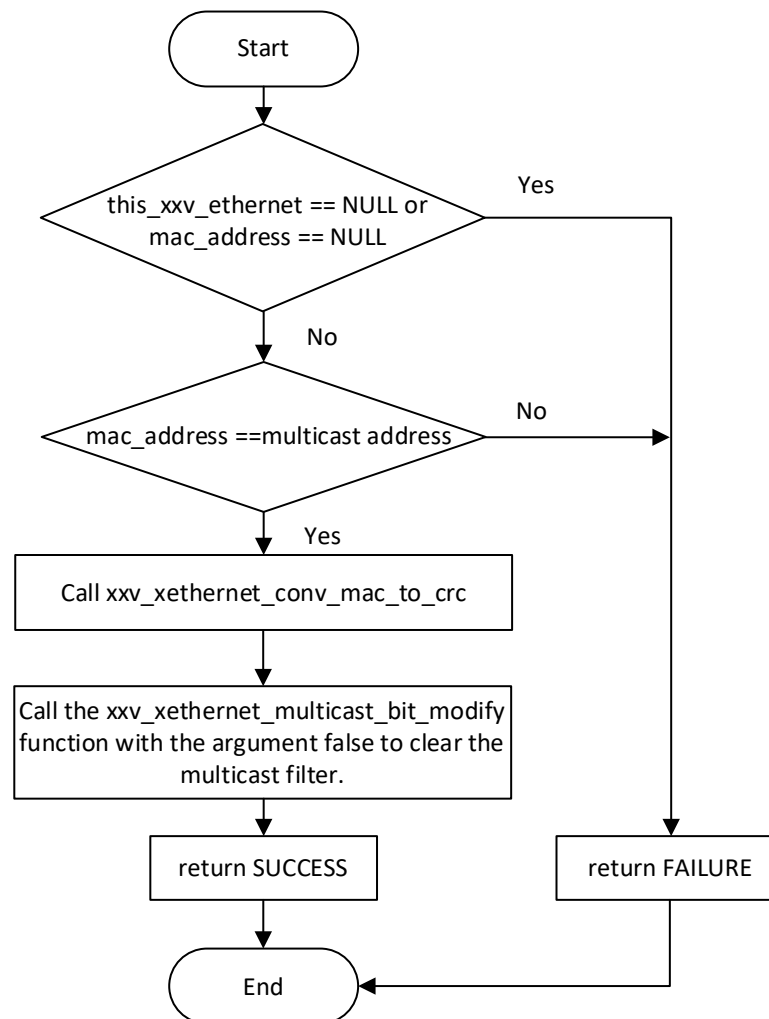


Figure 3.13. int xxv_xethernet_clear_multicast_filter()

3.14. xxv_xethernet_get_rx_vlan_tag()

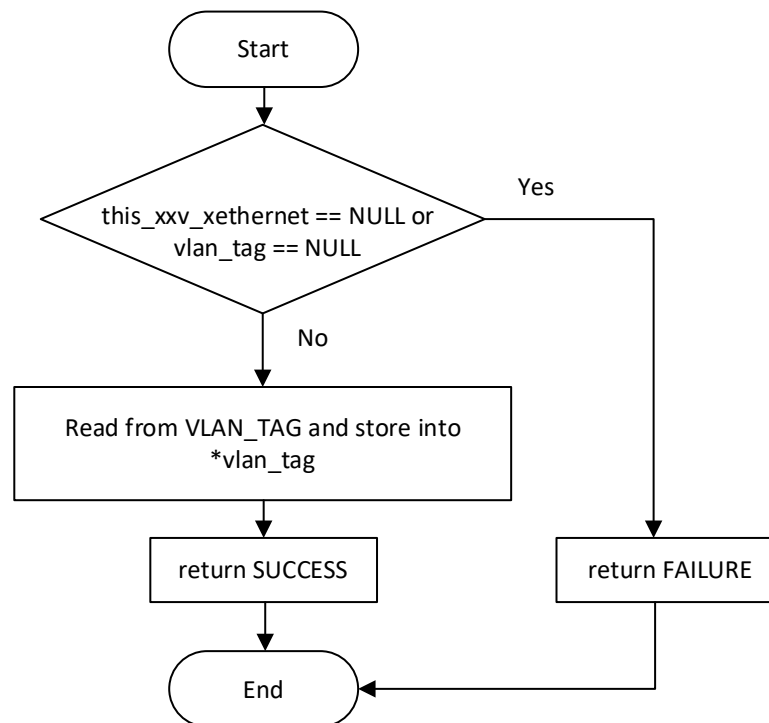


Figure 3.14. int xxv_xethernet_get_rx_vlan_tag()

3.15. xxv_xethernet_get_rx_idle()

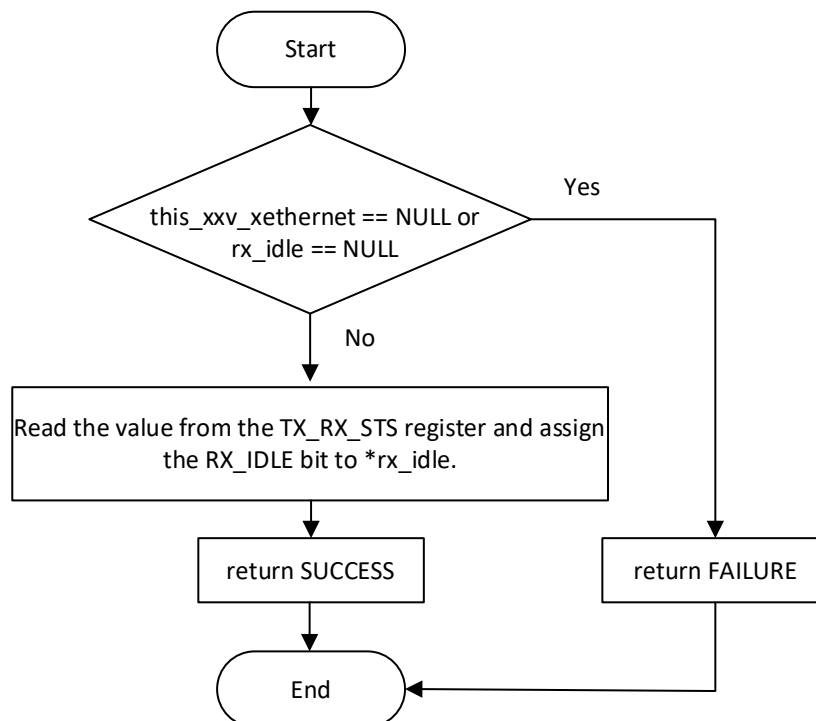


Figure 3.15. int xxv_xethernet_get_rx_idle()

3.16. xxv_xethernet_get_tx_idle()

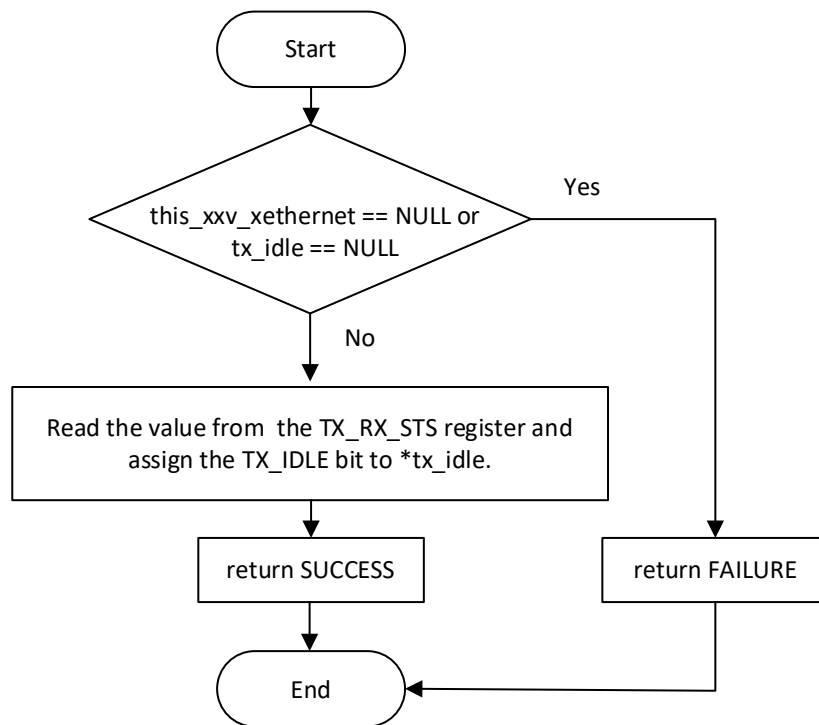


Figure 3.16. `int xxv_xethernet_get_tx_idle()`

3.17. xxv_xethernet_set_flow_control()

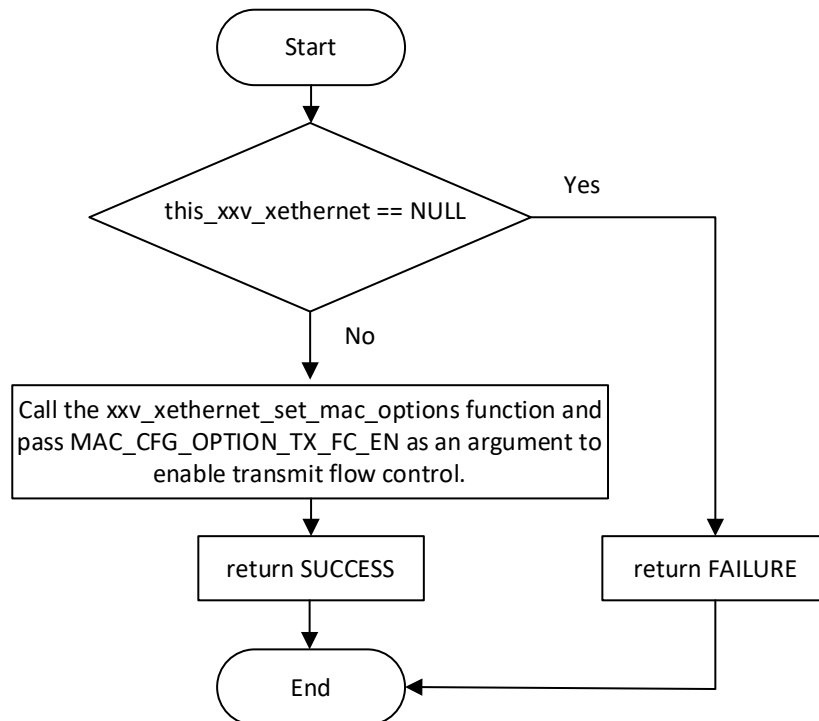


Figure 3.17. `int xxv_xethernet_set_flow_control()`

3.18. xxv_xethernet_set_rx_pause_en()

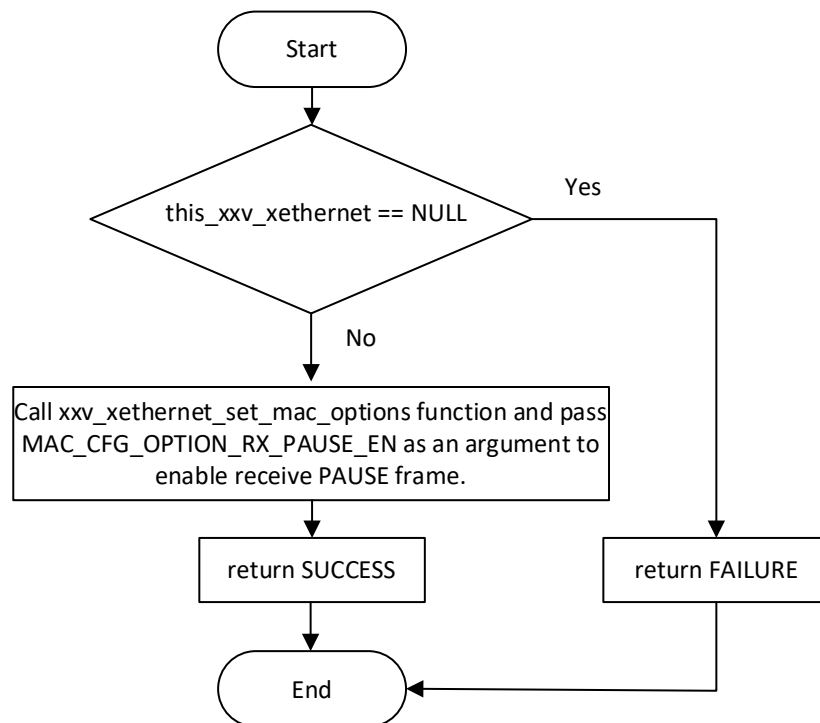


Figure 3.18. `int xxv_xethernet_set_rx_pause_en()`

3.19. xxv_xethernet_set_pause_tm()

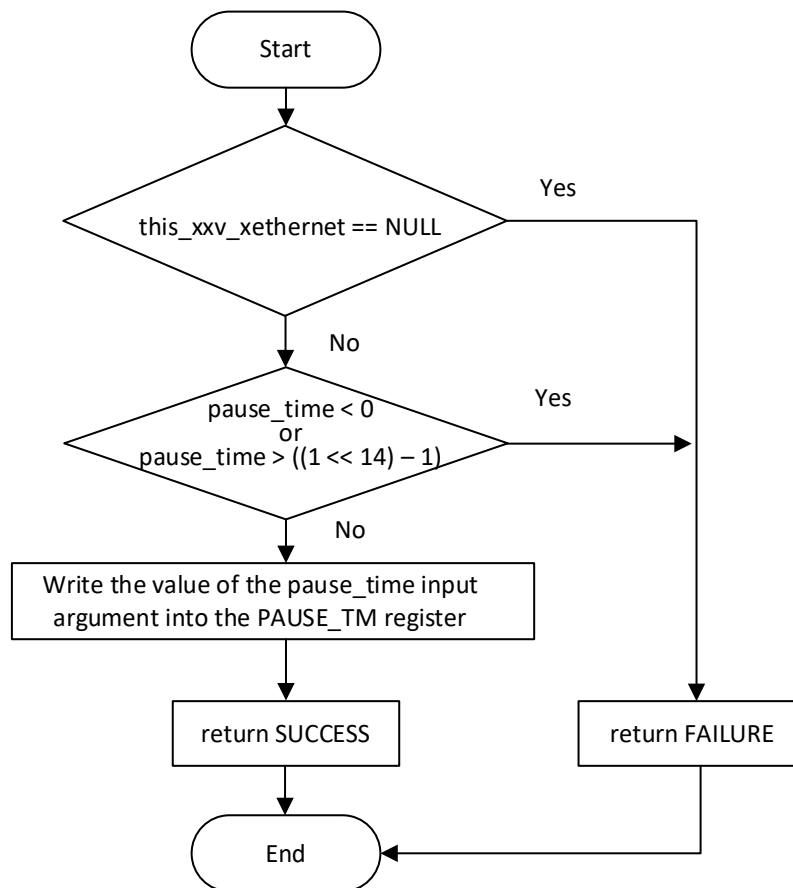


Figure 3.19. `int xxv_xethernet_set_pause_tm()`

3.20. xxv_xethernet_tx_pause_frm()

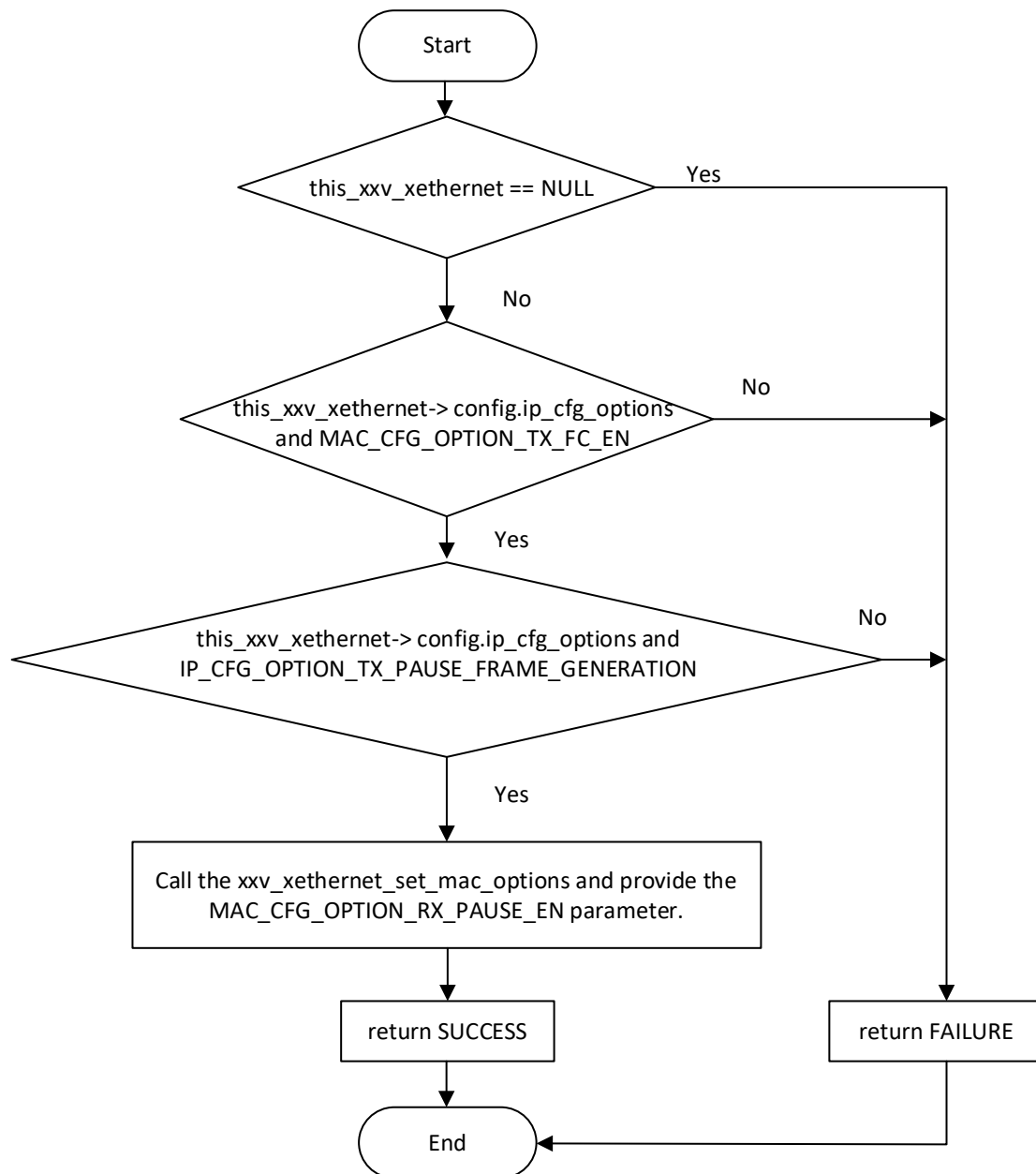


Figure 3.20. int xxv_xethernet_tx_pause_frm()

3.21. xxv_xethernet_set_ipg_val()

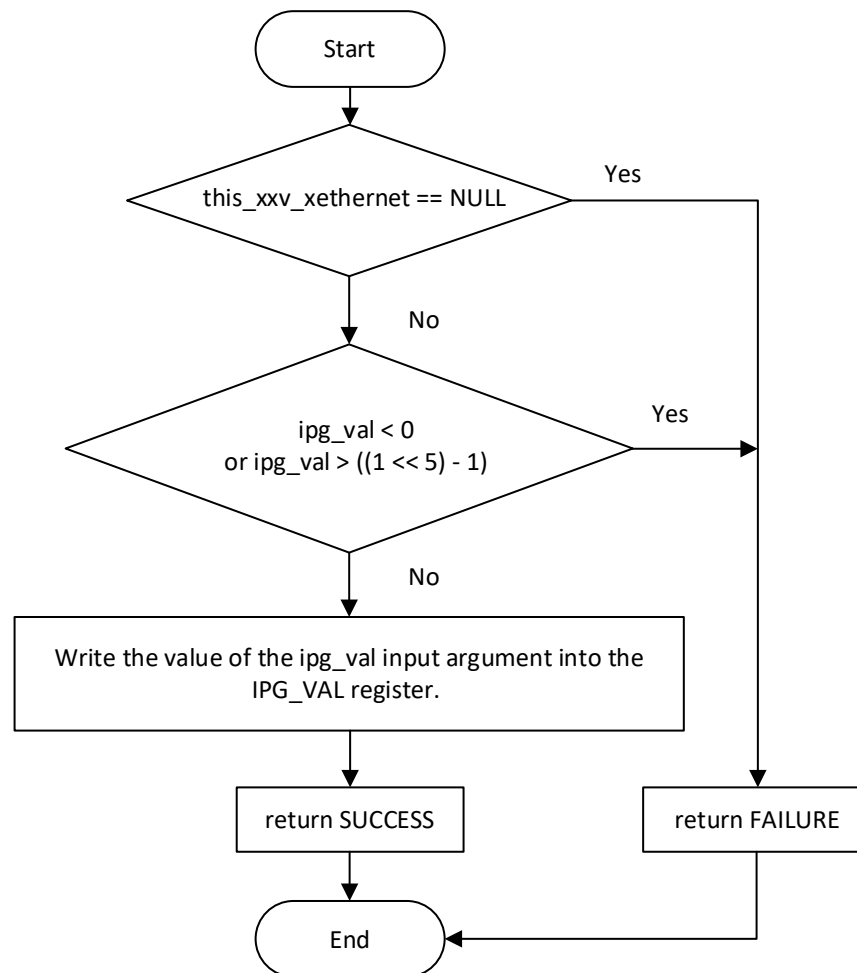


Figure 3.21. `int xxv_xethernet_set_ipg_val()`

3.22. xxv_xethernet_set_ipg_stretch_mode()

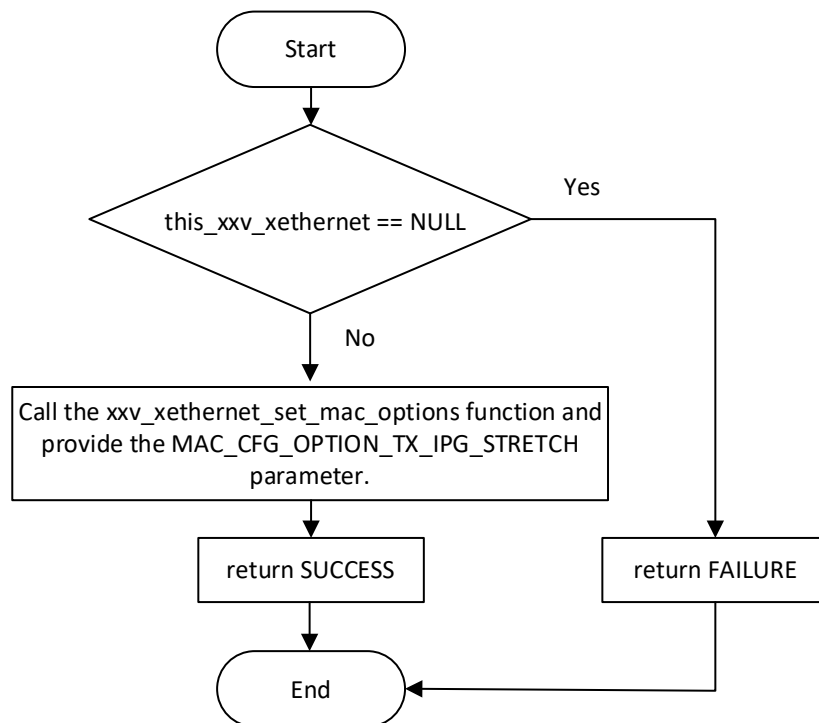


Figure 3.22. `int xxv_xethernet_set_ipg_stretch_mode()`

3.23. xxv_xethernet_enable_interrupt()

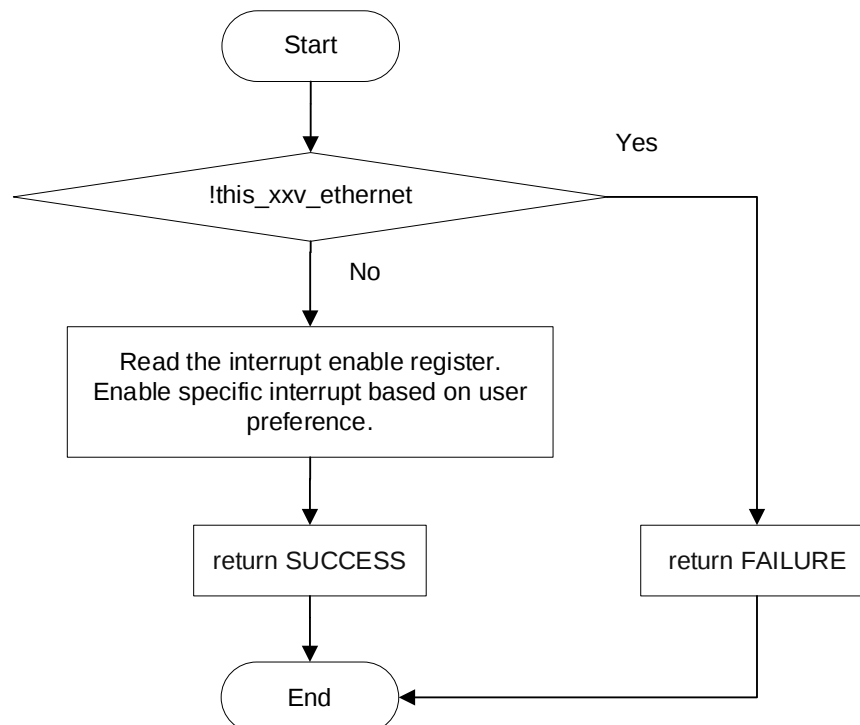


Figure 3.23. `int xxv_xethernet_enable_interrupt()`

3.24. xxv_xethernet_disable_interrupt()

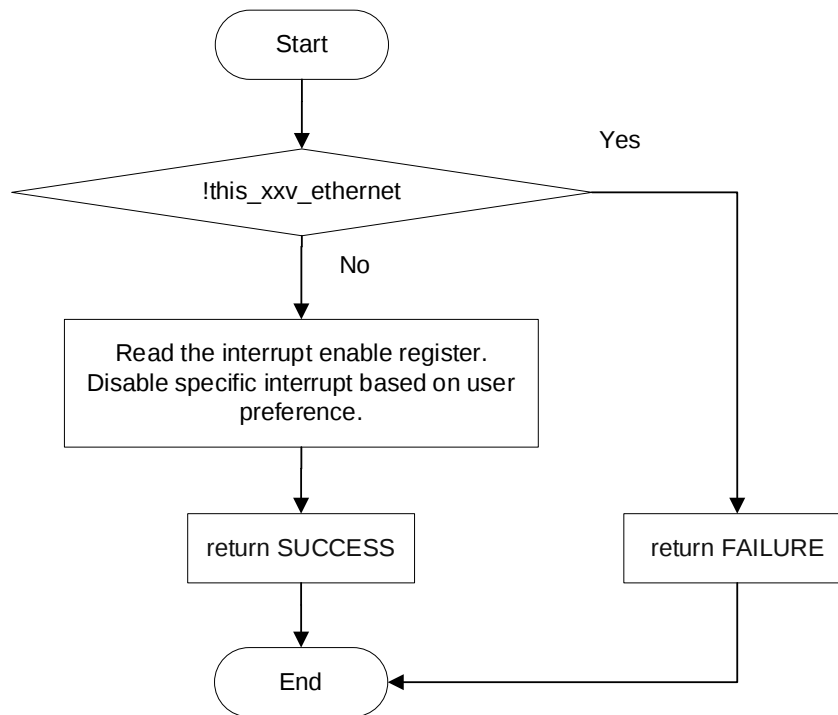


Figure 3.24. int xxv_xethernet_disable_interrupt()

3.25. xxv_xethernet_clear_interrupt_status()

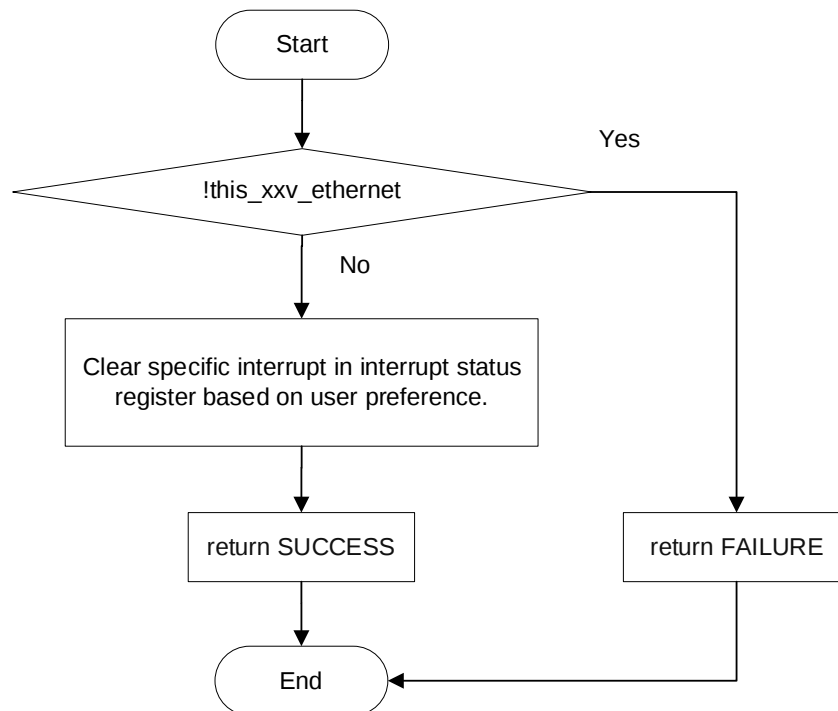


Figure 3.25. int xxv_xethernet_clear_interrupt_status()

3.26. xxv_xethernet_get_interrupt_status()

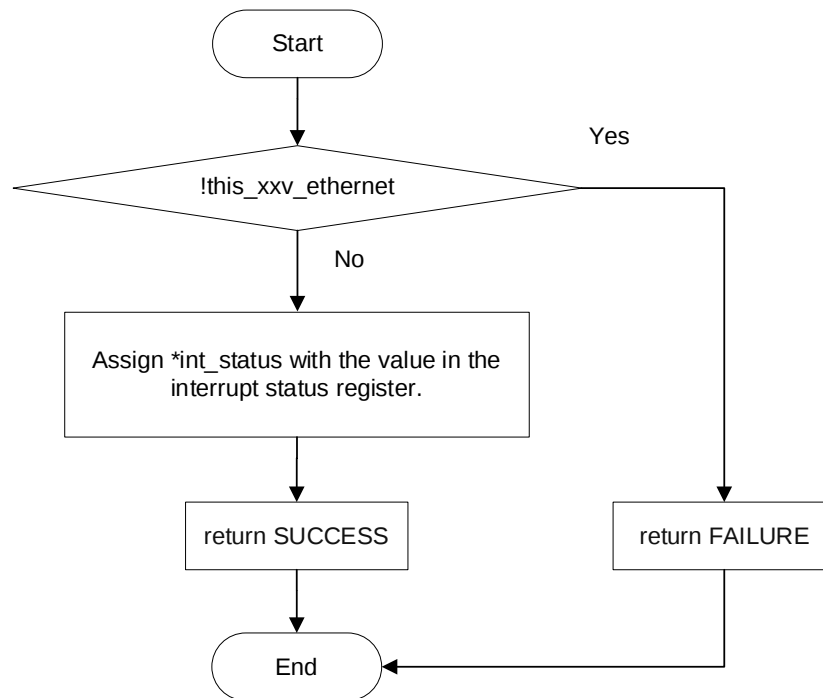


Figure 3.26. int xxv_xethernet_get_interrupt_status()

3.27. xxv_xethernet_trigger_interrupt()

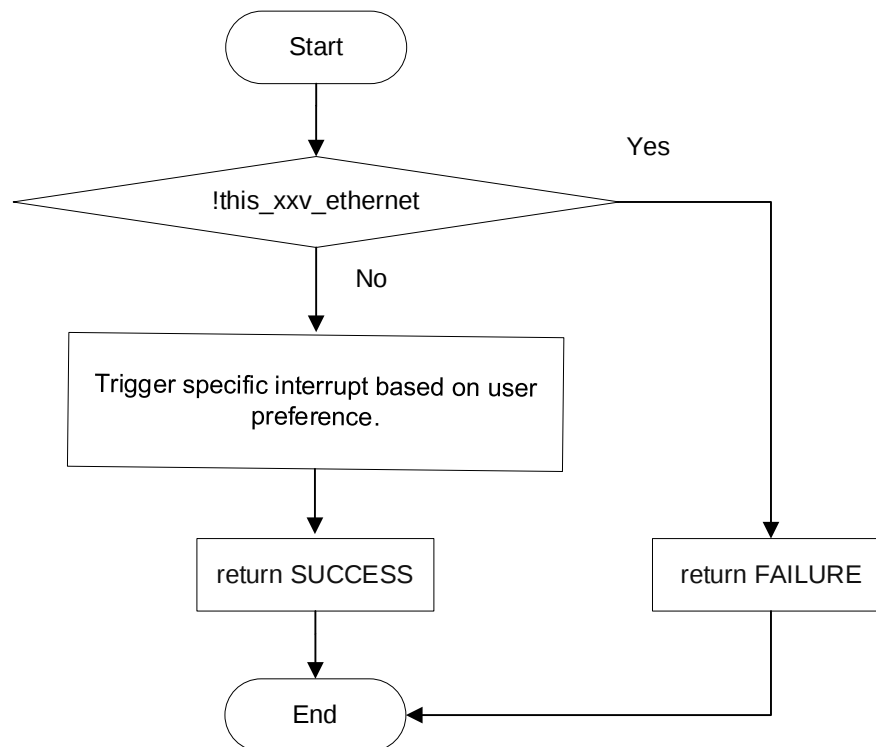


Figure 3.27. int xxv_xethernet_trigger_interrupt()

3.28. xxv_xethernet_get_statistic_counter()

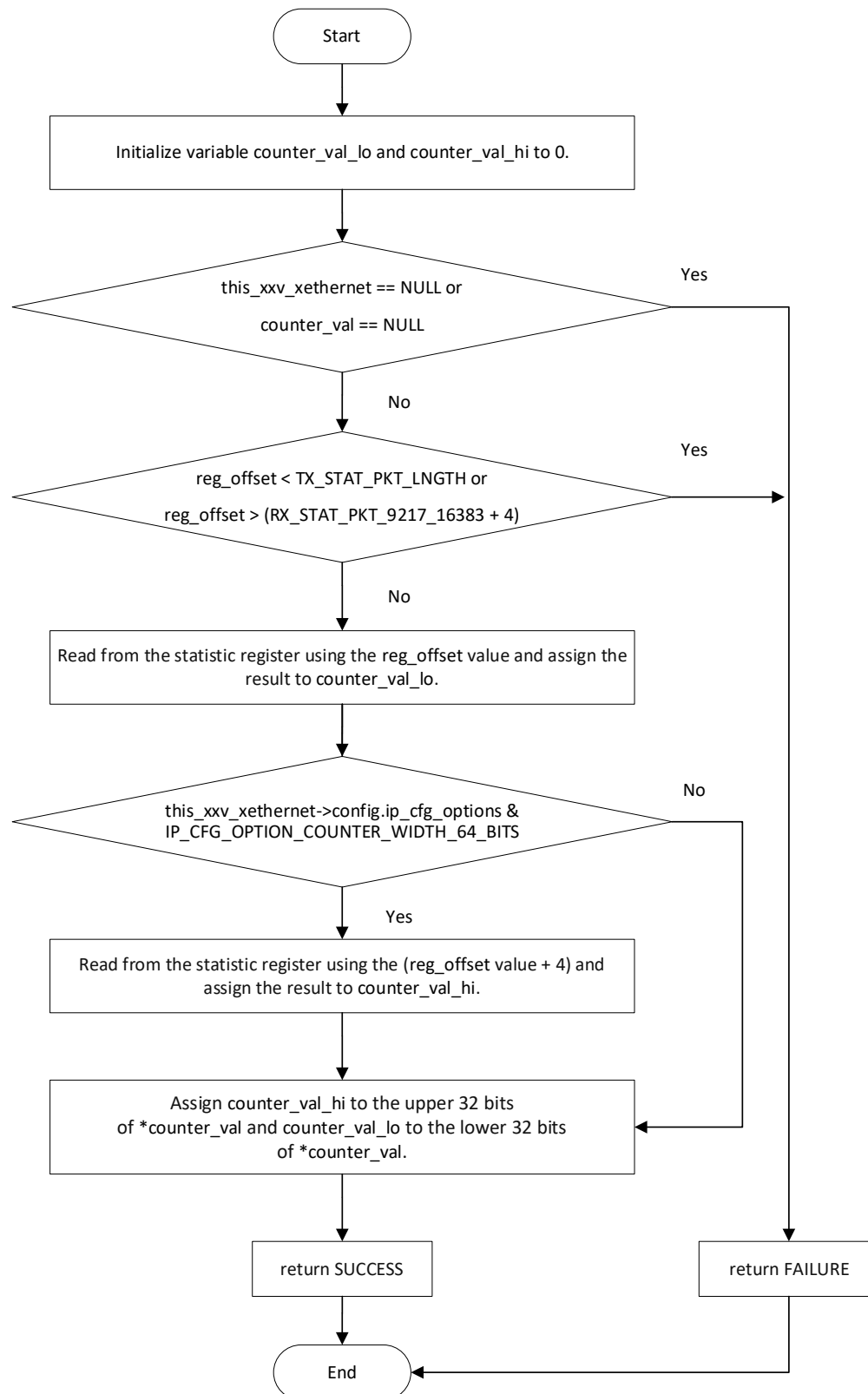


Figure 3.28. int xxv_xethernet_get_statistic_counter()

3.29. xxv_xethernet_print_statistic_counter()

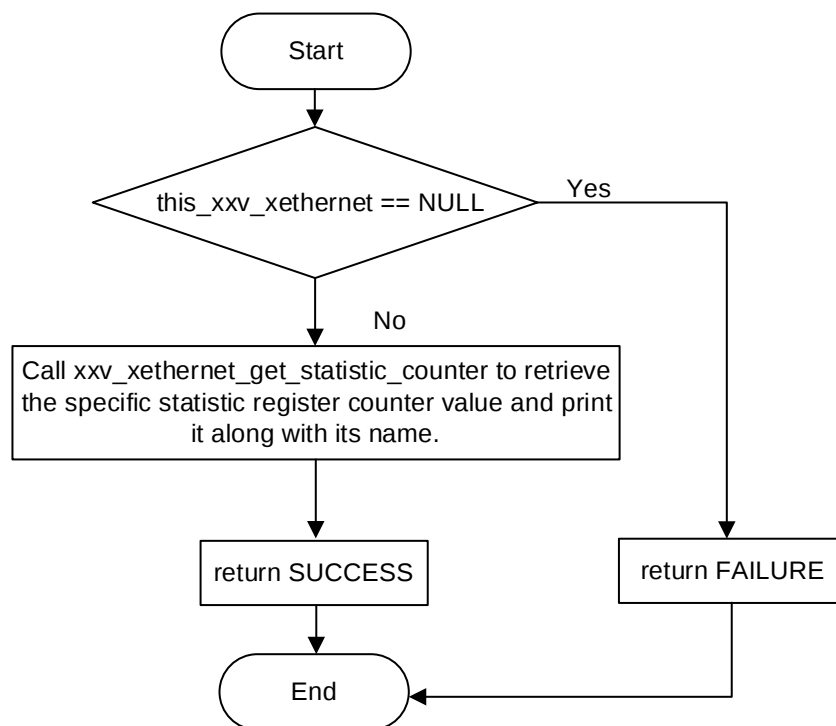


Figure 3.29. int xxv_xethernet_print_statistic_counter()

4. API Data Structures

4.1. struct xxv_xethernet_config

Table 4.1. xxv_xethernet_config Parameters

Data Type	Struct Member	Description
unsigned int	base_address	Base address of the 2.5G, 10G, or 25G Ethernet IP.
unsigned int	ip_cfg_options	IP capabilities configured in the Propel Builder.

4.2. struct xxv_xethernet_instance

Table 4.2. xxv_xethernet_instance Parameters

Data Type	Struct Member	Description
xxv_xethernet_config	config	Configuration information of the 2.5G, 10G, or 25G Ethernet IP.
unsigned char	phy	Physical layer information.
unsigned int	mac_cfg_options	Configuration settings for TX and RX MAC.

5. API Macros

Table 5.1. XXV_XETHERNET API Macros Description

Macro	Description
#define XXV_XETHERNET_CONTROLLER_DRV_VER	2.5G, 10G, and 25G Ethernet driver version.
#define MODE	Transmit MAC control register.
#define TX_CTL	Receive MAC control register.
#define RX_CTL	Maximum packet size register.
#define MAX_PKT_LENGTH	IPG value register.
#define IPG_VAL	MAC address register word 0.
#define MAC_ADDR_0	MAC address register word 1.
#define MAC_ADDR_1	Transmit and receive status register.
#define TX_RX_STS	VLAN tag register.
#define VLAN_TAG	Multicast tables register word 0.
#define MC_TABLE_0	Multicast tables register word 1.
#define MC_TABLE_1	Pause opcode.
#define PAUSE_OPCODE	MAC control register.
#define MAC_CTL	PAUSE time register
#define PAUSE_TM	Transmit MAC control register.
#define INT_STATUS	Interrupt status register.
#define INT_ENABLE	Interrupt enable register.
#define INT_SET	Interrupt set register.
#define MODE_TX_EN	TX MAC enable.
#define MODE_RX_EN	RX MAC enable.
#define TX_PASS_FCS	In-band FCS enable.
#define TX_FC_EN	Flow-control enable.
#define TX_IPG_STRETCH	IFG stretch mode.
#define TX_TRANSMIT_SHORT	Transmit short frames.
#define TX_PASS_PREARM	Transmit custom preamble mode.
#define RX_PRMS	Promiscuous mode.
#define RX_PASS_FCS	In-band FCS passing.
#define RX_PAUSE_EN	Receive PAUSE frames.
#define RX_ALL_MC	Receive Multicast frames.
#define RX_BC	Receive Broadcast frames.
#define RX_SHORT	Receive Short frames.
#define RX_DROP_MAC_CTRL	Drop MAC Control frames.
#define RX_PASS_PREARM	Receive custom preamble mode.
#define RX_IDLE	Receive MAC idle.
#define TX_IDLE	Transmit MAC idle.
#define LOCAL_FAULT_INT	Remote fault symbols received.
#define REMOTE_FAULT_INT	Local fault symbols received.
#define MAC_CFG_OPTION_TX_PASS_PREARM	User option to enable transmit custom preamble mode.
#define MAC_CFG_OPTION_TX_SHORT	User option to enable transmit short frames.
#define MAC_CFG_OPTION_TX_IPG_STRETCH	User option to enable IFG stretch mode.
#define MAC_CFG_OPTION_TX_FC_EN	User option to enable flow-control.
#define MAC_CFG_OPTION_TX_PASS_FCS	User option to enable in-band FCS.
#define MAC_CFG_OPTION_RX_PASS_REARM	User option to enable receive custom preamble mode.
#define MAC_CFG_OPTION_DROP_MAC_CTRL	User option to enable Drop MAC control frames.
#define MAC_CFG_OPTION_RX_SHORT	User option to enable receive Short frames.

Macro	Description
#define MAC_CFG_OPTION_RX_BC	User option to enable receive Broadcast frames.
#define MAC_CFG_OPTION_RX_ALL_MC	User option to enable receive Multicast frames.
#define MAC_CFG_OPTION_RX_PAUSE_EN	User option to enable receive PAUSE frames.
#define MAC_CFG_OPTION_RX_PASS_FCS	User option to enable receive in-band FCS passing.
#define MAC_CFG_OPTION_PRMS	User option to enable promiscuous mode.
#define IP_CFG_OPTION_PHY_XGMII	IP configurations choose PHY XGMII.
#define IP_CFG_OPTION_PHY_8_BITS_GMII	IP configurations choose PHY 8 bits GMII.
#define IP_CFG_OPTION_PHY_16_BITS_GMII	IP configurations choose PHY 16 bits GMII.
#define IP_CFG_OPTION_PHY_MII	IP configurations choose PHY MII.
#define IP_CFG_OPTION_MULTICAST_ADDRESS_FILTERING	IP configurations enable multicast address filtering.
#define IP_CFG_OPTION_STATISTICS_COUNTER_REGISTERS	IP configurations enable statistics counter registers.
#define IP_CFG_OPTION_TX_PAUSE_FRAME_GENERATION	IP configurations enable PAUSE frame generation.
#define IP_CFG_OPTION_COUNTER_WIDTH_32_BITS	IP configurations choose statistic counter 32 bits width.
#define IP_CFG_OPTION_COUNTER_WIDTH_64_BITS	IP configurations choose statistic counter 64 bits width.
#define IP_CFG_OPTION_TX_STATISTICS	IP configurations enable transmit statistics counter.
#define IP_CFG_OPTION_RX_STATISTICS	IP configurations enable receive statistics counter.
#define SUCCESS	1.
#define FAILURE	0.

Table 5.2. XXV_XETHERNET_HW API Macros Description

Macro	Description
#define TX_STAT_PKT_LENGTH	Transmit Packet Length Statistics Counter.
#define TX_STAT_ERR	Transmit TX Error Statistics Counter.
#define TX_STAT_UNDER_RUN	Transmit Underrun Error Statistics Counter.
#define TX_STAT_CRC_ERR	Transmit CRC Error Statistics Counter.
#define TX_STAT_LENGTH_ERR	Transmit Length Error Statistics Counter.
#define TX_STAT_LNG_PKT	Transmit Long packet Statistics Counter.
#define TX_STAT_MULTCST	Transmit Multicast Packet Statistics Counter.
#define TX_STAT_BRDCST	Transmit Broadcast Packet Statistics Counter.
#define TX_STAT_CNT	Transmit Control Packet Statistics Counter.
#define TX_STAT_JMBO	Transmit Jumbo Packet Statistics Counter.
#define TX_STAT_PAUSE	Transmit Pause Packet Statistics Counter.
#define TX_STAT_VLN_TG	Transmit VLAN Tag Statistics Counter.
#define TX_STAT_PKT_OK	Transmit Packet OK Statistics Counter.
#define TX_STAT_PKT_64	Transmit Packet 64 Statistics Counter.
#define TX_STAT_PKT_65_127	Transmit Packet 65 - 127 Statistics Counter.
#define TX_STAT_PKT_128_255	Transmit Packet 128-255 Statistics Counter.
#define TX_STAT_PKT_256_511	Transmit Packet 256-511 Statistics Counter.
#define TX_STAT_PKT_512_1023	Transmit Packet 512-1023 Statistics Counter.
#define TX_STAT_PKT_1024_1518	Transmit Packet 1024-1518 Statistics Counter.
#define TX_STAT_PKT_1518	Transmit Packet 1518 Statistics Counter.
#define TX_STAT_FRM_ERR	Transmit Frame Error Statistics Counter.
#define TX_STAT_PKT_1519_2047	Transmit Packet 1519-2047 Statistics Counter.
#define TX_STAT_PKT_2048_4095	Transmit Packet 2048-4095 Statistics Counter.
#define TX_STAT_PKT_4096_9216	Transmit Packet 4096-9216 Statistics Counter.
#define TX_STAT_PKT_9217_16383	Transmit Packet 9217-16383 Statistics Counter.
#define RX_STAT_PKT_LENGTH	Receive Packet Length Statistics Counter.

Macro	Description
#define RX_STAT_VLN_TG	Receive VLAN Tag Statistics Counter.
#define RX_STAT_PAUSE	Receive Pause Packet Statistics Counter.
#define RX_STAT_FLT	Receive Filtered Packet Statistics Counter.
#define RX_STAT_UNSP_OPCODE	Receive Unsupported Opcode Statistics Counter.
#define RX_STAT_BRDCST	Receive Broadcast Packet Statistics Counter.
#define RX_STAT_MULTCST	Receive Multicast Packet Statistics Counter.
#define RX_STAT_LNGTH_ERR	Receive Length Error Statistics Counter.
#define RX_STAT_LNG_PKT	Receive Long Packet Statistics Counter.
#define RX_STAT_CRC_ERR	Receive CRC Error Statistics Counter.
#define RX_STAT_PKT_DISCARD	Receive Packet Discard Statistics Counter.
#define RX_STAT_PKT_IGNORE	Receive Packet Ignored Statistics Counter.
#define RX_STAT_PKT_FRAGMENTS	Receive Packet Fragments Statistics Counter.
#define RX_STAT_PKT_JABBERS	Receive Packet Jabbers Statistics Counter.
#define RX_STAT_PKT_64	Receive Packet 64 Statistics Counter.
#define RX_STAT_PKT_65_127	Receive Packet 65-127 Statistics Counter.
#define RX_STAT_PKT_128_255	Receive Packet 128-255 Statistics Counter.
#define RX_STAT_PKT_256_511	Receive Packet 256-511 Statistics Counter.
#define RX_STAT_PKT_512_1023	Receive Packet 512-1023 Statistics Counter.
#define RX_STAT_PKT_1024_1518	Receive Packet 1024-1518 Statistics Counter.
#define RX_STAT_PKT_UNDERSIZE	Receive Packet Undersize Statistics Counter.
#define RX_STAT_PKT_UNICAST	Receive Packet Unicast Statistics Counter.
#define RX_STAT_PKT_RCVD	Packets Received Statistics Counter.
#define RX_STAT_PKT_64_GOOD_CRC	Receive Packet 64 with Good CRC Statistics Counter.
#define RX_STAT_PKT_1518_GOOD_CRC	Receive Packet 1518 with Good CRC Statistics Counter.
#define RX_STAT_PKT_1519_2047	Receive Packet 1519-2047 Statistics Counter.
#define RX_STAT_PKT_2048_4095	Receive Packet 2048-4095 Statistics Counter.
#define RX_STAT_PKT_4096_9216	Receive Packet 4096-9216 Statistics Counter.
#define RX_STAT_PKT_9217_16383	Receive Packet 9217-16383 Statistics Counter.
#define xxv_xethernet_reg_name_str	A lookup table returns the string representation of the statistics counter register based on the offset of the statistics counter register.

References

- [2.5G Ethernet MAC + PHY IP User Guide \(FPGA-IPUG-02293\)](#)
- [10G Ethernet MAC + PHY IP User Guide \(FPGA-IPUG-02245\)](#)
- [25G Ethernet MAC + PHY IP User Guide \(FPGA-IPUG-02249\)](#)
- [2.5G Ethernet MAC + PHY IP Release Notes \(FPGA-RN-02083\)](#)
- [10G Ethernet MAC + PHY IP Release Notes \(FPGA-RN-02031\)](#)
- [25G Ethernet MAC + PHY IP Release Notes \(FPGA-RN-02034\)](#)
- [2.5G Ethernet MAC + PHY IP web page](#)
- [10G Ethernet MAC + PHY IP Core web page](#)
- [25G Ethernet MAC + PHY IP web page](#)
- [Lattice Radiant FPGA design software web page](#)
- [Lattice Solutions IP Cores web page](#)
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.1, June 2025

Section	Change Summary
All	Updated the document title to <i>2.5G, 10G, and 25G Ethernet Driver API Reference</i> .
Abbreviations in This Document	Removed XG from the abbreviations table.
Introduction	- Updated this section to include 2.5G and 25G Ethernet IP. - Updated the Driver and IP Compatibility section.
API Description	- Updated this section to include 2.5G and 25G Ethernet IP. - Updated the following sections: xxv_xethernet_init(). xxv_xethernet_start(). xxv_xethernet_stop(). xxv_xethernet_reset(). xxv_xethernet_set_mac_options(). xxv_xethernet_clear_mac_options(). xxv_xethernet_set_mac_address(). xxv_xethernet_get_mac_address(). xxv_xethernet_conv_mac_to_crc(). xxv_xethernet_set_multicast_filter(). xxv_xethernet_clear_multicast_filter(). xxv_xethernet_get_rx_vlan_tag(). xxv_xethernet_get_rx_idle(). xxv_xethernet_get_tx_idle(). xxv_xethernet_set_flow_control(). xxv_xethernet_set_rx_pause_en(). xxv_xethernet_set_pause_tm(). xxv_xethernet_tx_pause_frm(). xxv_xethernet_set_ipg_val(). xxv_xethernet_ipg_stretch_mode(). xxv_xethernet_enable_interrupt(). xxv_xethernet_disable_interrupt(). xxv_xethernet_clear_interrupt_status(). xxv_xethernet_get_interrupt_status(). xxv_xethernet_trigger_interrupt(). xxv_xethernet_get_statistic_counter(). xxv_xethernet_print_statistic_counter(). - Added the following sections: xxv_xethernet_set_max_packet_length(). xxv_xethernet_multicast_bit_modify().
Function Call Flow Diagrams	Updated the content and all the figures in this section.
API Data Structures	Updated the following sections to include 25Gb Ethernet IP: struct xxv_xethernet_config. struct xxv_xethernet_instance.
API Macros	Updated the following tables: Table 5.1. XXV_XETHERNET API Macros Description. Table 5.2. XXV_XETHERNET_HW API Macros Description.
References	Added the following references: 2.5G Ethernet MAC + PHY IP User Guide (FPGA-IPUG-02293). 25G Ethernet MAC + PHY IP User Guide (FPGA-IPUG-02249). 2.5G Ethernet MAC + PHY IP Release Notes (FPGA-RN-02083). 10G Ethernet MAC + PHY IP Release Notes (FPGA-RN-02031).

Section	Change Summary
	• 25G Ethernet MAC + PHY IP Release Notes (FPGA-RN-02034). • 2.5G Ethernet MAC + PHY IP web page. • 25G Ethernet MAC + PHY IP web page.

Revision 1.0, July 2024

Section	Change Summary
All	Initial release.



www.latticesemi.com