MachXO5-NX Family Root-of-Trust Devices Hardware Checklist

Technical Note

FPGA-TN-02371-1.1

October 2025

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This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Figures

Tables

Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AC	Alternating Current
ADC	Analog to Digital Converter
BGA	Ball Grid Array
DC	Direct Current
DLL	Delay-Locked Loop
DRR3	Double Data Rate 3
ESR	Equivalent Series Resistance
FPGA	Field-Programmable Gate Array
HCSL	High-Speed Current Steering Logic
HSUL	High-Speed Unterminated Logic
I/O	Input/Output
JTAG	Joint Test Action Group
LVDS	Low-Voltage Differential Signaling
LVSTL	Low-Voltage Swing Terminated Logic
MIPI	Mobile Industry Processor Interface
NDA	Non-Disclosure Agreement
OSC	Oscillator
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
SSTL	Stub Series-Terminated Logic
SERDES	Serializer/Deserializer

1. Introduction

When designing complex hardware using the MachXO5™-NX Root-of-Trust devices, you must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware implementation items relative to the MachXO5-NX Root-of-Trust devices. The document does not provide detailed step-by-step instructions but gives a high-level summary checklist to aid in the design process.

Hardware checklists are developed after evaluation boards and incorporate optimized designs that improve upon the circuitry of evaluation boards. If you copy circuits from evaluation boards, ensure to optimize your designs according to the hardware checklists.

This technical note assumes that the reader is familiar with the MachXO5-NX Root-of-Trust device features as described in the MachXO5-NX Root-of-Trust Devices Family Data Sheet (FPGA-DS-02120). The data sheet includes the functional specifications for the device. Topics covered in the data sheet include, but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions.
- Device-specific information about peripherals and registers
- Electrical specifications

Refer to the MachXO5-NX Root-of-Trust Devices Family Data Sheet (FPGA-DS-02120) for details. The critical hardware areas covered in this technical note are:

- Power supplies as they relate to the MachXO5-NX Root-of-Trust power supply rails and how to connect them to the PCB and the associated system.
- Configuration mode selection for proper power-up behavior.
- Device I/O interface and critical signals.

Important: Refer to the following documents for detailed recommendations.

- sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099)
- sysI/O User Guide for Nexus Platform (FPGA-TN-02067)
- sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095)
- Memory User Guide for Nexus Platform (FPGA-TN-02094)
- MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286)
- Thermal Management (FPGA-TN-02044)
- sysDSP User Guide for Nexus Platform (FPGA-TN-02096)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- HSPICE SERDES simulation package (available under NDA, contact the license administrator at lic_admin@latticesemi.com)
- MachXO5-NX 15D pinout table (FPGA-SC-02043)
- MachXO5-NX 55TD pinout table (FPGA-SC-02041)
- MachXO5-NX 55TDQ pinout table (FPGA-SC-02109)
- MachXO5-NX 20TD pinout table (FPGA-SC-02104)
- MachXO5-NX 20TDQ pinout table (FPGA-SC-02105)
- MachXO5-NX 30TD pinout table (FPGA-SC-02106)
- MachXO5-NX 30TDQ pinout table (FPGA-SC-02107)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- ADC User Guide for Nexus Platform (FPGA-TN-02129)

2. Power Supplies

At power up, the V_{CC}, V_{CCAUX}, V_{CCIO1}, and V_{CCIO2} power supplies are monitored to determine when the MachXO5-NX Root-of-Trust device should de-assert its internal Power-On Reset state and enter the Power Good condition, which starts device initialization and configuration. These supplies should come up monotonically. Other supplies are not monitored during power-up but need to be at a valid and stable level before the device configuration is complete. Several other supplies are used in conjunction with onboard SERDES blocks and ADCs.

Table 2.1 describes the LFMXO5-15D, LFMXO5-20TD/Q, and LFMXO5-30TD/Q power supplies and the appropriate voltage levels for each supply.

Table 2.1. Power Supplies for LFMXO5-15D, LFMXO5-20TD/Q, LFMXO5-30TD/Q

Supply	Voltage (Nominal Value)	Description
V_{SS}	—	Ground for internal FPGA logic and I/O.
V_{SSSDx}	—	Ground for SERDES.
V_{CC}	1.0 V	FPGA core power supply. Required for Power Good condition.
V_{CCECLK}	1.0 V	FPGA core clock power supply.
V_{CCAUX}	1.8 V	Auxiliary power supply pin for I/O Bank 0, Bank 1, Bank 2, Bank 3, Bank 4, Bank 7, Bank 8, and Bank 9. Used for generating stable drive current for the I/O.
$V_{CCAUXHx}$	1.8 V	Auxiliary power supply pin for I/O Bank 5, and Bank 6. Used for generating stable drive current for the I/O and stable current for the differential input comparators.
V_{CCAUXA}	1.8 V	Auxiliary Supply Voltage for internal analog circuitry. Required for Power Good condition.
$V_{CCIO[9:0]}$	Wide-Range Banks: Banks 1, 2 : 3.3 V Only Banks 0, 3, 4, 7, 8, 9: 1.2 V, 1.35 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V High-Speed Banks: Banks 5, 6: 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V	Bank I/O Driver Supply Voltage. Each bank has its own V_{CCIO} supply. Banks 1 and 2 are 3.3V only. 1.35 V is for DDR3L only. V_{CCIO1} and V_{CCIO2} have pins used for device configuration and are required for Power Good condition.
$V_{CCADC18}$	1.8 V	ADC Block power supply. Should be isolated from excessive noise.
V_{CCSDx}	1.0 V	SERDES Block Core power supply voltage. Should be isolated from excessive noise. This rail is for **T** (SERDES support) parts only.
V_{CCSDCK}	1.0 V	SERDES Block Clock buffer supply voltage. Should be isolated from excessive noise. This rail is for **T** (SERDES support) parts only.
$V_{CCPLLSDx}$	1.8 V	SERDES Block PLL power supply voltage. Should be isolated from excessive noise. This rail is for **T** (SERDES support) parts only.
$V_{CCAUXSDQx}$	1.8 V	SERDES Block Auxiliary power supply voltage. Should be isolated from excessive noise. This rail is for **T (**(SERDES support) parts only.
V_{CCSDx}	1.0 V	SERDES Block Core power supply voltage. Should be isolated from excessive noise. This rail is for **T** (SERDES support) parts only.

Table 2.2 describes the LFMXO5-55TD/Q power supplies and the appropriate voltage levels for each supply.

Table 2.2. Power Supplies for LFMXO5-55TD/Q

Supply	Voltage (Nominal Value)	Description
V_{SS}	—	Ground for internal FPGA logic and I/O.
V_{SSADC}	—	Ground for ADC.
V_{SSSDx}	—	Ground for SERDES.
V_{SSR}	Pull down to ground	Connect to ground through a 1.0 kΩ resistor.
V_{CC}	1.0 V	FPGA core power supply. Required for Power Good condition.
V_{CCECLK}	1.0 V	FPGA core clock power supply.
V_{CCAUX}	1.8 V	Auxiliary power supply pin for I/O Bank 0, Bank 1, Bank 2, Bank 6, Bank 7. Used for generating stable drive current for the I/O.
$V_{CCAUXHx}$	1.8 V	Auxiliary power supply pin for I/O Bank 3, Bank 4, and Bank 5. Used for generating stable drive current for the I/O and stable current for the differential input comparators.
V_{CCAUXA}	1.8 V	Auxiliary Supply Voltage for internal analog circuitry. Required for Power Good condition.
$V_{CCIO[9:0]}$	Wide-Range Banks: Banks 0, 7: 3.3 V Only Banks 1, 2, 6: 1.2 V, 1.35 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V High-Speed Banks: Banks 3, 4, 5: 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V	Bank I/O Driver Supply Voltage. Each bank has its own V_{CCIO} supply. Banks 0 and 7 are 3.3 V only. 1.35 V is for DDR3L only. V_{CCIO0} and V_{CCIO1} have pins used for device configuration and are required for Power Good condition.
$V_{CCADC18}$	1.8 V	ADC Block power supply. Should be isolated from excessive noise.
ADC_REFP[1:0]	1.0 V to 1.8 V Typical	ADC External Reference. Should be isolated from excessive noise and have high accuracy (< 0.1% tolerance).
V_{CCSDx}	1.0 V	SERDES Block Core power supply voltage. Should be isolated from excessive noise.
V_{CCSDCK}	1.0 V	SERDES Block Clock buffer supply voltage. Should be isolated from excessive noise.
$V_{CCPLLSDx}$	1.8 V	SERDES Block PLL power supply voltage. Should be isolated from excessive noise.
$V_{CCAUXSDQx}$	1.8 V	SERDES Block Auxiliary power supply voltage. Should be isolated from excessive noise.

2.1. Power Noise

The power rail voltages of the FPGA allow for a worst-case normal operating tolerance of ±5% of these voltages. The 5% tolerance includes any noise.

2.2. Power Source

It is recommended that the designed voltage regulators are accurate to within 3% of the optimum voltage to allow power noise design margin.

When calculating the voltage regulator's total tolerance, include:

- Regulator voltage reference tolerance.
- Regulator line tolerance.
- Regulator load tolerance.
- Tolerances of any resistors connected to the regulator's feedback pin, which sets the regulator's output voltage.
- Expected voltage drops due to power filtering the ferrite bead's ESR × expected current draw.
- Expected voltage drops due to the current measuring resistor's ESR × expected current draw.

With a 3% tolerance allocated to the voltage source, the design has a remaining 2% tolerance for noise and layout related issues. The 1.0 V rail is especially sensitive to noise, as every 10 mV is 1% of the rail voltage. For SERDES power rails target a maximum 1% peak noise. For PLLs target a maximum of 0.5% peak noise to minimize jitter.

3. Power Supply Filtering

Providing a quiet, filtered supply is important for all rails and critical for the analog rails. Supplies should be decoupled with adequate power filters. Bypass capacitors must be located close to the device package pins with very short traces to keep inductance low.

For the best performance, use careful pin assignments to keep noisy I/O pins away from sensitive functional pins. The leading causes of PCB-related crosstalk with sensitive blocks are related to FPGA outputs found in close proximity to the sensitive power supplies. These supplies require cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet-filtered supplies for the analog supplies; however, robust PCB layout is required to ensure that noise does not infiltrate into these analog supplies.

It is critical to have very low-noise, highly filtered supplies for the SERDES and ADCs. Low noise LDO regulators for these rails is recommended. These supplies are also paired with dedicated ground pins.

3.1. Recommended Power Filtering Groups and Components

Table 3.1. Recommended Power Filtering Groups and Components

Power Input	Recommended Filter	Notes
V_{SSR}	Pull down to Ground	Connect to ground through a 1.0 kΩ resistor.
V_{CC}, V_{CCECLK}	10 µF x 2 + 100 nF per pin	Core and clock logic. Tie V_{CC} and V_{CCECLK} pins together. 1.0 V
V_{CCAUX}, $V_{CCAUXHx}$	120 Ω FB + 10 µF + 100 nF per pin	Auxiliary power supply pins. Tie V_{CCAUX} and $V_{CCAUXHx}$ pins together. 1.8 V
V_{CCAUXA}	120 Ω FB + 10 µF + 100 nF per pin	Auxiliary power supply pin for internal sensitive analog circuitry. 1.8 V
V_{CCIOX}	10 µF + 100 nF per pin for each V_{CCIOx}	Bank I/O. Unused banks can use a single 1.0 µF. For banks with lots of outputs or large capacitive loading replace the 10 µF with a 22 µF (or use two 10 µF). LFMXO5-15D, LFMXO5-20TD/Q and LFMXO5-30TD/Q Banks 1, 2: 3.3 V Only Banks 0, 3, 4, 7, 8, 9: 1.2 V, 1.35 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V Banks 5, 6: 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V LFMXO5-55TD/Q: Banks 0, 7: 3.3 V Only Banks 1, 2, 6 : 1.2 V, 1.35 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V Banks 3, 4, 5: 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V
$V_{CCADC18}$	220 Ω or 120 Ω FB + 10 µF + 100 nF per pin	ADC Blocks. If both ADC blocks are not used, leave open. 1.8 V
ADC_REFP[1:0]	220 Ω or 120 Ω FB + 1.0 µF + 100 nF per pin	ADC Block External Reference. Must have very low noise and high accuracy reference (≤ 0.1% Tolerance). Voltage source/regulator should be filtered by 220 Ω or 120 Ω FB + 1 µF. If ADC Block is not used, connect its ADC_REFPx to ground through 0 Ω resistor. 1.0 V to 1.8 V Typical

Power Input	Recommended Filter	Notes
V_{CCSDx}	120 Ω FB + 10 µF + 100 nF per pin	SERDES Block Core. If SERDES block is not used, leave it open. 1.0 V
V_{CCSDCK}	120 Ω FB + 10 µF + 100 nF per pin	SERDES Block Clock buffer. If both SERDES blocks are not used, leave it open. 1.0 V
$V_{CCPLLSDx}$	220 Ω FB + 47 µF + 470 nF per pin IMPORTANT: Connect capacitor grounds only to FPGA pin SDx_REFRET	SERDES Block PLL. If SERDES block is not used, leave open. Bypass capacitor grounds go only to SDx_REFRET 1.8 V
$V_{CCAUXSDQx}$	120 Ω FB + (10 µF and 100 nF to each channel's SDx_REFRET)	SERDES Block Auxiliary. If SERDES block is not used, leave open. Bypass capacitor grounds go only to SDx_REFRET 1.8 V

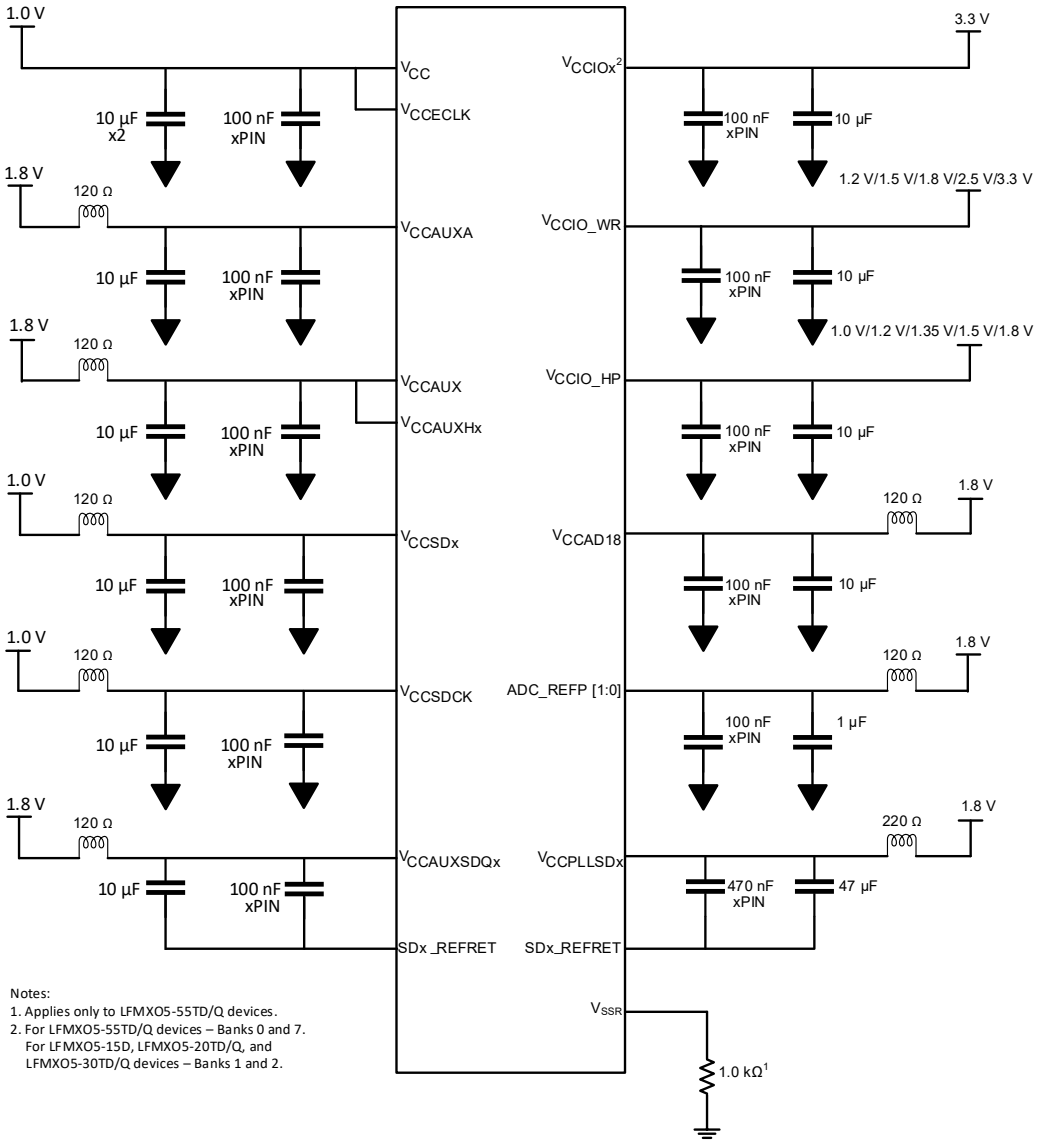


Figure 3.1. Recommended Power Filter

3.2. Ground Pins

- All V_{SS}, V_{SSSDx}, and V_{SSADC} ground pins need to be connected to the board's ground plane.
- V_{SSSDx} and V_{SSADC} pins are sensitive to noise and should be isolated from fast switching high current pathways on the ground plane. Ground plane islands can be used to help isolate sensitive grounds from noisy ground areas. The ground plane islands must connect at only one location to the main ground plane. Connection locations should be at least 2 mm wide. Only signals in the same domain as the ground plane island should be referenced to that island.
- V_{SSR} Should be connected to ground through a 1.0 kΩ resistor.
- SDx_REFRET — Input SERDES Reference Return Input. This pin should be AC coupled (bypassed) to the $V_{CCPLLSDx}$ supply.

3.3. Unused Bank V_{CCIOX}

- Connect unused V_{CCIOX} pins to a power rail. Do not leave them open.

3.4. Unused ADC Blocks

- If all ADC blocks are unused leave $V_{CCADC18}$ open.
- Unused ADC Blocks should connect ADC_REFx, ADC_DPx and ADC_DNx to board ground.
- V_{SSADC} pins should be connected to the board's ground plane even if ADC blocks are unused.

3.5. Unused Both SERDES Channels

- Connect to board ground V_{SSSDQ} pins, SDx_RXDP/N [x=0 and 3], SDx_REXT [x=0 and 3], SDx_REFRET [x=0 and 3] and SDQ0_REFCLKP/N.
- Leave the following open: V_{CCSDx} [x=0 and 3], $V_{CCPLLSDx}$ [x=0 and 3], SDx_TXDP/N [x=0 and 3], $V_{CCAUXSDQ0}$, and V_{CCSDCK}.

3.6. Single Unused SERDES Channel

- Connect to board ground V_{SSSDQ} pins, along with unused channel's SDx_RXDP/N [x=0 or 3], SDx_REXT [x=0 or 3], and SDx_REFRET [x=0 or 3].
- Leave the following open on the unused channel: V_{CCSDx} [x=0 or 3], $V_{CCPLLSDx}$ [x=0 or 3], SDx_TXDP/N [x=0 or 3].

3.7. Clock Oscillator Supply Filtering

When providing an external reference clock to the FPGA, for example, a single-ended or differential clock oscillator, proper power supply isolation and decoupling of the clock oscillator is required to reduce clock jitter.

When specifying components, choose good-quality dielectrics ceramic capacitors in small packages and place them as close to the clock oscillator supply pins as practically possible.

When providing an external reference clock to the FPGA, ensure that the oscillator's output voltage to the FPGA does not exceed the bank's voltage. Figure 3.2 shows a typical bypassing circuit.

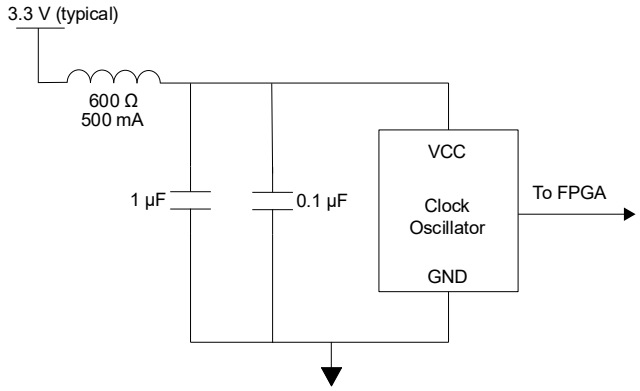


Figure 3.2. Clock Oscillator Bypassing

3.8. Ferrite Bead Selection

- Most designs work well using ferrite beads between 120 Ω at 100 MHz and 240 Ω at 100 MHz.
- Ferrite bead induced noise voltage from ESR × CURRENT should be < 1% of rail voltage for non-analog rails and < 0.25% for sensitive rails.
- Non-PLL rails should use ferrite beads with an ESR between 0.025 Ω and 0.10 Ω depending on the current load.
- PLL rails draw low current, which allows ferrite beads with an ESR ≤ 0.3 Ω.
- Small package size ferrite beads have a higher ESR than large package size ferrite beads of the same impedance.
- High impedance ferrite beads have a higher ESR than low impedance ferrite beads in the same package size.

3.9. Capacitor Selection

When specifying components, choose good quality ceramic capacitors in small packages and place them close to the power oscillator supply pins with short low inductance connections. Good quality capacitors for bypassing generally meet the requirements discussed in the following sections.

3.9.1. Capacitor Dielectric

Use dielectrics such as X5R, X7R, and similar that have good capacitance tolerance (≤ ±20%) over a temperature range. Avoid Y5V, Z5U, and similarly poor capacitance-controlled dielectrics.

3.9.2. Voltage Rating

Capacitor working capacitance decreases non-linearly with a higher voltage bias. To maintain capacitance, the capacitor voltage rating should be at least 80% higher than the voltage rail (maximum). Example: 3.3 V rail bypass capacitors should use the commonly available 6.3 V rating as a minimum.

3.9.3. Size

Smaller body capacitors have lower inductance, work at higher frequencies, and improve board layout. For a given voltage rating, smaller body capacitors tend to cost more than larger body capacitors. Optimizing the difference between market pricing and size-related inductance, the following capacitor sizes are recommended:

Table 3.2. Recommended Capacitor Sizes

Capacitance	Size Preferred	Size Next Best
0.1 µF	0201	0402
1.0 µF, 2.2 µF	0402	0201
4.7 µF	0402	0603
10 µF	0402	0603
22 µF	0805	0603

4. Power

There is no power-up sequence required for the MachXO5-NX Root-of-Trust device.

5. Power Estimation

Once you finalize the MachXO5-NX Root-of-Trust device density, package, and logic implementation, power estimation for the system environment should be determined using the Power Calculator included in the Lattice Radiant™ design tool. When performing power estimating, you should keep two goals in mind:

- Power supply budgeting should be based on the maximum power-up in-rush current, configuration current, and maximum DC and AC current under the system's environmental conditions.
- Thermal considerations are also important. Ensure the thermal design of the system environment and MachXO5-NX Root-of-Trust device can operate at the maximum operating junction temperature.

Consider both criteria early in the design phase to ensure reliable system performance.

6. Configuration Considerations

PCB layout design and breakout suggestions are outlined in PCB Layout Recommendations for BGA Packages (FPGA-TN-02024). For application-specific assembly guidance, consult the design guidelines of the assembly service provider.

The MachXO5-NX Root-of-Trust device supports provisioning the FPGA via the JTAG and SSPI interface . The JTAG port includes a 4-pin interface. The interface requires the following PCB considerations.

Table 6.1. JTAG Pin Recommendations for LFMXO5-15D, LFMXO5-20TD/Q and LFMXO5-30TD/Q

JTAG Pin	PCB Recommendation
TDO	4.7 kΩ pull-up to V_{CCIO2}
TMS	4.7 kΩ pull-up to V_{CCIO2}
TDI	4.7 kΩ pull-up to V_{CCIO2}
TCK	2.2 kΩ pull-down to GND
JTAG_EN	4.7 kΩ pull-down to GND (JTAG port disabled) or 1.0 kΩ pull-up to V_{CCIO2} (JTAG port enabled)

Table 6.2. JTAG and SSPI Pin Recommendations for LFMXO5-55TD/Q

JTAG Pin	PCB Recommendation
IF_TDO	4.7 kΩ pull-up to V_{CCIO7}
IF_TMS	4.7 kΩ pull-up to V_{CCIO7}
IF_TDO	4.7 kΩ pull-up to V_{CCIO7}
IF_TCK	2.2 kΩ pull-down to GND
CSN	4.7 kΩ pull-up to V_{CCIO7}
MCLK	No Pull Resistor
MISO	No Pull Resistor
MOSI	No Pull Resistor

Every PCB is recommended to have easy access to FPGA JTAG pins for provision For best results, route the TCK/IF_TCK, TMS/IF_TMS, TDI/IF_TDI, and TDO/IF_TDO signals or CSN, MCLK, MISO, and MOSI to a common test header along with the corresponding V_{CCIO} and ground.

External resistors are necessary on configuration signals if they are used to handshake with other devices. External pull-resistors are not necessary on individual configuration pins when the signal pin is not persisted.

Recommended pull-up resistors to the appropriate bank V_{CCIO} and pull-down resistors to board ground should be used on the pins in Table 6.3.

Table 6.3. Pull-up/Pull-down Recommendations for Configuration Pins for LFMXO5-15D, LFMXO5-20TD/Q and LFMXO5-30TD/Q

Pin	PCB Connection
PROGRAMN	4.7 kΩ pull-up to V_{CCIO1}
INITN	10 kΩ pull-up to V_{CCIO1}
DONE	10 kΩ pull-up to V_{CCIO1}
JTAG_EN	4.7 kΩ pull-down to GND (JTAG port disabled) or 1.0 kΩ pull-up to V_{CCIO2} (JTAG port enabled)
MODE	1.0 kΩ to 4.7 kΩ pull-up to V_{CCIO2}

Table 6.4. Pull-up/Pull-down Recommendations for Configuration Pins for LFMXO5-55TD/Q

Pin	PCB Connection
PROGRAMN	4.7 kΩ pull-up to V_{CCIO0}
INITN	10 kΩ pull-up to V_{CCIO0}
DONE	10 kΩ pull-up to V_{CCIO0}
MODE[2:0]	1.0 kΩ to 4.7 kΩ pull-up to V_{CCIO7}

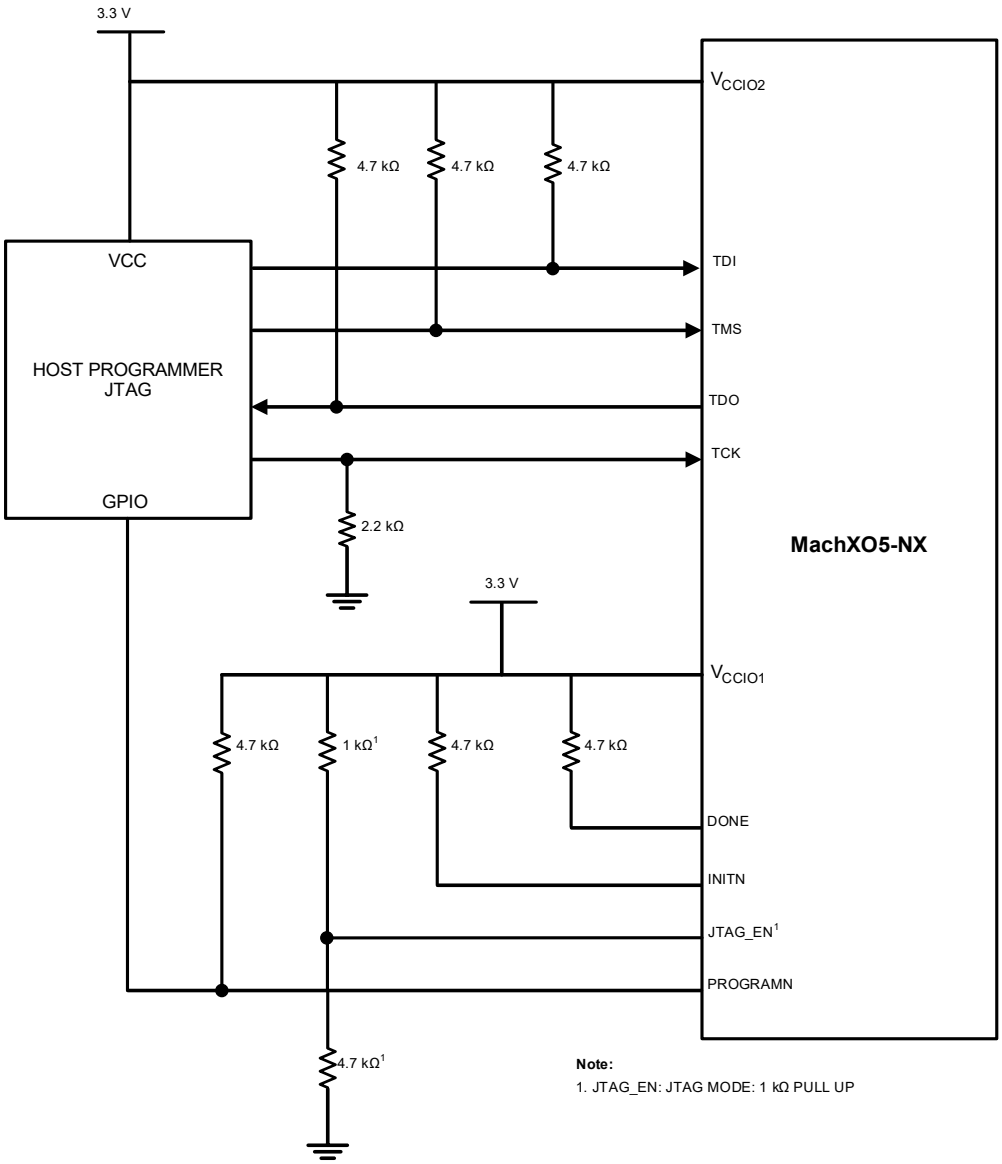


Figure 6.1. Typical Connections for Device Provisioning via JTAG for LFMXO5-15D, LFMXO5-20TD/Q and LFMXO5-30TD/Q

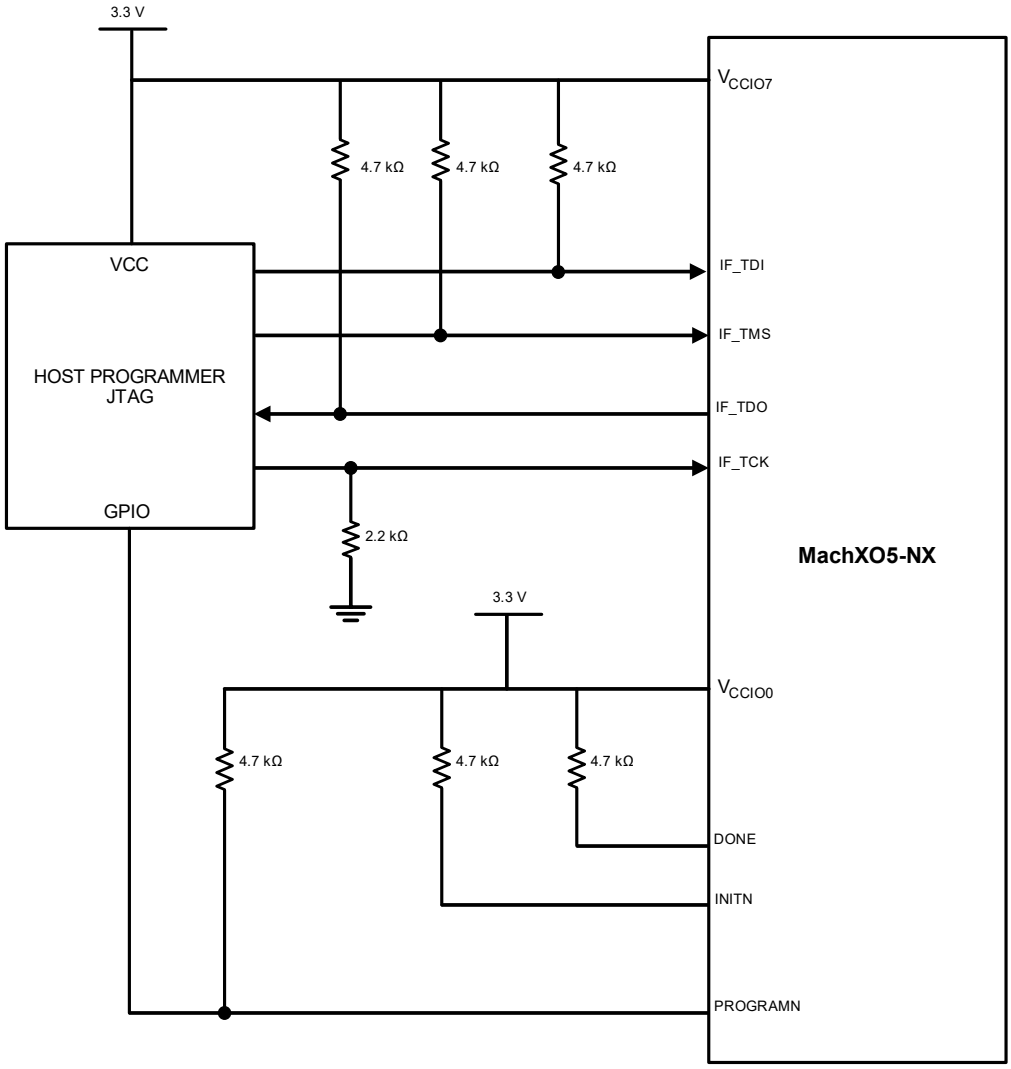
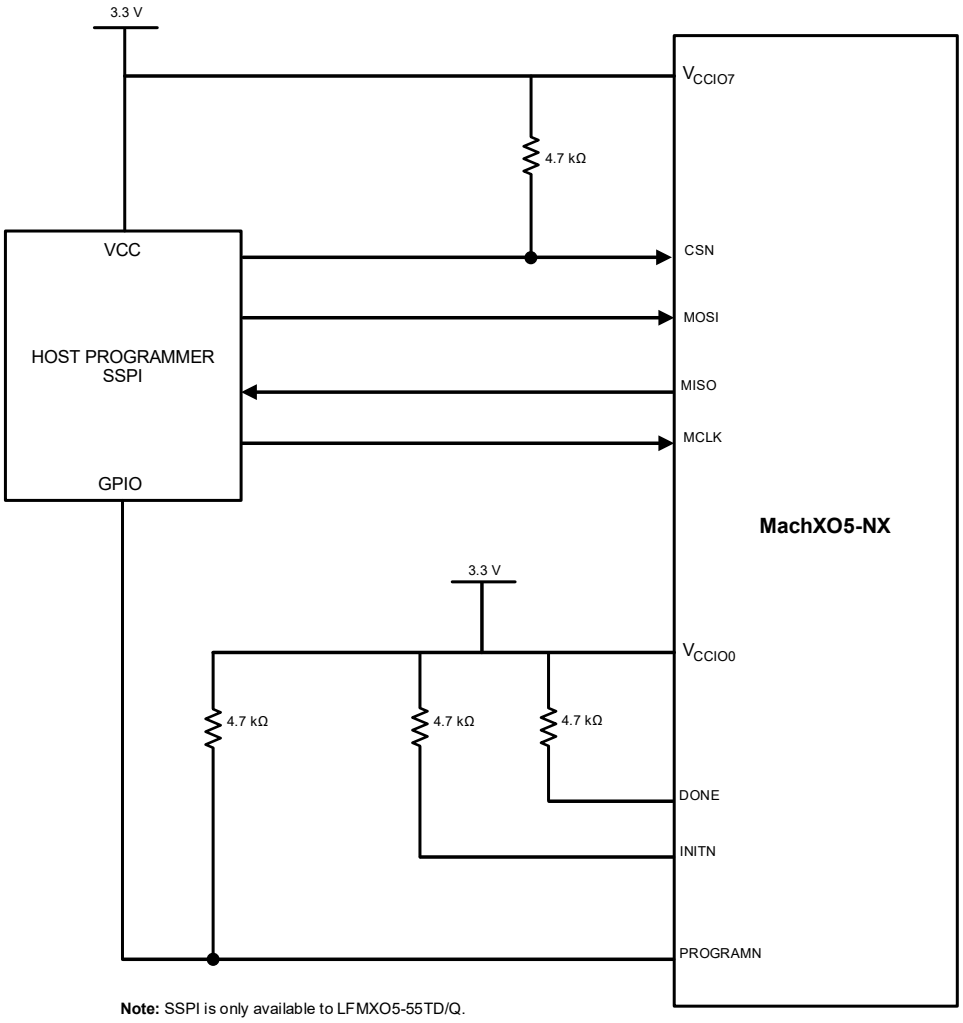


Figure 6.2 Typical Connections for Device Provisioning via JTAG for LFMXO5-55TD/Q



Note: SSPI is only available to LFMXO5-55TD/Q.

Figure 6.3. Typical Connections for Device Provisioning via SSPI

7. I/O Pin Assignments

The V_{CCSDCK}, $V_{CCPLLSDx}$ and $V_{CCAUXSDQx}$ provide quiet supplies for the SERDES blocks. For the best jitter performance, careful pin assignment keeps noisy I/O pins away from sensitive pins. The leading cause of PCB related SERDES crosstalk is related to FPGA outputs located in close proximity to the sensitive SERDES power supplies. These supplies require cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet filtered supplies; however, robust PCB layout is required to ensure that noise does not infiltrate into these analog supplies.

Although crosstalk generated coupling is reduced in the device packages of MachXO5-NX Root-of-Trust devices, the PCB board can cause significant noise injection from any I/O pin adjacent to SERDES data, reference clock, and power pins, as well as other critical I/O pins such as clock signals. Electrical Recommendations for Lattice SERDES (FPGA-TN-02077) provides detailed guidelines for optimizing the hardware to reduce the likelihood of crosstalk to the analog supplies. PCB traces running in parallel for long distances need careful analysis. Simulate any suspicious traces using a PCB crosstalk simulation tool to determine if they cause problems.

It is common practice for designers to select pinouts for their system early in the design cycle. For the FPGA designer, this requires detailed knowledge of the targeted FPGA device. Designers often use a spreadsheet program to initially capture the list of the design I/O. Lattice Semiconductor provides detailed pinout information that can be downloaded from the Lattice Semiconductor website in .csv format for designers to use as a resource to create pinout information. For example, by navigating to the pinout.csv file, you can gather the pinout details for all the different package offerings of the device in the family, including I/O banking, differential pairing, dual function of the pins, and input and output details.

7.1. Early I/O Release

The MachXO5-NX Root-of-Trust device supports an Early I/O Release feature, which allows the I/O that reside in the I/O banks on the left and right of the device (LFMXO5-15D, LFMXO5-20TD/Q, and LFMXO5-30TD/Q – Banks 2, 3, 4, 7, 8, 9 and LFMXO5-55TD/Q – Banks 1, 2, 6, 7) to assume user-defined drive states at the beginning of bitstream processing. The Early I/O Release feature releases the I/O after processing the I/O configuration for the left and right banks, which is located near the head of the bitstream data. Once data is programmed in the left/right Memory Interface Block (MIB), the I/O is released to a predefined state. This feature is enabled by setting the EARLY_IO_RELEASE preferences to ON in the Lattice Radiant Device Constraint Editor.

In addition, Early I/O Release requires you to instantiate an output buffer register with an asynchronous set or reset function to indicate the desired drive *1* or drive *0* behavior, respectively, during the Early Release period. Unregistered outputs in Early-Release banks drive High-Z until full device configuration is complete. Be aware that some of the I/O in Bank 2, including the dual-purpose sysCONFIG I/O, cannot be utilized as Early Released I/O. Also, if the ECDSA bitstream authentication is enabled for the MachXO5-NX Root-of-Trust device, the Early I/O Release feature is not supported.

8. sysI/O

The MachXO5-NX Root-of-Trust device provides the flexibility to configure each I/O according to your requirements. These pins can be configured as input, output, and tri-state. Additionally, attributes such as PULLMODE, CLAMP, HYSTERESIS, VREF, OPENDRAIN, SLEWRATE, DIFFRESISTOR, TERMINATION, and DRIVE STRENGTH can also be set up.

For the PULLMODE, pull-up and pull-down resistors can be set. The implementation of these resistors is by using a constant current that has the following values:

Table 8.1. Weak pull-up/down current specifications

Configuration	Parameter	Condition	Min	Max	Unit
Pull-up	I/O Weak pull-up resistor current	$0 \le VIN \le 0.7 \times V_{CCIO}$	–30	–150	µA
Pull-down	I/O Weak pull-down resistor current	$VIL\ (max) \le VIN \le V_{CCIO}$	30	150	µA

MachXO5-NX Root-of-Trust devices also provide special I/Os like HPIO and WRIO that can be used for high-speed communication.

Figure 8.1 shows the block diagram for HPIO. and Figure 8.2 shows the block diagram for WRIO.

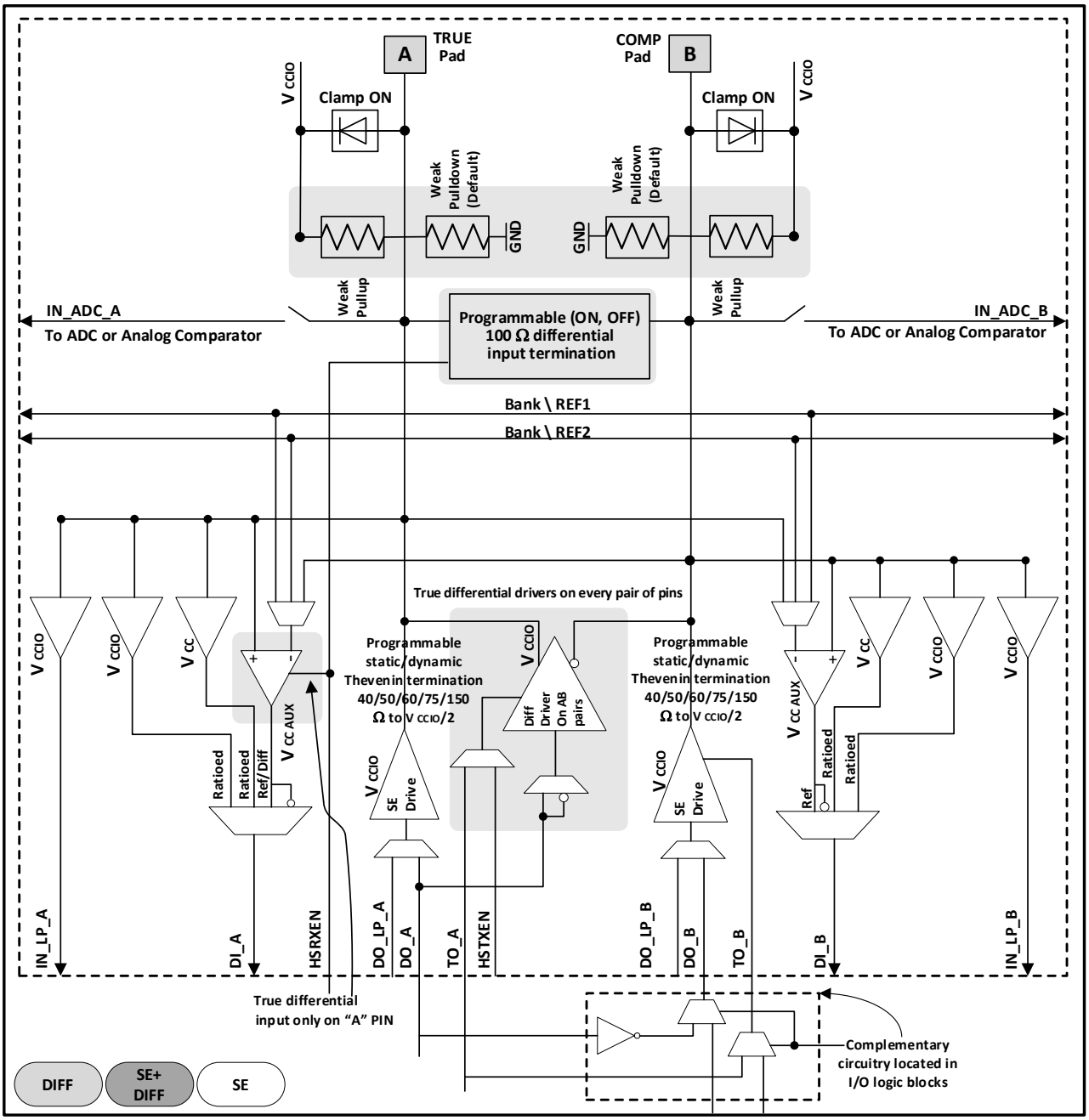


Figure 8.1. High-Performance sysI/O Buffer Pair for Bottom Side

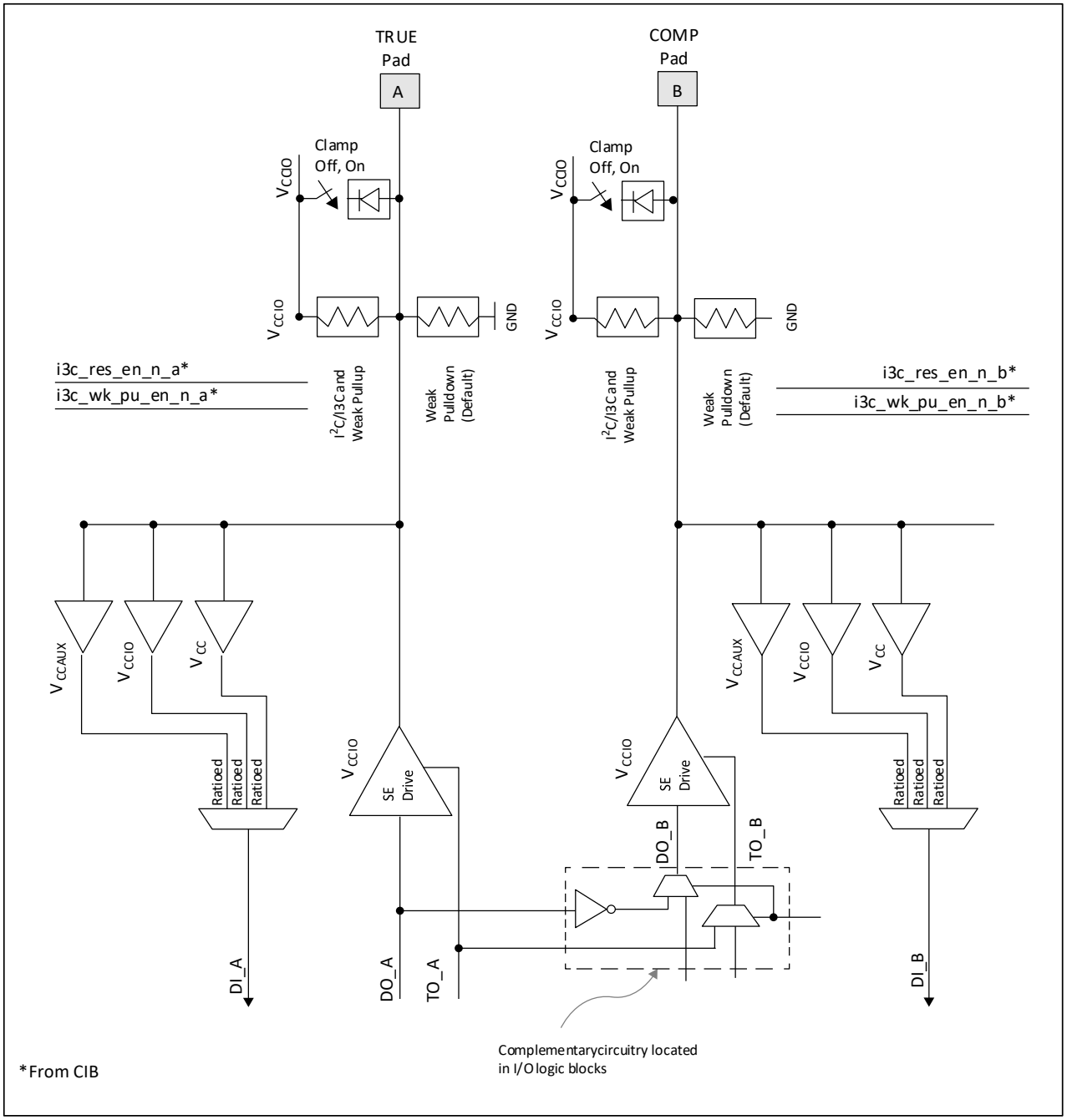


Figure 8.2. Wide Range sysI/O Buffer for Top, Left/Right Side

9. Clock Inputs

The MachXO5-NX Root-of-Trust device provides certain pins for use as clock inputs in each I/O bank. These pins are shared and can alternately be used for general purpose I/O. When these pins are used for clocking purposes, you need to pay attention to minimizing signal noise on these pins. Refer to the MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286).

These shared clock input pins, typically named GPLL and PCLK, can be found under the Dual Function column of the pinlist .csv file. High-speed differential interfaces (such as MIPI) must route their differential clock pairs into inputs that support differential clocking, specifically labeled as PCLKTx_y (+true) and PCLKCx_y (–complement). For single-ended I/Os, use only PCLKT pins as primary CLK pads.

For differential clock inputs to banks with a V_{CCIO} voltage of 1.5 V or lower, it is recommended to use an HCSL oscillator to keep the clock voltage less than or equal to the bank's V_{CCIO}. An LVDS oscillator can also be used if AC is coupled and then DC is biased at half the V_{CCIO} voltage. Example dual footprint design supporting HCSL and LVDS is shown below in Figure 9.1.

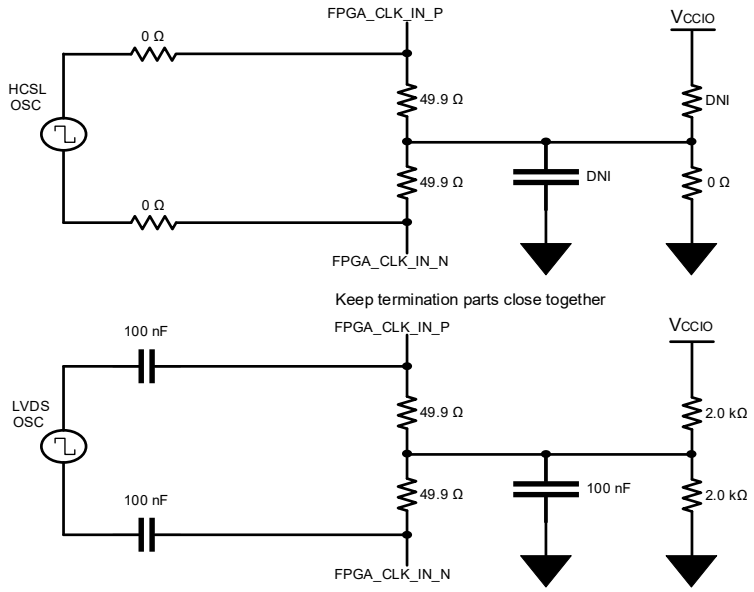


Figure 9.1. PCB Dual Footprint Supporting HCSL and LVDS Oscillators

9.1. PLL Reference Clock Locking

Reference clocks for PLLs must be stable before the PLL comes out of reset to guarantee proper PLL locking. PLLs should be held in reset using the PLL block's RST signal until the PLL's REFCLK signal is stable. See the Checklist section**.** The PLL reset procedure is usually required when an external oscillator or clock source becomes enabled or stable after the FPGA exits Power-On-Reset (POR). An example of a clock oscillator with a controlled enabled pin is shown in Figure 9.2.

Note: External board oscillators typically require 5 ms to 10 ms for their outputs to stabilize after being enabled. Check the oscillator's data sheet for the exact number.

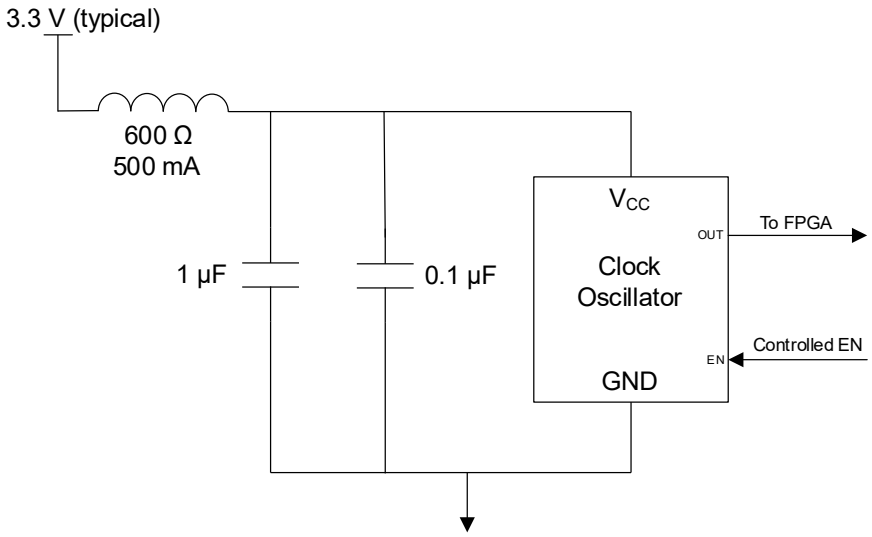


Figure 9.2 Clock Oscillator with Controlled Enable Pin

10. Pinout Considerations

The MachXO5-NX Root-of-Trust device supports many applications with high-speed interfaces. These include various rule-based pinouts that need to be understood prior to the implementation of the PCB design on these high-speed interfaces. The pinout selection must be completed with an understanding of the interface building blocks implemented in the FPGA fabric. These include IOLOGIC blocks such as DDR3L, clock resource connectivity, and PLL and DLL usage. Avoid placing noisy I/Os next to sensitive analog I/Os. Refer to MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286) for rules pertaining to these interface types.

10.1. LVDS Pin Assignments

True LVDS outputs are available on I/O pins on the device's bottom banks only (LFMXO5-15D, LFMXO5-20TD/Q and LFMXO5-30TD/Q – Banks 5, 6 and LFMXO5-55TD/Q – Banks 3, 4, 5). Other banks do not support the True LVDS output standard. Differential input pairing can be found in the pin list csv file.

Emulated LVDS output is available in pairs around all banks and requires external termination resistors. This is described in the sysI/O Usage Guide for Nexus Platform (FPGA-TN-02067).

10.2. Soft MIPI

Soft MIPI I/Os are available on the device's bottom banks only (LFMXO5-15D, LFMXO5-20TD/Q and LFMXO5-30TD/Q Banks 5, 6 and LFMXO5-55TD/Q Banks 3, 4, 5).

10.3. HSUL, SSTL, LVSTL[1], V_{REF} Pin Assignments

The HSUL, SSTL, and LVSTL[1] interfaces are reference I/O standards that require an external reference voltage. HSUL, SSTL, and LVSTL[1] are supported on the device's bottom banks only (LFMXO5-15D, LFMXO5-20TD/Q and LFMXO5-30TD/Q – Banks 5, 6 and LFMXO5-55TD/Q – Banks 3, 4, 5).

The V_{REF} pin(s) should get high priority when assigning pins to the PCB. These pins can be found in the Dual Function column with the V_{REF} label. Each bank includes a separate V_{REF} voltage. V_{REF} sets the threshold for the referenced input buffers. Each I/O is individually configurable based on the bank supply and reference voltages.

Connect a 0.1 µF capacitor to ground close to each used V_{REF} pin. The V_{REF} power source should have a relatively low output impedance (≤ 130 ohms).

Note:

1. LVSTL is supported only in LFMXO5-55TD/Q devices.

11. DPHY and SERDES Pin Considerations

High-speed signaling requires careful PCB design. Maintaining good transmission line characteristics is a requirement. A continuous ground reference should be maintained with high-speed routing. This includes tightly length matched differential routing (no larger than ±4 mil length mismatch) with very few discontinuities.

The DPHY clock input must use a PCLK pin so that it can be routed directly to the edge clock tree. Refer to High-Speed PCB Design Considerations (FPGA-TN-02178) for suggested methods and guidance. In the MachXO5-NX Root-of-Trust device the DPHY is a soft DPHY implementation.

12. Layout Recommendation

A good design from a schematic should also reflect a good layout for the system design to work without any issues with noise or power distribution. Below are some of the recommended layouts in general.

1. All power should come from power planes. This is to ensure good power delivery and thermal stability.
2. Each power pin has its own decoupling capacitor, typically 100 nF, that should be placed as close as possible to each other.
3. The placement of analog circuits must be away from digital circuits or high-switching components.
4. High-speed signals should have a clearance of five times the trace width of other signals.
5. High-speed signals that transition from one layer to another should have a corresponding transition ground if both reference planes are grounded. If the reference on the other layer is a V_{CC} plane, then a stitching capacitor should be used (ground to V_{CC}).

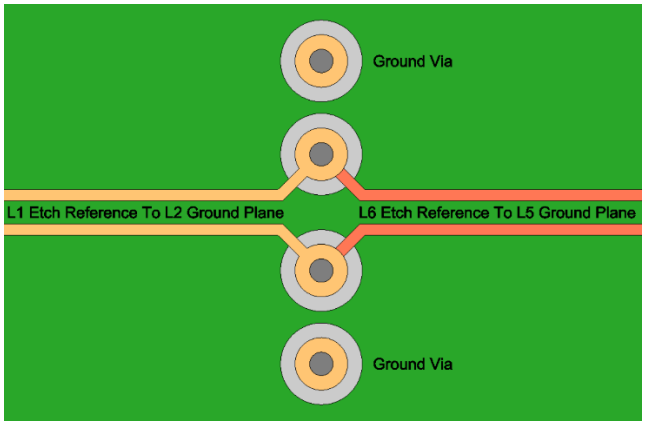


Figure 12.1. Ground Vias Implementation

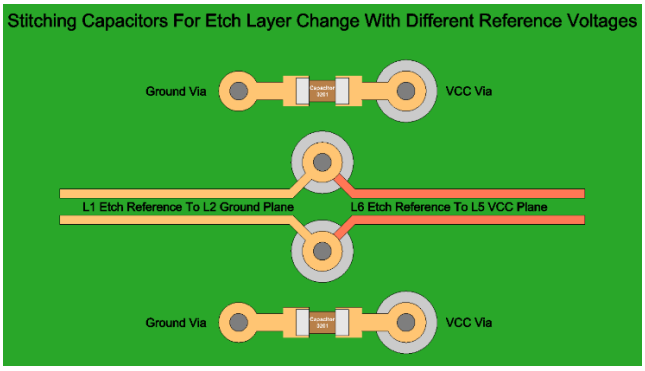


Figure 12.2. Stitching Vias Implementation

6. High-speed signals have a corresponding impedance requirement. Calculate the necessary trace width and trace gap (differential gap) according to the desired stack-up. Verify trace dimensions with the PCB vendor.
7. For differential pairs, be sure to match the length as closely as possible. A good rule of thumb is to match up to ±5mils.

For further information on layout recommendations, refer to:

- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)

13. Simulation and Board Measurement of Critical Signals

To ensure design reliability and high manufacturing yield, critical signals should be simulated during the design phase and subsequently measured on the assembled PCB to verify proper functionality.

13.1. Critical Signals

Signals that are sensitive to Signal Integrity (SI) degradation are considered critical signals and require additional design and verification attention.

Typical critical signals include:

- Differential Pairs (LVDS, subLVDS, SLVS, MIPI, USB, and the like)
- Clocks (Oscillator Inputs, Output Clocks)
- Data with embedded clocks
- Interrupts (Edge Triggered)
- Logic signals travelling long distances requiring termination

13.2. Simulation

Lattice Semiconductor supplies an IBIS (I/O Buffer Information Specification) file to be used with simulation tools. Popular simulations tools include:

- HyperLynx
- Sigrity
- SpectraQuest
- Micro-Cap (Free)

Most SI simulation tools are expensive and often require recurring subscription fees. These premium tools can import board design files and provide accurate simulations that include crosstalk and other signal integrity (SI) degrading effects.

Free IBIS-based tools (like Micro-cap) can offer useful basic simulations, but they require more manual effort to set up SI effects—especially when dealing with multiple signals, varying transmission line lengths, lossy lines, and crosstalk.

Simulation results should be used to optimize each critical signal for best signal integrity:

- Define output pin drive strength.
- Define output pin slew rate.
- Define output pin termination design (ex. output series termination resistor value).
- Define setting of internal pin pull-up and pull-down resistors.
- Improve PCB layout.

13.3. Board Measurements

Critical signals should be measured on the assembled PCB using an oscilloscope to verify proper signaling behavior and signal integrity (like eye diagrams and other SI parameters).

Measurement results should be used to optimize each critical signal for best signal integrity:

- Adjust output pin drive strength.
- Adjust output pin slew rate.
- Adjust output pin termination design (for example output series termination resistor value).
- Adjust the setting of internal pin pull-up and pull-down resistors.

Specification compliance testing is recommended for popular signaling methods (for example USB, MIPI).

14. Checklist

Table 14.1. Hardware Checklist

	Item	OK	NA
1	**FPGA Power Supplies**		
1.1	Core Supplies		
1.1.1	V_{SSR} connected to ground through a 1.0 kΩ resistor.		
1.1.2	V_{CC} and V_{CCECLK} tied together, core at 1.0 V ±3% (allowing for 2% noise).		
1.1.3	Use a PCB plane for V_{CC} and V_{CCECLK} core with proper decoupling.		
1.1.4	V_{CC} and V_{CCECLK} core sized to meet power requirement calculation from software.		
1.1.5	V_{CCAUX}, $V_{CCAUXHx}$, and V_{CCAUXA} at 1.8 V ±3% (allowing for 2% noise).		
1.1.6	V_{CCAUX}, $V_{CCAUXHx}$, and V_{CCAUXA} must be quiet and isolated from other switching noises.		
1.1.7	V_{CCAUX} pins ganged together with $V_{CCAUXHx}$ pins. Solid PCB plane is recommended.		
1.1.8	V_{CCAUXA} is sensitive, these pins should be ganged together and use a separate FB + Capacitor filtering. Solid PCB plane is recommended.		
1.2	I/O Supplies		
1.2.1	*Wide Range* V_{CCIO1} and V_{CCIO2} (LFMXO5-15D, LFMXO5-20TD/Q and LFMXO5-30TD/Q) 3.3 V Only. *Wide Range* V_{CCIO0} and V_{CCIO7} (LFMXO5-55TD/Q) 3.3 V Only.		
1.2.2	*Wide Range* V_{CCIOx} LFMXO5-15D, LFMXO5-20TD/Q and LFMXO5-30TD/Q Banks 0, 3, 4, 7, 8, 9 are between 1.2 V to 3.3 V. *Wide Range* V_{CCIOx} LFMXO5-55TD/Q Banks 1, 2, 6 are between 1.2 V to 3.3 V.		
1.2.3	*High Performance* V_{CCIOx} LFMXO5-15D, LFMXO5-20TD/Q and LFMXO5-30TD/Q Banks 5, 6 are between 1.0 V to 1.8 V. *High Performance* V_{CCIOx} LFMXO5-55TD/Q Banks 3, 4, 5 are between 1.0 V to 1.8 V.		
1.2.4	V_{CCIOx} bank voltage matches sysCONFIG peripheral devices such as system I3C, SPI Flash, etc.		
1.3	ADC power supply		
1.3.1	$V_{CCADC18}$ is 1.8 V ±3% (allowing for 2% noise).		
1.3.2	$V_{CCADC18}$ is quiet *and* isolated.		
1.3.3	Use accurate voltage reference for ADC_REFP[1:0] (≤ ±0.1% tolerance)		
1.3.4	If both ADC Blocks are unused leave $V_{CCADC18}$ open.		
1.3.5	Unused ADC Blocks should connect ADC_REFPx to ground through 0 Ω resistor.		
1.3.6	V_{SSADC} pin should be connected to the board's ground plane even if ADC Blocks are unused.		
1.4	SERDES Power Supplies		
1.4.1	V_{CCSDx} and V_{CCSDCK} are at 1.0 V ±5%		
1.4.2	V_{CCSDx} and V_{CCSDCK} quiet *and* isolated from each other and other 1.0 V supplies		
1.4.3	$V_{CCPLLSDx}$ and $V_{CCAUXSDQ0}$ are 1.8 V +5%		
1.4.4	$V_{CCPLLSDx}$ and $V_{CCAUXSDQ0}$ quiet *and* isolated from each other and other 1.8 V supplies		
1.4.5	$V_{CCPLLSDx}$ and $V_{CCAUXSDQ0}$ bypass capacitor grounds go only to SDx_REFRET		
1.4.6	Unused Both SERDES Channels Connect to board ground V_{SSSDQ} pins, SDx_RXDP/N [x=0 and 3], SDx_REXT [x=0 and 3], SDx_REFRET [x=0 and 3] and SDQ0_REFCLKP/N. Leave the following open: V_{CCSDx} [x=0 and 3], $V_{CCPLLSDx}$ [x=0 and 3], SDx_TXDP/N [x=0 and 3], $V_{CCAUXSDQ0}$, and V_{CCSDCK}.		
1.4.7	Single Unused SERDES Channel Connect to board ground V_{SSSDQ} pins, along with unused channel's SDx_RXDP/N [x=0 or 3], SDx_REXT [x=0 or 3], and SDx_REFRET [x=0 or 3]. Leave the following open on the unused channel: V_{CCSDx} [x=0 or 3], $V_{CCPLLSDx}$ [x=0 or 3], SDx_TXDP/N [x=0 or 3].		
1.5	**Grounds**		
1.5.1	All ground pins must be connected to low impedance ground plane.		

	Item	OK	NA
1.6	**Reference Clocks**		
1.6.1	External reference clock source, such as oscillators, should have quiet power filtering to reduce clock jitter. Refer to the Clock Oscillator Supply Filtering section for details.		
1.6.2	When providing an external reference clock to the FPGA, ensure that the oscillator's output voltage to the FPGA does not exceed the bank's voltage.		
1.7	**Power Filtering Components**		
1.7.1	Power filter circuits should use good-quality ferrite beads and capacitors. Ceramic capacitor dielectrics should be low at loss, and capacitors should be placed close to power supply pins. Refer to the Ferrite Bead Selection section and Capacitor Selection section for details.		
2	**JTAG**		
2.1	Pull-up or Pull-down on JTAG_EN, per Table 6.1.		
2.2	Keep JTAG_EN accessible on PCB to recover JTAG port, especially during development.		
2.3	Keep JTAG port pins accessible on PCB, especially during development		
2.4	Pull-down on TCK per Table 6.1.		
2.5	Pull-up on TMS per Table 6.1.		
3	**Configuration**		
3.1	Pull-ups or pull-downs on persisted configuration specific pins per Table 6.1, Table 6.2, Table 6.3 and Table 6.4.		
3.2	V_{CCIOx} bank voltage matches sysCONFIG peripheral devices such as system I3C, SPI Flash, etc.		
4	**Special Pin Assignments**		
4.1	V_{REF} assignments followed for single-ended reference inputs		
4.2	Properly decouple the V_{REF} pin		
4.3	The V_{REF} source should have relatively low output impedance (≤ 130 Ω)		
4.4	Soft MIPI I/Os are on the device's bottom banks only (LFMXO5-15D, LFMXO5-20TD/Q, and LFMXO5-30TD/Q – Banks 5, 6 and LFMXO5-55TD/Q – Banks 3, 4, 5).		
5	**Critical Pinout Selection**		
5.1	Pinout is chosen to address FPGA resource connections to I/O logic and clock resources per MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286).		
5.2	Shared general purpose I/O are used as inputs for FPGA PLL and Clock inputs.		
5.3	Differential pair I/O polarity: I/O are named P[T/B/L/R] [Number]_[A/B] Diff pair positive signal connects to name ending in A, Negative connects to name ending in B.		
5.4	Differential clock inputs, including for soft MIPI, must use a PCLK pin input.		
5.5	For single-ended I/Os, use only PCLKT pins as primary CLK pads.		
6	**DDR3L Interface Requirements**		
6.1	DQ, DM, and DQS signals should be routed in a data group and should have similar routing and matched via counts. Using more than three vias is not recommended in the route between the FPGA controller and memory device.		
6.2	Maintain trace length matching to a maximum of ±20 mil between any DQ/DM and its associated DQS strobe within a DQ group. Use careful serpentine routing to meet this requirement.		
6.3	All data groups must reference a ground plane within the stack-up.		
6.4	DDR trace reference must be solid without slots or breaks. It should be continuous between the FPGA and the memory.		
6.5	Provide a separation of 3 W spacing between a data group and any other unrelated signals to avoid crosstalk issues. Use a minimum of 2 W spacing between all DDR traces excluding differential CK and DQS signals. (W is the minimum width of the signal trace allowed)		
6.6	Assigned FPGA I/O within a data group can be swapped to allow clean layout. Do not swap DQS assignments.		
6.7	Differential pair of DQS to DQS_N trace lengths should be matched to ±10 mil.		
6.8	Resistor terminations (DQ) placed in a fly-by fashion at the FPGA is highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mil.		
6.9	LDQS/LDQS_N and UDQS/UDQS_N trace lengths should be matched within ±100 mil.		

	Item	OK	NA
6.10	Address/control signals and the associated CK and CK_N differential FPGA clock should be routed with a control trace matching ±100 mil.		
6.11	CK to CK_N trace lengths must be matched within 10 mil.		
6.12	Address and control signals can be referenced to a power plane if a ground plane is not available. Ground reference is preferred.		
6.13	Address and control signals should be kept on a different routing layer from DQ, DQS, and DM to isolate crosstalk between the signals.		
6.14	Differential terminations used by the CLK/CLKN pair must be located as close as possible to the memory.		
6.15	Address and control terminations placed after the memory component using a fly-by technique are highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mils.		
7	**ADC**		
7.1	When using ADC function, use the PLL in the lower right corner (this PLL is closest on die to the ADC.)		

References

- MachXO5-NX Root-of-Trust Devices Family Data Sheet (FPGA-DS-02120)
- MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286)
- MachXO5-NX 15D pinout table (FPGA-SC-02043)
- MachXO5-NX 55TD pinout table (FPGA-SC-02041)
- MachXO5-NX 55TDQ pinout table (FPGA-SC-02109)
- MachXO5-NX 20TD pinout table (FPGA-SC-02104)
- MachXO5-NX 20TDQ pinout table (FPGA-SC-02105)
- MachXO5-NX 30TD pinout table (FPGA-SC-02106)
- MachXO5-NX 30TDQ pinout table (FPGA-SC-02107)
- sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099)
- sysI/O User Guide for Nexus Platform (FPGA-TN-02067)
- sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095)
- Memory User Guide for Nexus Platform (FPGA-TN-02094)
- sysDSP User Guide for Nexus Platform (FPGA-TN-02096)
- Thermal Management (FPGA-TN-02044)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- ADC User Guide for Nexus Platform (FPGA-TN-02129)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- Lattice Radiant FPGA design software.
- Lattice Insights for Lattice Semiconductor training courses and learning plans.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at https://www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.1, October 2025

Section	Change Summary
All	• Minor editorial fixes. • Added *LFMXO5-55TDQ*, *LFMXO5-20TD/Q* and *LFMXO5-30TD/Q* devices.
Abbreviations in This Document	Replaced *Acronyms* with *Abbreviations*.
Introduction	Removed a statement, *The device family consists of FPGA densities ranging from 14k to 53k logic cells*.

Power Supplies	• Updated Table 2.1. Power Supplies for LFMXO5-15D, LFMXO5-20TD/Q, LFMXO5-30TD/Q.
	  • Added *VSS, VSSSDx, VCCSDx, VCCSDCK, VCCPLLSDx, and VCCAUXSDQx.*
	  • Added *Bank 2* to power-on at 3.3 V only for Wide-Range banks.
	  • Added *LFMXO5-20TD/Q* and *LFMXO5-30TD/Q* devices.
	• Updated Table 2.2. Power Supplies.
	  • Added *VSS*, *VSSADC*, *VSSDX*, *VSSR*, and *VCCAUXSDQX* supplies.
	  • Added *Bank 7* to power-on at 3.3 V for Wide-Range banks.

Power Supply Filtering	• Added a statement, *Low noise LDO regulators for these rails is recommended.*
	• Updated Table 3.1. Recommended Power Filtering Groups and Components.
	  • Added *VSSR* supply.
	  • Added *Bank 2* to power-on at 3.3 V only for LFMXO5-15D, LFMXO5-20TD/Q and LFMXO5-30TD/Q.
	  • Added *Bank 7* to power-on at 3.3 V only for LFMXO5-55TD/Q.
	• Added *VSSR* and *note 2* in Figure 3.1. Recommended Power Filter.
	• Updated 3.2 Ground Pins section.
	  • Added *VSS*, *VSSSDX*, and *VSSADC.*
	  • Added a statement, *VSSR should be connected to ground through 1 kΩ resistor*.
	• Reworked the Clock Oscillator Supply Filtering section.
	  • Added Figure 3.2. Clock Oscillator Bypassing.

Configuration Considerations	• Added SSPI support.
	• Renamed Table 6.1 to Table 6.1. JTAG Pin Recommendations for LFMXO5-15D, LFMXO5-20TD/Q and LFMXO5-30TD/Q.
	• Added Table 6.2. JTAG and SSPI Pin Recommendations for LFMXO5-55TD/Q for SSPI pin configuration.
	• Split the Pull-up and Pull-down Recommendations Tables for LFMXO5-15D, LFMXO5-20TD/Q LFMXO5-30TD/Q, and LFMXO5-55TD/Q and created the tables below.
	  • Table 6.3. Pull-up/Pull-down Recommendations for Configuration Pins for LFMXO5-15D, LFMXO5-20TD/Q and LFMXO5-30TD/Q.
	  • Table 6.4. Pull-up/Pull-down Recommendations for Configuration Pins for LFMXO5-55TD/Q.
	• Removed old *Table 6.3 Configuration Pins Needed per Programming Mode.*
	• Removed old *Figure 6.2 Typical Connections for Programming SRAM/FLASH via I2C/I3C.*
	• Split the schematic diagram for LFMXO5-15D, LFMXO5-20TD/Q, LFMXO5-30TD/Q, and LFMXO5-55TD/Q and created the figures below.
	  • Figure 6.1. Typical Connections for Device Provisioning via JTAG for LFMXO5-15D, LFMXO5-20TD/Q and LFMXO5-30TD/Q.
	  • Figure 6.2 Typical Connections for Device Provisioning via JTAG for LFMXO5-55TD/Q.
	• Added Figure 6.3. Typical Connections for Device Provisioning via SSPI.
	• Removed *VCCIO_WR* of Figure 6.1, Figure 6.2, and Figure 6.3 and replaced by *3.3 V* only.

Section	Change Summary
Clock Inputs	• Added a statement, *For single-ended I/O's use only PCLKT pins as primary CLK pads*. • Moved the Clock Oscillator Bypassing figure to the Clock Oscillator Supply Filtering section. • Added the PLL Reference Clock Locking section.
Layout Recommendation	Replaced old *Figure 12.1 PCB Layout Recommendation* with Figure 12.1. Ground Vias Implementation and Figure 12.2. Stitching Vias Implementation.
Simulation and Board Measurement of Critical Signals	Added this section.
Checklist	• Added item 1.1.1, *VSSR connected to ground through a 1KOhm resistor*. • Added in item 1.2.1, *VCCIO2* to LFMXO5-15D, LFMXO5-20TD/Q and LFMXO5-30TD/Q. • Added in item 1.2.1, *VCCIO7* to LFMXO5-55TD/Q. • Removed in item 1.2.2, *Bank 2* from LFMXO5-15D, LFMXO5-20TD/Q and LFMXO5-30T/D/Q. • Removed in item 1.2.2, *Bank 7* from LFMXO5-55TD/Q. • Added in item 1.2.3, *LFMXO5-20TD/Q* and *LFMXO5-30TD/Q*. • Added item 1.6 *Reference Clocks*. • Added item 1.7 *Power Filtering Components*. • Added in item 3.1, Table 6.2 and Table 6.3. • Added item 5.5, *For single-ended I/O's use only PCLKT pins as primary CLK pads*.
References	Added Pinout files for *LFMXO5-55TDQ*, *LFMXO5-20TD/Q* and *LFMXO5-30TD/Q* devices.

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Section	Change Summary
All	Production release

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