Lattice Radiant 2024.1 Software Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant 2024.1 Software

- **Radiant Installer**
  - A new version of the Radiant installer has been uploaded to the Lattice website. Installing the latest 2024.1.0.34.2 version is recommended if you are currently using the 2024.1.0.34.1 version or older.
  - **Installation Instructions**

    Refer to the list below for the instructions to install the new version of the Radiant software. Also ensure that no instances of Radiant are running before attempting to install the new version.

    - **To install the new version on Windows:**

      1. Extract the zip file and navigate to the location where you want to save it.
      2. Double-click the 2024.1.0.34.2_Radiant.exe file to install the software.

    - **To install the new version on Linux:**

      1. Extract the zip file and navigate to the location where you want to save it.
      2. Execute the Radiant run file as follows:

         % cd <directory_with_RUN>

         % ./ 2024.1.0.34.2_Radiant_lin.run

If you are using Lattice Radiant 2024.1 (2024.1.0.34.1), refer to the instructions below.

- **To install the new version on Windows:**

  1. Uninstall Lattice Radiant 2024.1 (2024.1.0.34.1).
  2. Extract the zip file and navigate to the location where you want to save it.
  3. Double-click the 2024.1.0.34.2_Radiant.exe file to install the software.

- **To install the new version on Linux:**

  1. Uninstall Lattice Radiant 2024.1 (2024.1.0.34.1).
  2. Extract the zip file and navigate to the location where you want to save it.
  3. Execute the Radiant run file as follows:

     % cd <directory_with_RUN>

     % ./ 2024.1.0.34.2_Radiant_lin.run

- **Device Support:**
  - Lattice Avant™ (LAV-AT)
    - E70ES1 (-1/-2/-3) 0.82V (COM/IND) – LFG676, CSG841, LFG1156
    - Designs targeting the E70 device in 2023.2 or 2023.2.1 should now target the E70ES1 device.
    - For Avant products, this release supports targeting of silicon based on their release status. Refer to the following table for details.

2024.1 Designator	Status	Prior Designator
E70ES1	Engineering Sample	E70
E70B	Production	NA
E70	Early Access	NA

  - Certus™-NX (LFD2NX)
    - 9K (-7/-8/-9) 1.00V (COM/IND) – CSFBGA121
    - 28K (-7/-8/-9) 1.00V (COM/IND) – CABGA196, CABGA256, CSFBGA121

- **Tool and Other Enhancements:**
  - **License**
    - The version of Lattice license FlexNet utility and license daemon has been upgraded to v11.19.4.1.

      Note: Restart the license server after installing Radiant 2024.1 or obtaining the new FlexNet utility.

    - The new “LSC_RADIANT_3” RTL encryption key has been added to Radiant to prevent the encrypted RTL in 2024.1 from being used in earlier versions of Radiant.
  - **Radiant Installation Wizard**
    - The LATTICE_LICENSE_FILE and SALT_LICENSE_SERVER environment user variables have been added to the installation page.
    - The default Flexnet variable LM_LICENSE_FILE is now displayed on the installation page.
  - **Foundation IP**
    - JESD204B support has been added for the CertusPro-NX (LFCPNX) device.
    - The IP on Server tab in Radiant has been updated to support publishing of third-party IP.
  - **Strategies**
    - The “Read Write Check on RAM” LSE strategy has been added to Radiant strategy settings for Nexus and Avant devices.
    - Impose Hold Timing Correction strategy has been added to the Radiant Place & Route strategy settings.
  - **Block-Based Design**
    - The Block-Based Design feature now supports Lattice Synthesis Engine (LSE).
    - Isolation Design Flow has been added to Block-Based Design. This new feature allows you to create prohibited regions that excludes any logic or routing from the rest of the design.
  - **Design Rule Checking** – DRC has been updated to generate a report which specifies any combinational loops or clocks that have been identified and connected to black box modules.

- **Simulation**
  - Radiant software now includes QuestaSim™ Lattice OEM Edition for simulation, debugging, and verification processes. The ModelSim simulator has been replaced by this new tool.
  - Since QuestaSim is a 64-bit application, it can support designs whose memory usage is greater than 4GB during simulation.
  - To be able to use the new QuestaSim Lattice FPGA edition on Radiant 2024.1, you need to regenerate your license from the website.
- **Power Calculator**
  - Watt values in Power Calculator reports are rounded off to 3 digits after the decimal point.
  - When using Avant, the Power Screen field is available for selecting power screen options based on device license.
- **Disable Message Tcl Command** – Warning and info messages can now be disabled using the msg_disable Tcl command.
- **Programmer** – "Verify feature row" and "Verify lock policies" operations for generating VME have been added to Programmer.
- **Reveal**
  - Reveal Inserter provides the option to choose between the standard RTL (Pre-Synthesis) and the Post-Synthesis debug flows. Post-synthesis debugging allows easier monitoring of debug signals and the insertion of debug logic after a design has been synthesized.
  - Configuring User Memory Setup section has been updated.
  - When debugging a JTAG chain, bypass instruction can be used to select or isolate specific devices to debug or to skip.
  - In the Eye Diagram interface, "Unit Interval" has been changed to "Phase Step" and "Voltage" has been changed to "Vertical Step".
- **IP Packager** – New Tcl commands have been added for IP Packager.
- **Export Files** – Gate-level simulation and IBIS files are set to "Disabled" by default in creating a new project.
- **Tool Options** – Centralized management for individual and group settings is now supported in Tool Options.
- **Timing Constraints**

- The Timing Analyzer now supports set_false_path -setup and -hold options.
- Generated clocks now include -add and -master_clock parameters.

- **Timing Tcl Commands**
  - All sta_report_timing commands now support the -file and -app options. The -file command saves the result to a file whose name is provided after the -file option, and the -app flag informs the command to append the report instead of overwriting the file.

- **Hardware Data File**
  - The DDR delay code settings has been updated for the MachXO5-NX (LFMXO5) device.
  - CertusPro-NX (LFCPNX)
    - Differential 100ohm termination for input differential IO types has been added to the CertusPro-NX (LFCPNX) .ibs file.
    - On-die termination (ODT) support for input and bidirectional models have been fixed for CertusPro-NX (LFCPNX) IBIS models.
  - Hard DPHY now captures the rising edge of the byte clock of u_txwordclkhs (UTWDCKHS).

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, it may be necessary to re-create some IP, per the procedures described in the following table.

These procedures adapt the project for the changes in Radiant software.

Versions	IP			IP Regeneration Procedures
	Avant (LAV-AT-E)	**CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP), MachXO5-NX (LFMXO5)**	**iCE40UP**	
2024.1	DDR Generic	DDR Memory		These IP used in designs created in Radiant 2023.2.1 or earlier must be regenerated in
	DDR 7:1	PLL		
	SDR	SDR		
	PLL	Barrel Shifter		
	DDRPHY	FIFO		
	MIPI DPHY	FIFO_DC		
	MPPHY	RAM_DP		
	SEDC	RAM_DP_True		

Versions	IP			IP Regeneration Procedures
	Avant (LAV-AT-E)	**CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP), MachXO5-NX (LFMXO5)**	**iCE40UP**	
	Barrel Shifter	RAM_DQ		Radiant 2024.1.
	FIFO	ROM		
	FIFO_DC			
	RAM_DP			
	RAM_DP_True			
	RAM_DQ			
	ROM			

The following server IP are not compatible with Radiant 3.0 onwards. Use the latest versions of the IP available on the IP server:

- I2C Master version 1.0.3
- UART 16550 version 1.0.4
- DDR3 SDRAM Controller version 1.1.1
- DDR3 SDRAM Controller version 1.2.1
- LPDDR2 SDRAM Controller Lite version 1.1.1
- LPDDR2 SDRAM Controller Lite version 1.2.1

Supported Devices

Lattice Radiant software can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
iCE40 UltraPlus (iCE40UP)	◀	
Lattice Avant (LAV-AT-E)		◀
CertusPro™-NX (LFCPNX)	Evaluation Mode	◀
Certus™-NX (LFD2NX)	◀	
MachXO5™-NX (LFMXO5)	Evaluation Mode	◀

Device Family	Free License	Subscription License
CrossLink-NX (LIFCL)	◄	
Certus™-NX-RT (UT24C)		RT Subscription
CertusPro™-NX-RT (UT24CP)		RT Subscription

Support for Third-Party Synthesis and Simulator Tools

The Synopsys Synplify Pro® for Lattice synthesis tool and the Siemens QuestaSim® Lattice Edition simulator tools are included in the Radiant software.

- **Synopsys Synplify Pro FPGA synthesis software version V-2023.09LR-1**
  - Release Notes for Synplify Pro are located in ..\<*install_directory*>\radiant\2024.1\synpbase\doc\. The file name is release_notes.pdf.
  - A full set of documents for Synplify Pro are also located in \<*install_directory*>\radiant\2024.1\synpbase\doc\.
- **Siemens QuestaSim Lattice Edition 2024.2**
  - Release Notes for QuestaSim Lattice Edition are located in <install_directory>\radiant\2024.1\questasim\.
    The file names are RELEASE_NOTES.html or RELEASE_NOTES.txt.
  - A full set of documents for QuestaSim Lattice Edition are located in <install_directory>\radiant\2024.1\questasim\docs\pdfdocs.
- **Siemens Questa® 2022.3**
- **Cadence Xcelium® 24.03.003**
- **Synopsys VCS® U-2023.03-SP2**

Help Resources

- Online Help updated with CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP), and Lattice Avant (LAV-AT) content.
- To view the Online Help, start the Lattice Radiant software and select the  “Getting Started” icon under Information Center.

  Note: The Firefox Snap install is not supported if you are using Ubuntu 20.04 or 18.04 to access the Radiant Help. This is a result of the snap install's inability to open local HTML pages. You may reinstall the latest version

of Firefox using Apt install. For installation instructions, please refer to this guide.

System Requirements

The following shows the basic system requirements for Radiant software:

- Intel x86 64-bit or 64-bit-compatible PC
- OS Support:

64-bit OS	Radiant	Synplify Pro	QuestaSim
Windows 10	✓	✓	✓
Windows 11	✓	✓	✓
Red Hat Enterprise Linux 7.9	✓	✓	✓
Red Hat Enterprise Linux 8.8	✓	✓	✓
Ubuntu version 20.04 LTS	✓	✓	✓*
Ubuntu version 22.04 LTS	✓	✓	✓*
CentOS 7.9	✓	✓	✓*

***Note**: The third-party tools have been tested by Lattice on the listed platforms, but the vendors do not officially support them.

- Approximately 50 GB free disk space
- Computer Memory Requirement:
  - Nexus – 16GB
  - Avant – 32GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.
- 1024 X 768 graphics display
- Network adapter for license and network connectivity
- A Web browser with JavaScript capability
- Acrobat Reader

Issues Fixed in this Release

The following known issues are fixed in this release. Their workarounds are no longer needed.

Deployment tool generates blocks in a way that causes issues in some cases for ping pong boot.

Devices affected: All devices

Bug number: DNG-21418

Programmer encounters issues when three HW-USB-2B Cables are connected.

Devices affected: All devices

Bug Number: DNG-21262

Map encounters an error on dual-rank LPDDR4 Memory controller when running Radiant Flow

Device affected: CertusPro-NX (LFCPNX)

Bug number: DNG-20832

LMMIRDATA port does not output data correctly during RTL simulation of CONFIG_LMMIE.

Devices affected: MachXO5-NX (LFMXO5-100T)

Bug number: DNG-20666

Synplify Pro infers unsupported primitive "SP16K_1" during synthesis for CrossLink-NX.

Device affected: CrossLink-NX (LIFCL-33U)

Bug number: DNG-20643

RAM_DP_True outputs zeroes and does not retain data from address 800h during certain transactions.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20532

Create_generated_clock constraint may be overwritten by Synplify pro, changing the destination clock path.

Devices affected: All devices

Bug number: DNG-20228

Unexpanded interface port error during synthesis with Synplify Pro for some designs using the System Verilog interface construct.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-19872

"Identifier not declared" error encountered during simulation with VCS in encrypted lmmis_init_fsm.v file.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-19861

You may encounter the following limitations when using SEI Editor on different devices.

1. **Nexus devices (LIFCL-17K, LFD2NX-17K, and LFMXO5-25K) cannot support SEI 2-bit with Unused strategy for combinations such as EBR-EBR or DSP-DSP.**
2. **The requirement for SEI 2-bit is that both error bits should be in the same data frame. The data frame corresponds to the FPGA column with reference to the "array" architecture.**
3. **In Nexus architecture, any device with a density less than 30K has only 1 EBR or 1 DSP per column. Due to this limitation, it cannot support multiple error injection on an EBR or DSP site for these densities.**
4. **However, those device densities can support SEI 2-bit Random strategy combinations and SEI 2-bit PFU-PFU combination with Unused strategy.**

			Nexus	
SEI	**1-bit**	**2-bit**	**Density >= 30K**	**Density < 30K**
Random	Supported	Supported		
Unused	Supported	Supported	EBR-EBR	PFU-PFU
			DSP-DSP	
			PFU-PFU	

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-19715

Post-route simulation error when using GDDR for Avant devices due to parameters not being passed correctly from the original RTL.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-18794

Synplify Pro implements RAM using LUTs instead of EBRs for certain Lattice RISC-V IP on Avant.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-18479

"Not user declared module (VERIFIC_AND)" error during post-synthesis when using LSE when the modulus operator is used in RTL.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-16713

Known Issues for Radiant 2024.1

The following are known issues for the Radiant Software 2024.1. For assistance with these issues, please contact Lattice Technical support.

Combinational loops are inferred within hub2lmmi_inst when Reveal is added. It does not impact the general functionality of Reveal.

Devices affected: All devices

Bug number: DNG-21798

Synplify Pro incorrectly removes virtual wire signals that were preserved using the "syn_rvl_debug" attribute.

Devices affected: All devices

Bug number: DNG-21236

QuestaSim simulation fails for DDR5 IP due to undeclared Micron model packages.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-21086

Synplify Pro does not report an error or warning for clocks that are driven by logic.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-21048

The PDPSC32K primitive does not have an output path despite outreg being used.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20772

You may encounter an issue with CONFIG_LMMI and CONFIG_LMMA's lmmi_ready signal during simulation.

Devices affected: Certus-NX (LFD2NX), CrossLink-NX (LIFCL)

Bug number: DNG-20717

CONFIG_LMMI RTL simulation error occurs and data missing in output ports.

Devices affected: Certus-NX (LFD2NX), CrossLink-NX (LIFCL)

Bug number: DNG-20543

Synplify Pro does not correctly process macro creation constraints with escape characters.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-20134

When using Synplify Pro, you may encounter the following error during macro reuse: “Synthesis exit by 9. Child process exited abnormally. Done: error code 1.”

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20116

IBIS reports I/O models of some sysCONFIG pins even if they are used as GPIO.

Workaround: Remove duplicated pins in IBIS file.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19646

Simulation with XCELIUM may fail when simulating projects using the CNTL_LR_U_POWER primitive due to incorrect compilation order of cmpl_libs.

Devices affected: CrossLink-NX (LIFCL-33U)

Bug number: DNG-19623

Cannot assign input ports as MIPI_DPHY type for Avant.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19199

Reveal Power-on Reset (POR) Debug function does not work when using LSE with only one Trigger Unit (TU).

Workaround: Add another Trigger Unit (TU) that can be unrelated to POR Debug.

Devices affected: All devices except iCE40UP

Bug number: DNG-13901

The CSI-2/DSI D-PHY Transmitter and Receiver Soft IP simulations fail when using Synopsys VCS as simulation tool.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-13225

Post-route simulation error when using GDDR for Nexus devices due to parameters not being passed correctly from the original RTL.

Workaround: Intrinsic delay similar to the delay value on the vo.vo file needs to be added to the IP testbench.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-9639

MAP incorrectly reports number of DPHY and PCIE/ADC resources for CrossLink-NX (LIFCL) QFN72 package.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-8297