Product Bulletin

May 2024 **#PB240501 Rev 1.0**

Use of SED with Distributed RAM in the Lattice Nexus FPGA Platform

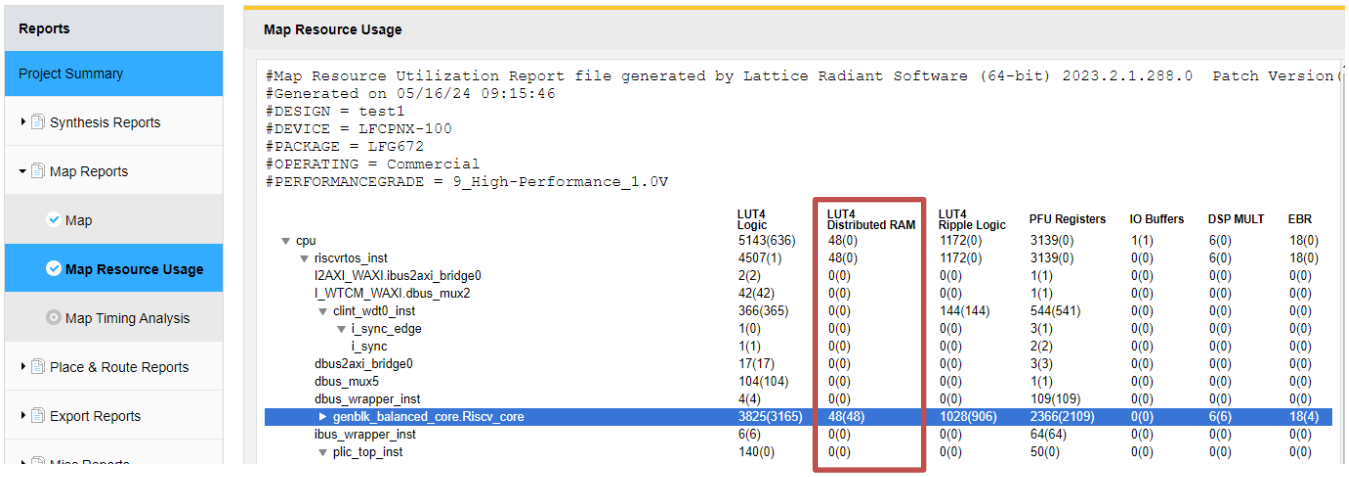
Purpose: This product bulletin supplements the use of the SED (Soft Error Detection) function available in the Lattice Nexus FPGA platform as described in FPGA-TN-02076-1.9.

Product Affected: Lattice Radiant software release 2023.2 and earlier releases that support the Nexus platform (CertusPro-NX, Certus-NX, CrossLink-NX, MachXO5-NX FPGA families) are covered by this Product Bulletin.

Customers Affected: Designs that are using SED together with Distributed RAM and/or Reveal Analyzer.

Observation: Lattice found that there is an issue in Radiant versions prior to Radiant 2023.2 SP1 whereby the use of SED together with distributed RAM (LUT RAM) may result in a false SED error.

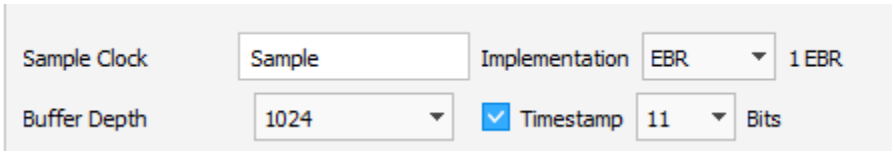
Detailed Workaround Description: The use of Distributed RAM in the design is reported in the Radiant Map Resource Usage Report.



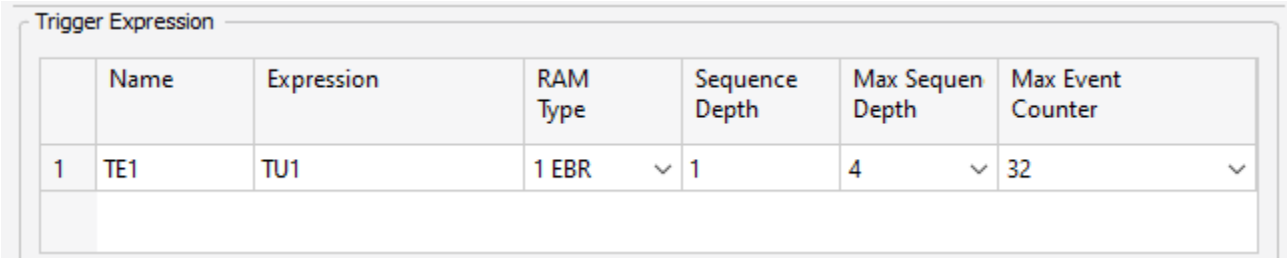
If distributed RAM is used in the design, there are four separate workarounds that can be used to avoid this issue.

1. Restrict the use of SED together with Reveal.
   The SED can be used together with Reveal if there is no Distributed RAM used by Reveal. The use of distributed RAM in Reveal can be avoided by following steps a and b below.

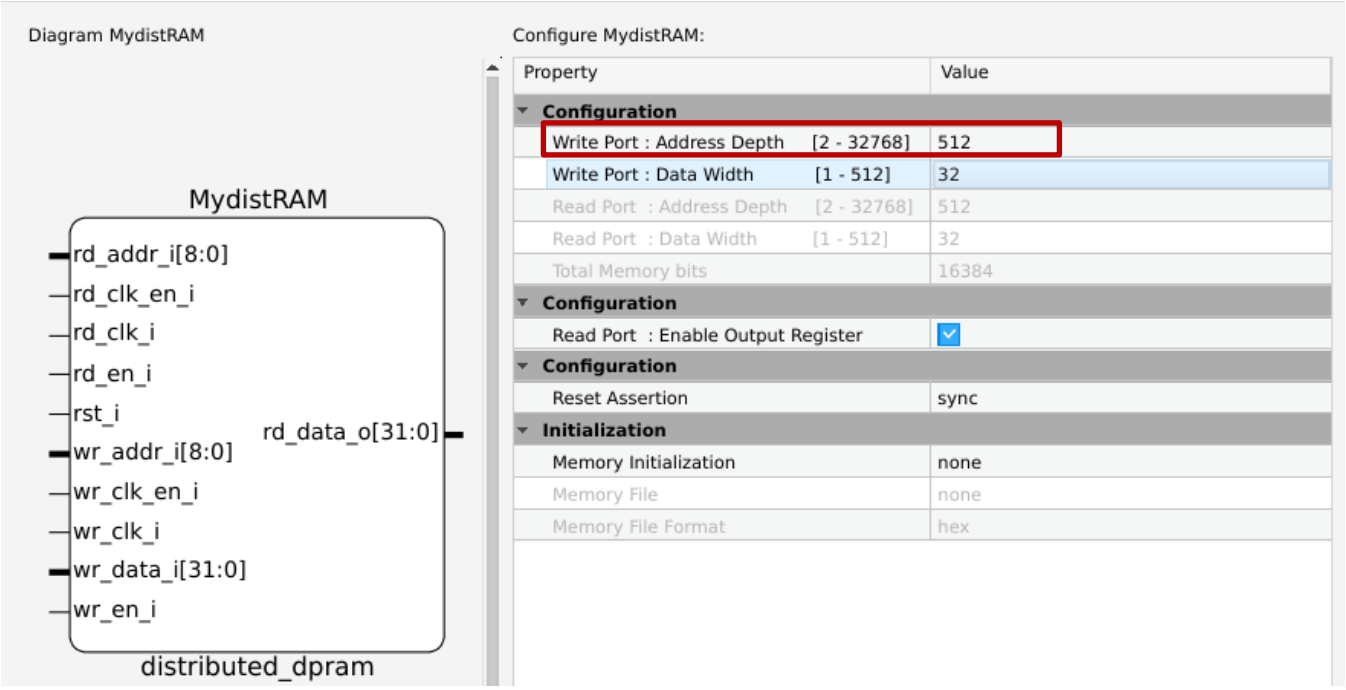
   a.) Reveal Inserter Implementation must be set to EBR and NOT Distributed RAM



b.) All trigger expressions must be set to all EBR. Do not use Slices.



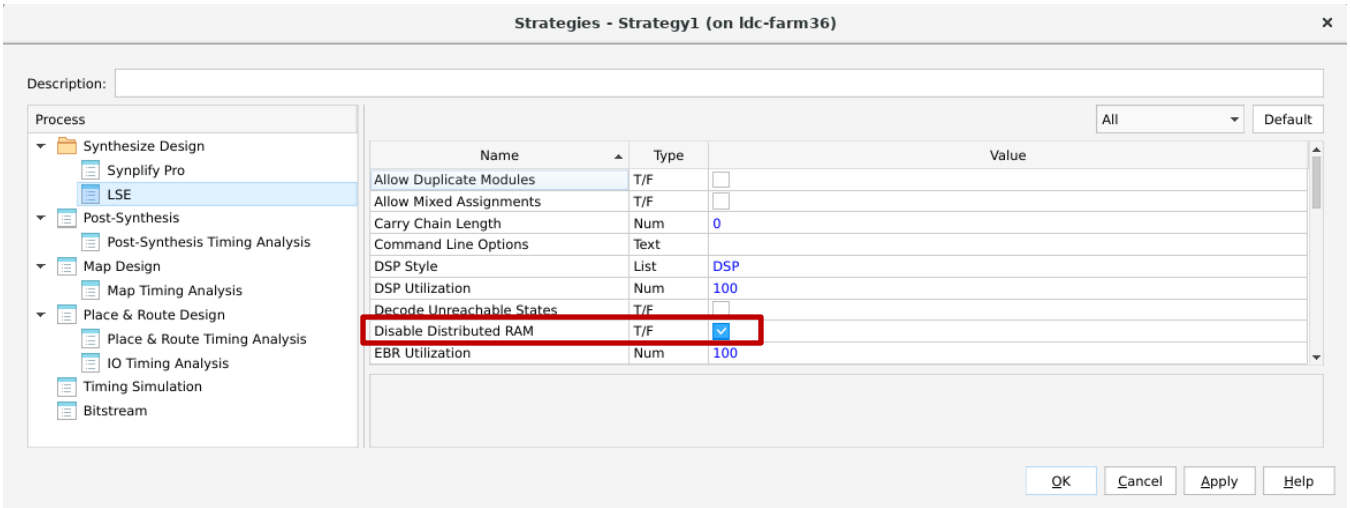
2. Only use SED on Distributed RAM that has data widths that are multiples of 4.
   If inferencing Distributed RAM, ensure the data width is a multiple of 4, e.g. 4, 8, 12, 16, etc.
   If instantiating a RAM primitive, e.g. Distributed_DPRAM, Distributed_ROM, or Distributed_SPRAM, only use data widths that are multiples of 4.



Note: If the design includes Lattice or 3rd party IP that uses Distributed RAM that has data widths that are not a multiple of 4, please contact Lattice Technical Support.

3. Prevent the use of SED together with Distributed RAM in the design.
   If you are using Synplify Pro or LSE for synthesis, do not use the syn_ramstyle = “Distributed” attribute when inferring RAM inference in your design.
   You can force the use of Block RAM in the design by using the syn_ramstyle = “block_ram” attribute in your RTL. This will map the RAM to EBR resources.

Alternatively, if you are using LSE(Lattice Synthesis Engine) for synthesis, you can prevent the use of Distributed RAM in the design by selecting the Disable Distributed RAM option in the LSE Strategy settings.



Note: If the design includes Lattice or 3rd party IP that uses Distributed RAM that has data widths that are not a multiple of 4, please contact Lattice Technical Support.

4. Use Radiant 2023.2 SP1 or a later release of Radiant.

Revision History:

Date	Version	Description of Revisions
May 31, 2024	1.0	1st Release