Upscale Your Product and Rebuild Business Resiliency – Migrating to Lattice FPGAs

A Lattice Semiconductor White Paper.

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1. Introduction

Nothing is certain and businesses still need to flourish regardless of all the uncertainties. Hence companies continue to invest heavily in their business continuity and business resilience strategies. Unfortunately, at times, even the best business resilience strategies can get disrupted due to supplier actions just like the recent announcement by AMD on discontinuing some of their FPGA families.

Such disruptive events from FPGA vendors will trigger an initial response from your business organization. The recovery strategy can be to quickly get to prior state of normalcy. But more strategic and resilience-centric organizations will optimize this disruptive event to create a new normal for their business.

Business Continuity And Business Resilience

Business as usual	Event	Business Recovery Actions		Business Normalcy
	Disruptive event like EOL of AMD parts	Initial business response	Recovery activities E.g. Engaging with partner like Lattice for quick resumption	Return to normalcy OR Create a new normal for your business
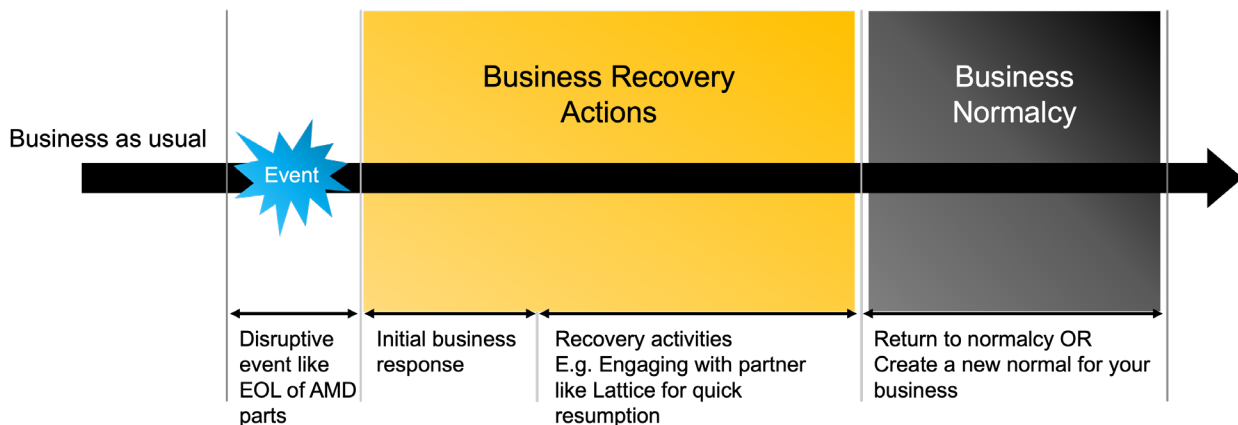
Business continuity is typically defined as the capability of an organization to continue the delivery of its products or services at acceptable predefined levels following a disruption. Whereas business resilience is more about the ability of an organization to absorb and adapt, survive, and prosper in a changing environment and enable it to deliver its goals. Business continuity is mostly process centric whereas business resilience is more strategic.

For any successful business resilience strategy, robust supply chain is one of the main requirements. Companies have built resilient and agile supply chains that allow them to forecast, anticipate, and respond efficiently to risks and opportunities. Any disruption in supply chain needs to be addressed promptly. The EOL of AMD parts is one such instance of impending supply chain disruption.

Besides disrupting your supply chain, such disruptions can impact your revenue streams and profit margins, both in short and long term. It also puts a burden on your engineering teams to migrate your products to new FPGA devices and get business back to normalcy.

Rebuilding Supply Chain Resiliency: Selecting The Right Partner

The decision of choosing the right FPGA partner is critical. It involves evaluating options to improve product features, assessing competitive landscape, analyzing impact on engineering costs, product pricing, margins, time to market (TTM) and securing your supply chain. It is vital to holistically look at all these factors in the process of rebuilding your supply chain resiliency.

Additionally, design migration, the next step in this process, can be complex.
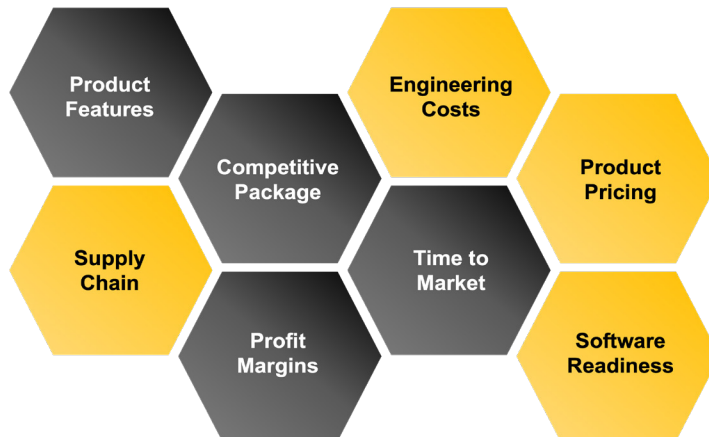
Lattice have created a couple of programs to mitigate the irksome complexity of migrating your products from EOL AMD devices to Lattice FPGAs. As a part of these programs, we work with our partners and customers to rebuild their supply chain resilience and ease their design migration journey.

The focus of this document is to outline the overall design migration workflow and highlight some key benefits of migrating to Lattice devices.

This paper starts with an overview of the essential factors that need to be considered before starting the design migration process. The next section provides some example Lattice devices that can effectively replace the EOL AMD parts.

The subsequent sections investigate key points related to design migration workflow. I.e.:

- HDL design migration: AMD ISE to Lattice Diamond™ and Lattice Radiant™ tool suite
- Mapping device features
- Board schematics and layout
- Timing & constraints
- I/O Mapping
- Programming/Configuration
- Embedded design migration

The summary section outlines the programs offered by Lattice to help in the overall design migration process and rebuilding business resilience.

2. The First Step: Factors to Consider for Migration

AMD recently announced that it is discontinuing some of their FPGA product families that includes XC9500XL™, CoolRunner™ XPLA™ 3, CoolRunner II, Spartan™ II, and Spartan 3, 3A, 3AN, 3E, 3ADSP Commercial/ Industrial "XC" and Automotive "XA" Product Families. The first step, before getting into details of choosing a replacement FPGA device, is to evaluate some key factors for product migration. Some of the factors are:

- Power
- Performance (or Performance per watt)
- Board design
- IPs
- Engineering costs
- Robust supply chain
- TTV (Time to Value) and
- TTM (Time to Market)

Let's explore why these factors are important and how Lattice FPGAs can help to upscale your products as you migrate the designs from EOL AMD parts to Lattice FPGAs.
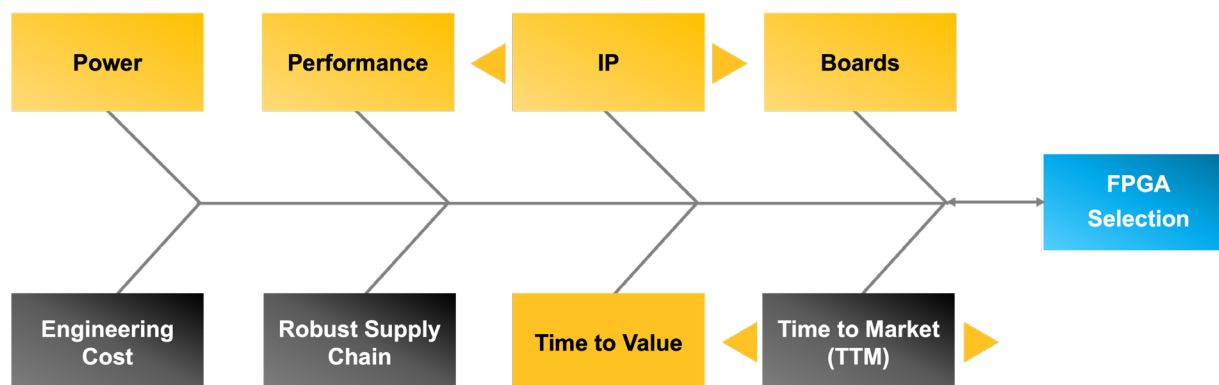
Factors To Be Considered for FPGA Selection

Some factors can involve board migration, functional equivalence with previous design, and how extensive changes are needed to firmware and software with a replacement FPGA. These factors are non-trivial and requires strong technical collaboration with FPGA vendor. We will explore some of them in a bit more detail.

Power: For almost all products, power is one of the main differentiating features. Power savings can be achieved through multiple aspects of FPGA development. For example: choice of FPGA device, design architecture, choice of IPs, thermal solutions and overall board design. Selecting the right low power FPGA is essential to get low power differentiation. Lattice is low power programmable leader and by selecting devices from Lattice, your products can have the best-in-class power savings.

Performance (or Performance per watt): This is the most common product differentiator. Achieving the best performance is a strong function of the design architecture, capability of the FPGA device and the software tool suite. You can achieve the best performance per watt when you use low power FPGA devices from Lattice and utilize Radiant or Diamond software tool suite that provides all the necessary features to achieve the best possible performance for your design.

Board design: This requires a little more thought.

- For some products, you may choose not to overhaul the board design and maintain the stability of your supply chain for all non-FPGA board components. In such cases, it is important to find a replacement FPGA device that will cause minimal disruption to your board design.
- Then there are products for which you may decide to upscale them and are okay with overhauling your board design. The long-term benefits of additional revenue and better margins is worth the effort of re-normalizing your supply chain.

In both the cases stated above, it is critical to find a FPGA provider like Lattice who can support and expedite the board redesign efforts. Our strong applications team can guide you through the process of partial or complete board redesign.

IPs: The key criteria for IP migration can be matching power/performance specs, achieving same level of functionality, and ability to fit in the FPGA programmable core. You may have two possible scenarios when it comes to IPs.

- There is no proprietary or 3rd party IPs that are used in your EOL AMD device. This implies that the IP migration strategy will primarily involve mapping the IP functionalities to Lattice primitive or macro IPs.
- The design uses proprietary and/or 3rd party IPs. In such a scenario, some focused effort may be required to migrate the functionality to an equivalent Lattice IP.

We understand the complexities associated with both scenarios and our Apps team at Lattice is well positioned to support your IP migration effort.

Engineering costs: Complexity of the design, familiarity of the engineering team with the FPGA tools and flows, and availability of engineering resources are key considerations when evaluating the total engineering costs.

We understand these challenges and hence we have created collaterals and trainings that will make migration from ISE to Lattice's Diamond and Radiant tools as easy as possible. We can work closely with your engineering teams to ensure that the engineering efforts during the migration process are optimized.

Robust supply chain: It is critical to look beyond the immediate stop-gap solutions and focus on long term strategy for the product's supply chain. The FPGA devices should be available without any disruption for next 10+ years and it should also have a strong roadmap for the future. Let's explore the pros and cons of making a decision to make a large LTV (Lifetime Value) from AMD or redesigning with a Lattice FPGA.

The benefit of making a large LTV buy is re-engineering cost savings. But on the other hand, there are few downsides:

1. Risk of having large left-over scrap inventory with an over-buy OR risk of upsetting customers who can't obtain the products in case of under-buy as there is an inherently high uncertainty when buying for either 5, 10, or 15 years of inventory
2. The NPV (net present value) of cash spent in buying a large inventory from AMD is much more expensive compared to the lower engineering cost in migrating the design
3. There is also a huge opportunity cost associated with locking the cash in inventory

Meanwhile there is some amount of engineering cost and time associated with migrating the design to a Lattice FPGA,. But there is significant upside in terms of less overall cost compared to last-time inventory buy and building a resilient supply chain.

Lattice is committed to providing a robust supply of our devices and there is a strong roadmap of future devices that will help future-proofing your overall product strategy.

Time to Value (TTV): This is a key metric that is typically used to determine whether a product or service is worth buying. It is measured in terms of how long it takes to recognize the value of the product or a service. Hence, as a part of these migration programs, we work with our customers to evaluate the TTV once they express their interest in migrating to Lattice device. As an example, it can be the time taken by your engineering team to migrate your design from EOL AMD device to FPGA device once you receive the Lattice evaluation boards.

Time to Market (TTM): This is probably one of the topfactors that needs to be assessed. TTM can be expedited by getting your migration design done right the first time. It includes board schematic and layout redesign, meeting power and performance goals, signing off on timing and functional correctness.
As a part of the migration programs, Lattice's Apps team can assist you in reducing your TTM.

3. A Typical Design Migration Workflow

Design migration involves many steps and it can involve multiple engineering organizations. The flow chart below shows a typical design migration workflow. The intent is to help customers in planning and scoping the overall effort. Additionally, Lattice support is available to assist with each step of the workflow.

Typical Design Migration Workflow
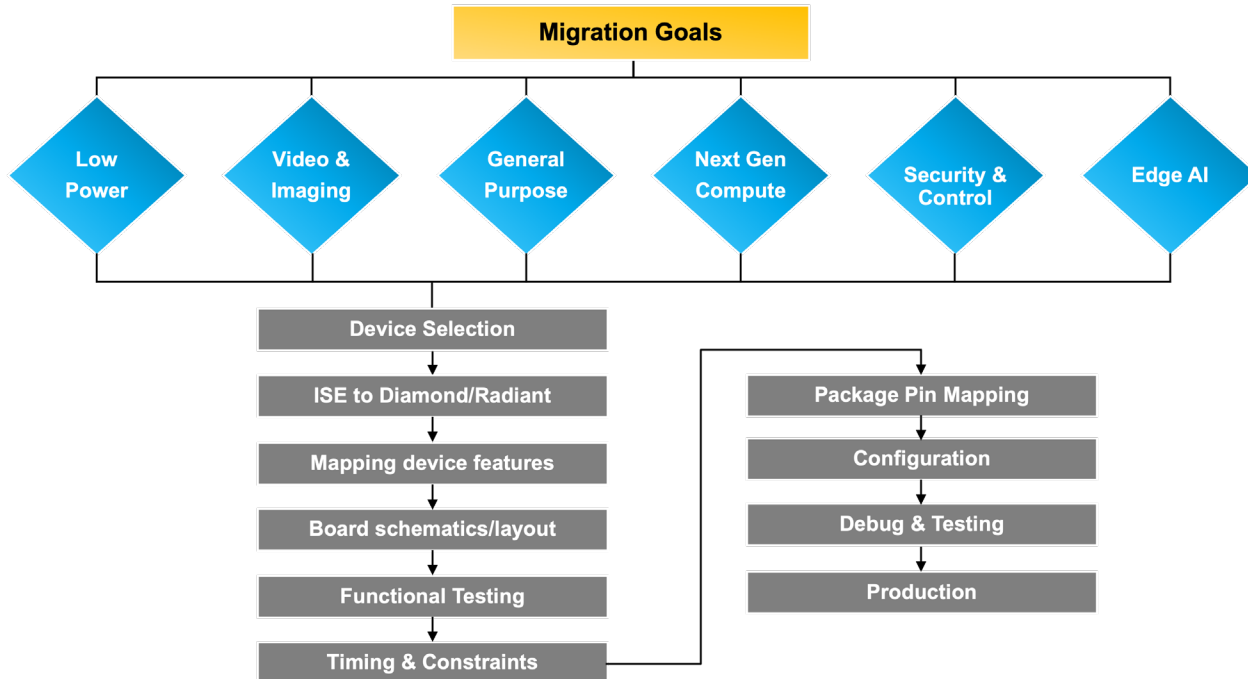
The first step in the workflow requires establishing the migration goals. It includes identifying the primary target market for your product (e.g. Video & Imaging, Security and Control, or Edge AI). Device selection is the key second step in this workflow. Once these two steps are completed, there are a series of engineering efforts that are needed to get your product into final production.

The next sections briefly go over some of the important steps.
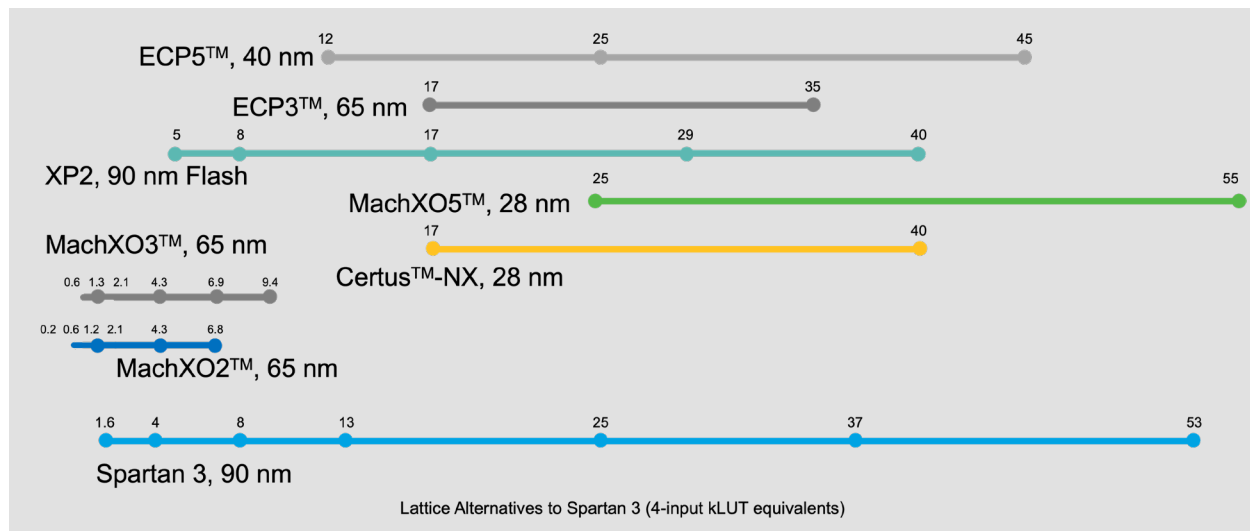
4. Device Selection

Once all the factors mentioned in the previous sections are considered, the next step is to select an appropriate device for migration. These EOL parts land right in the sweet spot of Lattice's FPGA portfolio. As an example, the chart shows a broad range of Lattice FPGA devices that are available for migration from EOL AMD Spartan devices. These device families provide a wide selection of power, features, size, and robust supply chain.

Some examples:

- Low power leadership: If the key goal is to drive low power leadership for your product, one of the low power devices from Lattice can be a great candidate.
- Security features: To upscale the product with new security features, the Lattice Mach™ FPGA family is a great choice.
- Embedded flash: Lattice Mach FPGA family has embedded flash that can help save board and BOM costs. It can also open other use cases for your products.

Lattice Devices for Replacing EOL AMD Spartan 3 Parts

ECP5™, 40 nm — 12, 25, 45
ECP3™, 65 nm — 17, 35
XP2, 90 nm Flash — 5, 8, 17, 29, 40
MachXO5™, 28 nm — 25, 55
MachXO3™, 65 nm — 0.6, 1.3, 2.1, 4.3, 6.9, 9.4
Certus™-NX, 28 nm — 17, 40
MachXO2™, 65 nm — 0.2, 0.6, 1.2, 2.1, 4.3, 6.8
Spartan 3, 90 nm — 1.6, 4, 8, 13, 25, 37, 53

Lattice Alternatives to Spartan 3 (4-input kLUT equivalents)

If you are planning to use this opportunity and completely overhaul the product, Lattice FPGA devices built on the Lattice Nexus™ platform can be ideal. It provides best-in-class performance per watt, strong portfolio of IPs, and a suite of reference designs that can fast-track your design migration process.

## 5. HDL Design Migration: AMD ISE to Lattice Diamond and Lattice Radiant

Most customers are rightly concerned about the effort needed to migrate from one tool chain like ISE to a new tool flow like Lattice Diamond or Lattice Radiant. The effort needed to migrate the HDL code to a new tool can seem daunting. There are also worries related to timing constraints, identifying IPs and primitives that needs to be migrated, and compiling the design to generate the final bitstream.

These are indeed important issues and if they are not planned correctly, it can quickly become a tedious engineering effort. We have created collaterals and tools to make this process more efficient and handle some of the idiosyncrasies associated with HDL design migration.

Some of the collaterals are listed below. They can be requested through your sales or FAE partners at Lattice.

■ Python scripts to automate the first step of migrating your ISE project over to Diamond or Radiant tool project.
■ Document with a step-by-step walkthrough of the following steps in design cycle:
  ■ Project creation and management
  ■ Design entry
■ Implementation flow
■ Programming/Configuration
■ Training modules on Lattice Insights and
■ Hands-on labs

At its core, a hardware description language (HDL) code of the register transfer level (RTL) can be imported into one of Lattice's design software and then configured to one of Lattice's FPGA.
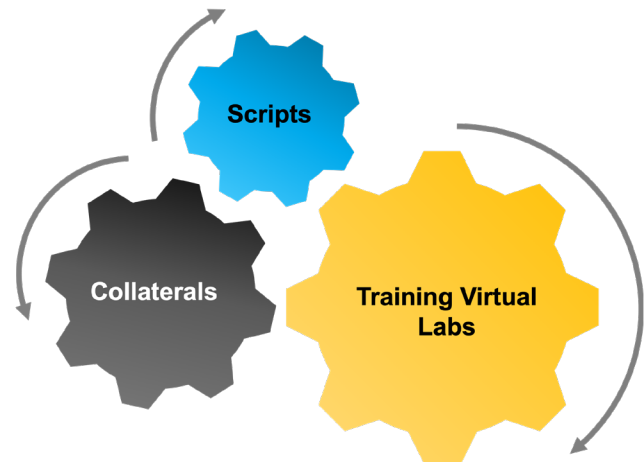
6. Mapping Device Features

The next step is to map the features from the EOL AMD part to the selected Lattice FPGA device. To accomplish this task, it is imperative to understand the silicon, architectural and electrical compatibility between the two devices.

To quickly enable our customers, Lattice has created a detailed document that highlights some key mapping guidelines from EOL AMD part to Lattice FPGA. For example, the Spartan3-A to ECP5 mapping App Note is available upon request.

Let's quickly highlight some of the key architectural and silicon features that needs to be considered.

■ PLB (Programmable Logic Block)
■ Embedded RAM
■ PLL
■ Clocks
■ DSP
■ Configuration
■ SERDES
■ Packages
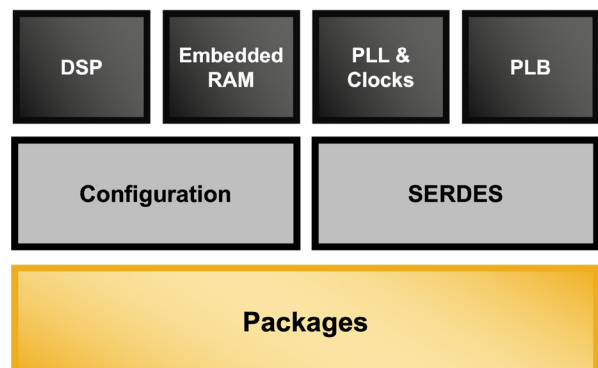
PLB (Programmable Logic Block): This is the programmable portion of the device that typically consists of LUT (Look-up tables), registers, and distributed RAM.

Embedded RAM: This is a critical component for many products and Lattice's devices provide multiple options. As an example, RAM is designed to work as Single-Port RAM, Dual-Port RAM, Pseudo Dual-Port RAM, Shift Register, and ROM memories. FIFO mode is available to implement Single and Dual clock modes.

PLL: This macro directly impacts the quality of overall clocking scheme and system jitter. For instance, the ECP5 part has 4X PLL/DLL and has an input range from 8-400 MHz with a lock time of 15 ms.

Clocks: Mapping of the clock schema requires understanding of the clocking features and resources available on the Lattice device. For example, the a FPGA device clock tree can have 64 clock inputs and global clock trees across 4 quadrants.

DSP: As the edge AI use cases are quickly getting proliferated in today's new products, DSP resources become critical part of your design migration strategy. Depending on the Lattice device selected for migration, the DSP IP can offer many best-in-class features for upscaling your product.

As an example, Lattice's DSP IP as strong multiplication support and dedicated architectural features that enable efficient implementation of machine learning, wearable, mobile, video, and other DSP-intensive applications. It has dedicated input shift registers, dedicated pipeline registers, and cascaded DSP to support multi-tap FIR/IIR implementation.

Configuration: Depending on the product, it is important to map the required configuration features from EOL AMD part to selected Lattice FPGA. For instance, mapping the master mode, slave mode and JTAG mode to the new device. Similar exercise is needed for pin mapping for the respective configuration modes.

SERDES: Since none of the EOL AMD parts had SerDes capabilities, this is a great opportunity to consider adding this feature to your product during this design migration effort. Adding SERDES to your product can provide great flexibility to implement new applications and achieve significant performance gains.

Lattice has a strong history of enabling their customers with high speed SERDES solutions and expedite their TTM. Please reach out to your sales partner for more details.

Packages: Selecting the right package is critical since it will directly impact the amount of effort needed to redesign the board schematics and layout. Lattice offers multiple options for packages depending on the FPGA device selected to replace the EOL AMD part.

7. Board Schematics and Layout

Another key aspect for a successful design migration effort is correct-by-construction board redesign. If done correctly, it can significantly reduce the TTM for your products. It typically may involve evaluating your power tree architecture, operating conditions, board components, power supply requirements, and power and/or signal integrity requirements.

An efficient way to get started is by ordering an evaluation board for your chosen FPGA device. With minimal lead time on delivery and comprehensive list of collaterals, we can quickly enable your board design team.
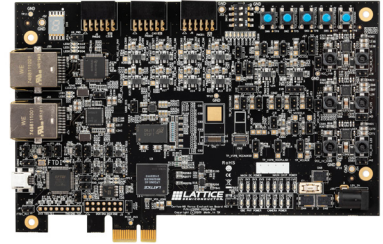
Some snapshots of evaluation boards from ECP5, MachXO5 and Certus-NX devices are shown below. More details are available on Lattice website or through your Sales/FAE partners.
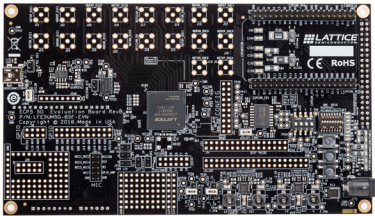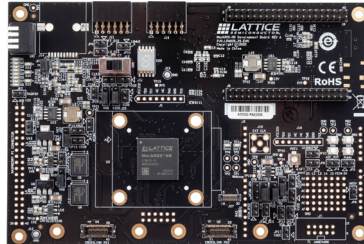

| ECP5 | MachXO5-NX | Certus-NX |

8. Timing and Constraints

One of the significant engineering efforts for most customers is migration of timing constraints and achieving timing closure. At Lattice, we have created documentation and trainings that can help expedite the constraints migration and timing closure process.

As an example, the picture below shows the constraints flow in Diamond. There are some subtle differences between the ISE and Diamond constraints flow.
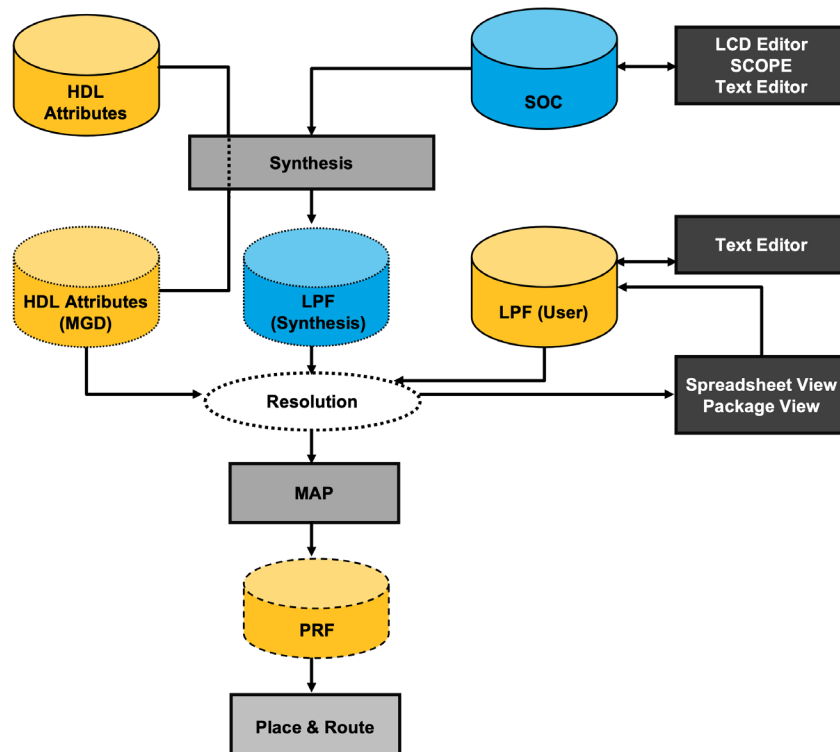
The table below shows most used timing Preferences and it's equivalent Diamond preferences. Diamond software help has detailed description of each of these preferences.

ISE Constraint	Constraint Function	Diamond Equivalent Preference
FAST	This constraint turns on Fast Slew Rate Control	This preference is a part of the SLEWRATE preference
OFFSET IN	To specify input delay	INPUT_SETUP to specify input delay
OFFSET OUT	To specify output delay	CLOCK_TO_OUT to specify output delay
KEEP	The KEEP constraint is used to prevent a net from either being absorbed by a block, or synthesized out	Can be controlled using the synthesis attribute/*synthesis syn_keep=1*/
MAXDELAY	This constraint is used to specify the maximum delay in a net	MAXDELAY
MAXSKEW	This constraint is used to specify the maximum skew in a net	MAXSKEW
PERIOD	This constraint specifies the timing relationship of a global clock such as an fMAX requirement	PERIOD/FREQUENCY
TIG	Timing ignore or flase path	BLOCK
FROM/THRU/TO	Multi cycle path constraints contrained using FROM: TO: in ISE	MULTICYCLE
SYSTEM JITTER	Used to specify system jitter of the design	SYSTEM JITTER

As a part of the migration programs. please reach out to your sales or FAE partners on how Lattice can further assist you in migrating your timing constraints from EOL AMD parts to FPGA devices.

9. I/O and Package Pins Mapping

Another key activity in the design migration workflow is mapping of package pins between the EOL AMD part and Lattice device. As an example, the Spartan-3A part has the following types of pins that needs correct mapping to Lattice FPGA.

VCC
VSS
NC
Config Pins
SERDES Config
GPIO
Input Only
LVDS Pair

We have created an excel based framework that helps in mapping all the pins from EOL AMD part to equivalent Lattice FPGA device. If you are planning to replace Spartan3A with Lattice's ECP5 part, you can request this excel from your Sales or FAE partner.

10. Programming and Configuration

After you have migrated and verified your design, you can use the final output data file to download or upload a bitstream to or from an FPGA device using the Diamond or Radiant Programmer (depending on the FPGA device chosen for migration). The bitstream file contains all the configuration information from the physical design that define the internal logic and interconnections of the FPGA, as well as device-specific information from other files associated with the target device. The types of file formats supported are:

File Format	Description
Bit File (binary) (.bit)	Binary bitstream files are the default output of the bitstream process and contain the configuration information in bitstream (zeroes and ones) that is represented in the physical design (.ncd) file
Raw Bit File (ASCII) (.rbt)	The Raw Bit File is a text file containing ASCII ones and zeros representing the bits in the bitstream file. If you are using a microprocessor to configure a single FPGA, you can include the Raw Bit file in the source code as a text file to represent the configuration data. The sequence of characters in the Raw Bit file is the same as the bit sequence that is written into the FPGA. The .rbt file differs from the .bit file in that it contains design information in the first six lines
Hex Mask File (.msk)	Used to compare relevant bit locations for executing a read back of configuration data contained in an operating FPGA
Bit Generation Report File (.bgn)	Outputs information on a bit generation (bitgen) run and displays information on options that are set. This file is output by default and given the name, design_ name>.bgn
JEDEC	The programming standard from the Joint Electron Design Engineering Committee, a committee of programmer and semiconductor manufacturers that provide common standards for programmable issues. Examples include acceptable test characters for PLDs and standard data transfer/programming formats for PLDs. The JEDEC Standard is the industry standard for PLD formats. In Diamond Programmer, JEDEC usually refers to the JEDEC fuse map of your design for the device that you have selected

11. Embedded Designs

When thinking about migrating an embedded design, the entire ecosystem needs to be considered for migration. Hence this section probably deserves a white paper of its own. More on that later but for now we'll cover few key points here as a part of the overall design migration workflow.

Some EOL AMD parts supported MicroBlaze soft processor whereas Lattice FPGAs supports RISC-V soft processor. Points for consideration are:

- Processor
  - Instruction Set Architecture
  - Internal Core Features
  - Native Interfaces
  - Performance
- Peripheral Portfolio
- Toolchain
  - Compiler
  - Compiler Libraries
  - Debugger Utilities
- Execution Environment
  - Bare Metal
  - RTOS
- Vendor Provided Firmware
 - C-Run Time Library
  - Boot Loader(s)

At Lattice, we have support for the entire ecosystem to facilitate your embedded design migration efforts.

12. Summary

Supply chain disruptions are hard for any business. It can have a negative ripple effect on your business continuity plans and can stress your business resilience processes. But it can also be a great strategic opportunity to future proofing your business through product upscaling, rebuilding business resiliency by securing your supply chain for long term, and unlocking additional revenue and better profit margins. The EOL announcement from AMD of multiple product families is one such instance where great organizations can transform this disruption into a strategic opportunity. We understand that design migration, which is a key component for the success of this transformation, can seem daunting.

At Lattice, we have carefully considered these challenges and have created a couple of migration programs to guide our customers through their transformational journey of migration from EOL AMD parts to Lattice FPGA devices.

We are here to help you in securing your supply chain, upscaling your product while going through design migration workflow, and quickly getting your product to the market.
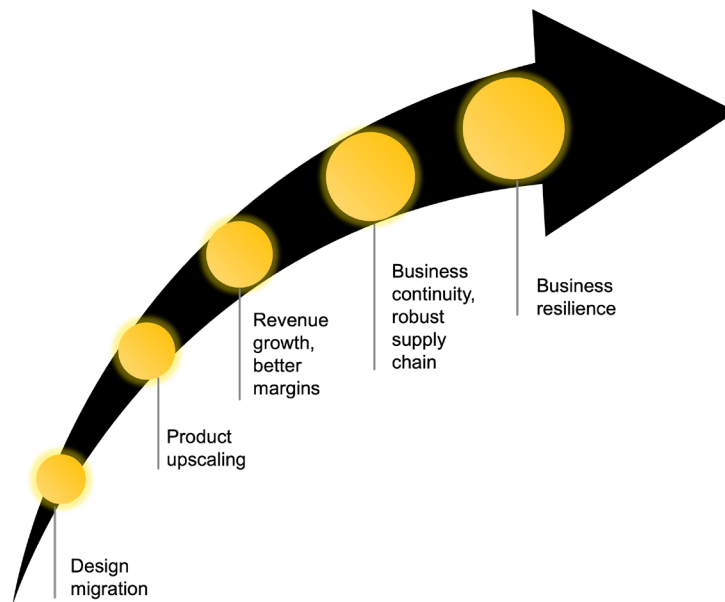
Please reach out to your Sales or FAE partners to learn more about the migration programs that Lattice has to offer.

13. Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.
For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/en/Support/AnswerDatabase.

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