Migrating Designs from AMD ISE Design Suite to Lattice Radiant Software

Application Note

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
CPLD	Complex Programmable Logic Device
DDR	Double Data Rate
DQS	DDR Data Q Strobe
ECLK	Edge clock
ECO	Engineering Change Order
FPGA	Field Programmable Gate Array
GUI	Graphical User Interface
HDL	Hardware Description Language
I/O	Input/Output
IP	Intellectual Property
LDC	Lattice Design Constraints
LSE	Lattice Synthesis Engine
PACE	Pinout and Area Constraints Editor
PAR	Place and Route
PCB	Printed Circuit Board
PLC	Programmable Logic Controller
PLL	Phase Locked Loop
RTL	Register Transfer Level
SDC	Synopsys Design Constraints
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TCE	Timing Constraints Editor
TCL	Tool Command Language
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
XCF	XST Constraint File
XST	Xilinx Synthesis Technology

1. Introduction

The Lattice Semiconductor Field Programmable Gate Array (FPGA)/Complex Programmable Logic Device (CPLD) design flow is similar in conception and implementation to the AMD FPGA design flow. At its core, a hardware description language (HDL) code of the register transfer level (RTL) can be imported into one of Lattice's design software and then configured to one of Lattice's FPGA.

This document guides FPGA designers familiar with the AMD ISE® Design Suite software, specifically version 14.7, to migrate existing designs to the Lattice Radiant® software and highlights some of the differences and similarities between the design flows of AMD ISE Design Suite and Lattice Radiant software.

This migration guide starts with an overview and comparison of the design software and a mapping of the tools and file extensions between the two. The next section compares the design flows of the design software. The succeeding sections provides a step-by-step walkthrough on the following:

- Project creation and management
- Design entry
- Implementation flow
- Programming/Configuration

You can view Lattice Radiant software tutorial videos by following the links listed in Table 1.1.

Table 1.1. Lattice Radiant Software Tutorial Videos

Tutorial Video Links	Descriptions
Introduction to Lattice Radiant Software	An introductory video featuring key design experience features of Radiant software.
Lattice Radiant Software Tool Flow - Part 1	A training series showing procedure on full design flow and key features of Radiant software.
Lattice Radiant Software Tool Flow - Part 2	
Lattice Radiant Software Tool Flow - Part 3	
Setting Up a Floating License Tutorial	An instructional video on how to set up a floating license on a server and how to setup environment variables on a client machine to access the server license.

2. Design Software Overview

A design software is required to develop and implement FPGA/CPLD designs for market usage. The design software must have the following characteristics to reduce the design's time-to-market:

- Is full-featured which means it offers all necessary tools for design development.
- Has high performance which means it can perform powerful optimizations and analyses.
- Has intuitive user interface which provides the best user experience with a graphical user interface (GUI) that is both modular and wizard driven.

The Radiant software has these characteristics, making it one of the best industry solutions for low-end to mid-range FPGA designs. The Radiant software integrated tool environment provides a modern and comprehensive user interface to control Lattice Semiconductor FPGA implementation process. The Radiant software supports newer Lattice FPGA device families when compared to Lattice Diamond™ software.

The Radiant software uses an expanded project-based design flow and integrated tool views to create and analyze design alternatives and what-if scenarios easily. The Implementations and Strategies concepts provide a convenient way for you to try alternate design structures and manage multiple tool settings.

Key features of the Radiant software are as follows:

- Has system-level information, integrated HDL code checking, and consolidated reporting features.
- Includes a Timing Analysis View that saves time by allowing interactive changes to design constraints and viewing the results without disturbing your design.
- Has an Engineering Change Order (ECO) Editor and Programmer tools that are tailored to make individual task easier.
- Has a cross-probing feature and a shared memory architecture to ensure fast performance and better memory utilization.
- Is highly customizable and provides Tool Command Language (TCL) scripting capabilities from either its built-in console or from an external shell.

2.1. Design Software Comparison

Most of the capabilities available in the AMD ISE Design Suite software are also available in the Radiant software.

However, the terminology of the individual tools, features, and file formats may differ from one software to the other. Table 2.1 lists some of the tools, features, and file formats in AMD ISE Design Suite software and their corresponding names in the Radiant software.

Table 2.1. Tools, Features, and File Extensions Mapping between AMD ISE Design Suite and Radiant Software

Comparison Items	AMD ISE Design Suite software	Lattice Radiant software
Optimization or Implementation Settings	Design Strategies	Design Strategies
Design Entry	HDL file AMD Core Generator	HDL file IP Catalog
Design Constraints	Constraints Editor ISE Text Editor PlanAhead™ tool for FPGA Pinout and Area Constraints Editor (PACE) for CPLD Commercially available text editors HDL source file using a text editor XST Constraint File (XCF) using a text editor	Device/Physical Constraint Editor Timing Constraint Editor Source Editor
Synthesis Tools	Xilinx Synthesis Technology (XST) Synplify Pro Precision	Lattice Synthesis Engine (LSE) Synplify Pro
Schematic Tools	Schematic Viewer for RTL and Technology View	Netlist Analyzer
Place and Route	Xilinx Implementation Tool	Radiant Place and Route

Comparison Items	AMD ISE Design Suite software	Lattice Radiant software
Simulation	Isim Siemens ModelSim® Siemens QuestaSim™	Cadence® Xcelium™ Synopsys® VCS® Siemens QuestaSim Siemens ModelSim
Power	Xpower Analyzer	Power Calculator
On-Chip Debug Tool	ChipScope™ Pro Tool	Reveal Inserter Reveal Analyzer
Project File Extension	.xise	.rdf

3. FPGA Design Flow Overview

When creating designs for FPGA, Lattice and AMD software tools have similarities in terms of concepts, approach, and functionality.

The Radiant software framework technology uses the typical FPGA design flow (shown in Figure 3.1) that adheres to a sequence of steps which begins with setting up the design environment and ends with generating the programming files that will be used to program the hardware.

If you are familiar with ISE Design Suite and would like to convert your existing ISE designs to Lattice Radiant software environment, you can simply import your HDL files to Lattice Radiant software and begin implementing the project-based methodology which is shown in Figure 3.2.

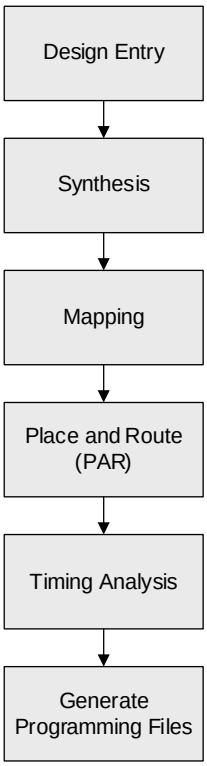

Figure 3.1. Typical FPGA Design Flow Used by AMD ISE Design Suite and Lattice Radiant Software

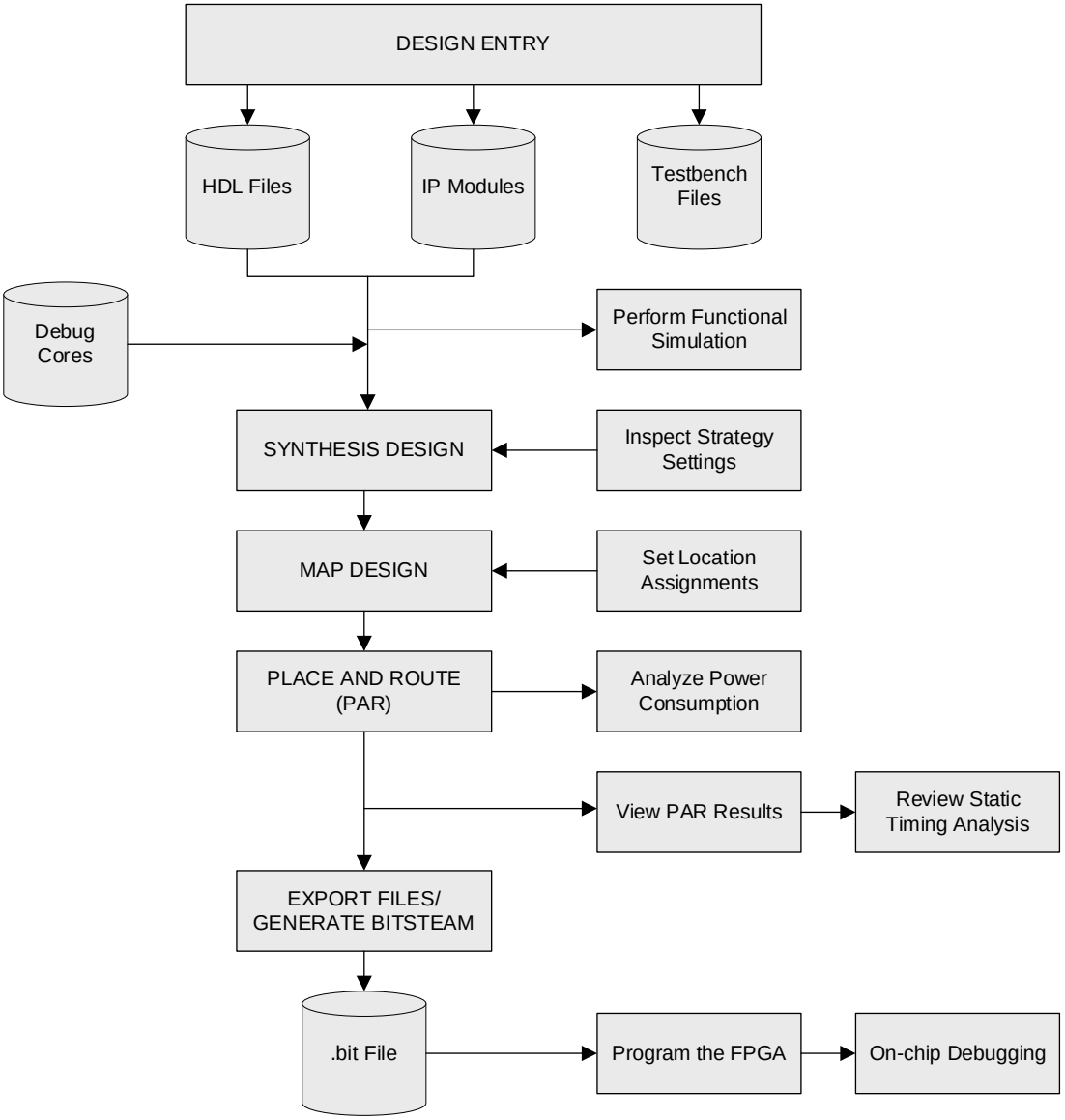

Figure 3.2. Lattice Radiant Software Detailed Design Flow

4. Design Entry

HDL such as Verilog and VHSIC Hardware Description Language (VHDL) are fully supported in both Lattice Radiant software and AMD ISE Design Suite software. This section describes various design HDL methodologies used in both the Radiant software and the ISE Design Suite software, and highlights the similarities and differences.

4.1. Using HDL in Radiant Software

You can reuse your Verilog and VHDL source files when migrating designs from AMD ISE Design Suite to Lattice Radiant software.

In ISE Design Suite software, new source files are added using the New Source wizard by clicking **File** > **New** or by right-clicking anywhere on the hierarchy window and choosing **New Source** or **Add Source** to add existing sources.

In the Radiant software, you can do this by performing the following steps:

1. Clicking **File** > **New** or by right-clicking the **Input Files** folder on the **File List** tab.
2. From the dropdown menu click on **Add** > **New File**. A **New File** dialog box as shown in Figure 4.1 opens and you can choose the HDL file type to add to the design. You can also add an existing source by selecting **Add** > **Existing File**.

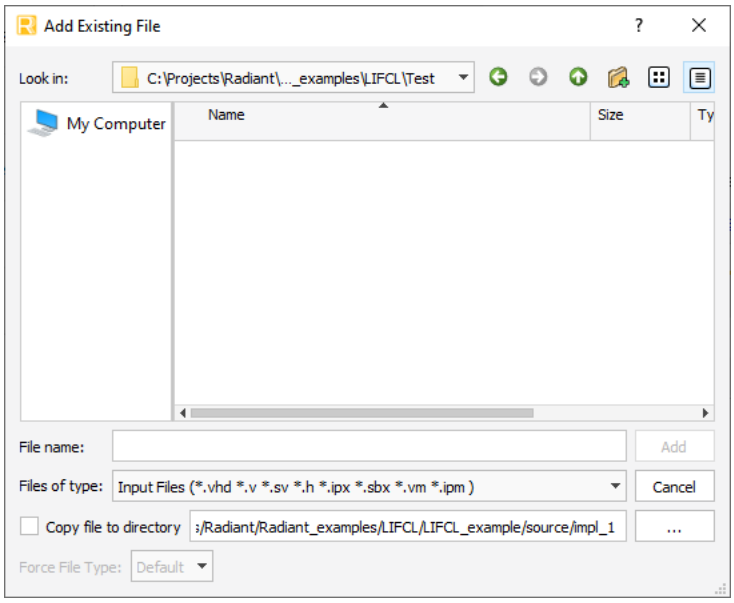

Figure 4.1. New File Wizard in Radiant Software

Table 4.1 shows the list of files supported as input files to the Radiant software.

Table 4.1. Radiant Software Input File Types

File Types	Descriptions
*.vhd, *.v, *.sv, *.h, *.ipx, *.vm	Input files
*.sdc	Pre-synthesis constraints file
*.ldc	Lattice LSE constraints file
*.pdc	Post-Synthesis constraints file
*.rva, *.rvl	Debug files
*.spf	Script file
*.pcf	Analysis file
*.xcf	Programming file
.	Other files

4.2. Using Radiant Software Device-specific Primitives

If your design contains any ISE Design Suite software device-specific primitives, you may need to replace them with the Radiant software device-specific primitives. Refer to *Libraries Reference Guide* in Radiant software Help section for a complete list of primitives available for Radiant software devices.

4.3. Using an IP Core in Radiant Software

In the ISE Design Suite software, Core Generator is used to import an intellectual property (IP) core into a project. Whereas in the Radiant software, IP Catalog is used to configure and import an IP core into a project.

In ISE Design Suite software, you can open the Core Generator under **Tools** > **Core Generator**. The Core Generator window opens and you can select which IP core to customize and add to the design. Figure 4.2 shows the ISE Design Suite software Core Generator flow.

In the Radiant software, an IP core can be accessed through the IP Catalog. The foundation IP is available under **IP** on **Local** tab and soft IP is available under the **IP** on **Server** tab of the IP Catalog.
Figure 4.3 shows the Radiant software soft IP flow.

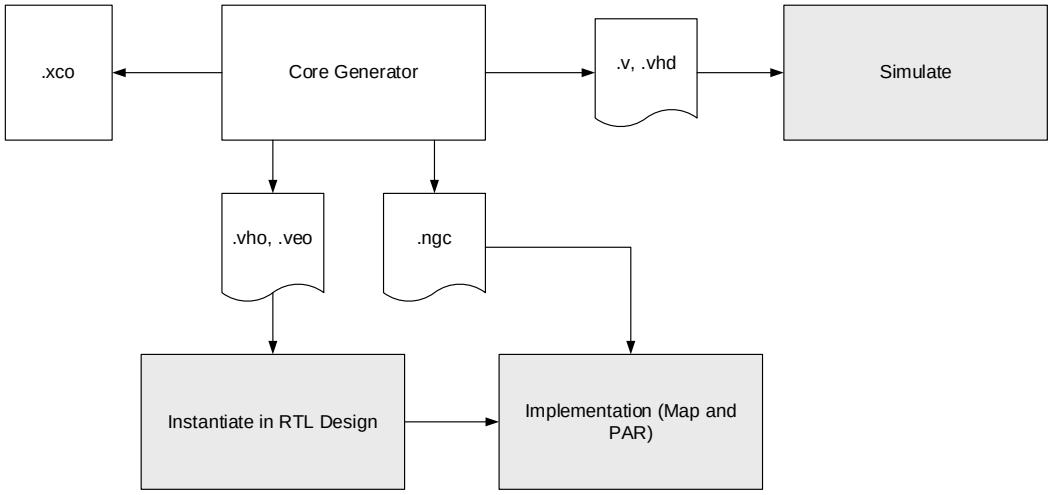

Figure 4.2. ISE Design Suite Software Core Generator Flow

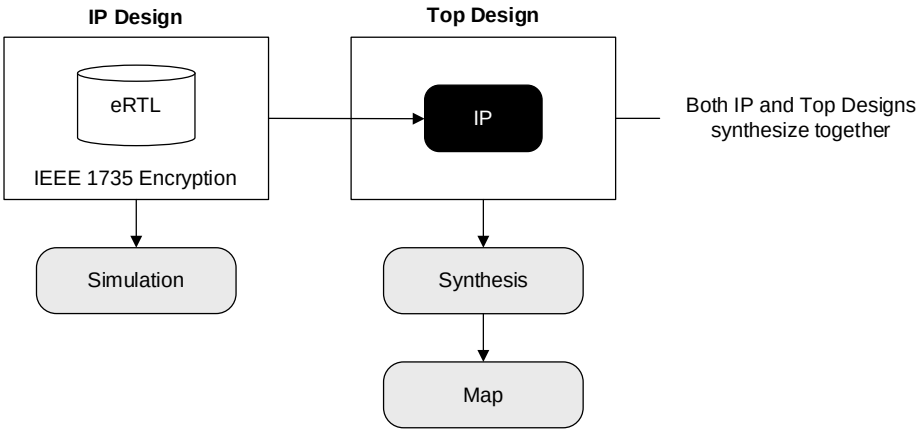

Figure 4.3. Radiant Software Soft IP Flow

Refer to the following steps to configure and import an IP core using the Radiant software IP Catalog:

1. Click the IP Catalog icon on the Radiant software toolbar as shown in Figure 4.4 to open the IP Catalog tab.

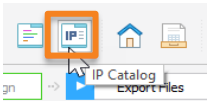

Figure 4.4. IP Catalog Icon on Radiant Software Toolbar

2. **IP Information** tab as shown in Figure 4.5 opens.

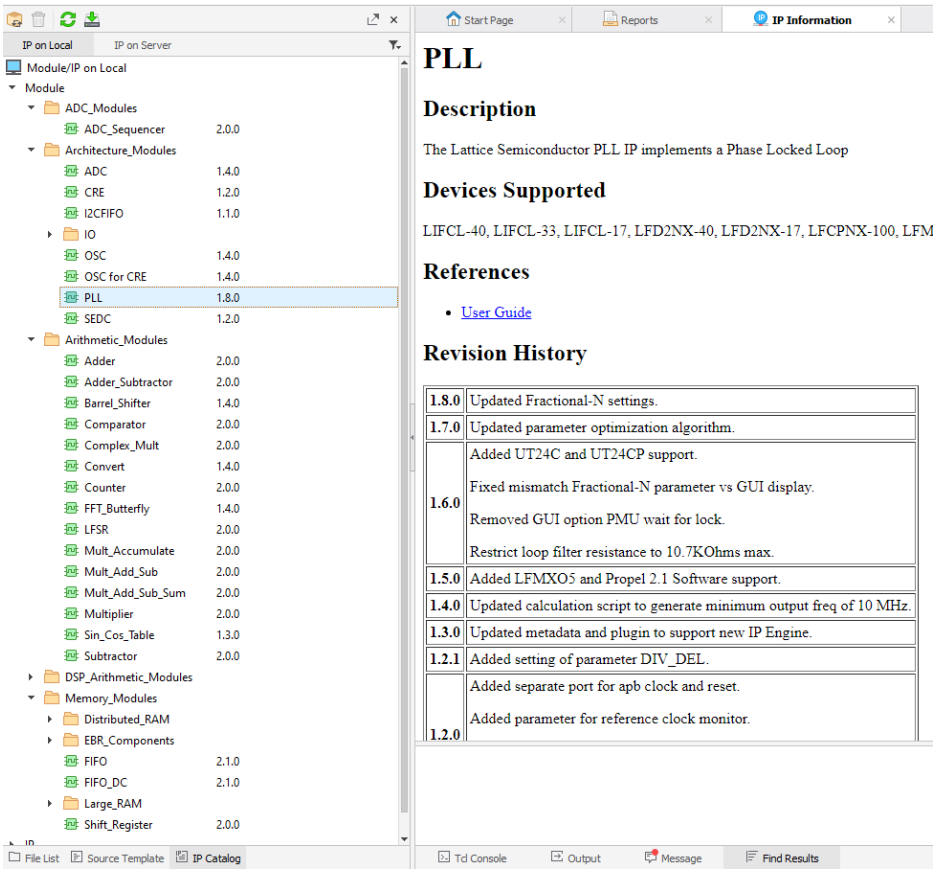

Figure 4.5. Radiant IP Catalog GUI

The output file structure generated by IP Catalog and their descriptions are listed in Table 4.2.

Table 4.2. IP Catalog Output Files and their Descriptions

File Names	Descriptions
constraints	IP constraints
misc	IP instantiation template
rtl	IP source RTL
testbench	IP testbench files
component.xml	IP definition .xml file
design.xml	IP configuration .xml file
ip_name.cfg	User IP configuration settings file
ip_name.ipx	IP file that must be imported to the Radiant software

Some of the common IP cores used in AMD Spartan 3E and Lattice CertusPro™-NX devices are listed in Table 4.3. For the detailed descriptions of the IP cores, refer to the Radiant software Help section.

Table 4.3. Comparison of Common IP Cores Used between AMD Spartan 3E and Lattice Certus-Pro Devices

Purpose	Spartan 3E IP Cores	CertusPro-NX IP Cores
Clock Manager	Single DCM_SP	PLL IP
FIFO Operations	FIFO Generator	FIFO IP, FIFO_DC IP
Memory Blocks	RAM IP (SP, Dual Port, True Dual Port, and Dual Port)	RAM_DP, RAM_DP_TRUE, RAM_DQ
Distributed Memory	Distributed Memory (ROM, Single Port, Dual Port, and SR16 based memory)	Distributed_DPRAM, Distributed_ROM, Distributed_SPRAM
Shift Register	RAM-based Shift Register	RAM_Based_Shift_Register
Arithmetic Operations	Adder Subtractor	Adder, Adder_Subtractor
	Multiplier	Multiplier, Multiply_Accumulate
Trigonometric Operations	CORDIC	Sin-Cos_Table

5. Design Constraints

Design constraints are used to specify the performance requirements desired for the FPGA design. Constraints are instructions applied to the design elements that guide the design toward desired results and performance goals. They are critical for achieving timing closure or managing reusable IP. The most common constraints are those for timing and pin assignments, but constraints are also available for placement, routing, and other functions.

The ISE Design Suite stores all the design constraints and attributes in one single file (.ucf) which includes all timing and device constraints.

In the Radiant software, constraints can be defined in different constraint files (.ldc/.pdc/.sdc/.fdc). The constraints can also be defined with HDL attributes for physical pin locking. The constraints defined depend on the synthesis tool used and their entry points.

A *.ldc or *.sdc constraint file is used at pre-synthesis and specifies the design goals. Synthesis, Map, and Place and Route (PAR) stages work to meet these goals. Pre-synthesis constraint file support depends on the synthesis tool used. See the following for more details:

- .ldc (for LSE)
- .sdc (for Synplify Pro and LSE)
- .fdc (for Synplify Pro)

A *.pdc constraint file can also be specified at post-synthesis which applies the constraints to Map and PAR stages. The constraints flow combines these constraints based on their different entry points within the Radiant software design flow. See Figure 5.1 for more details. The timing analysis tool reports whether the timing goals are met.

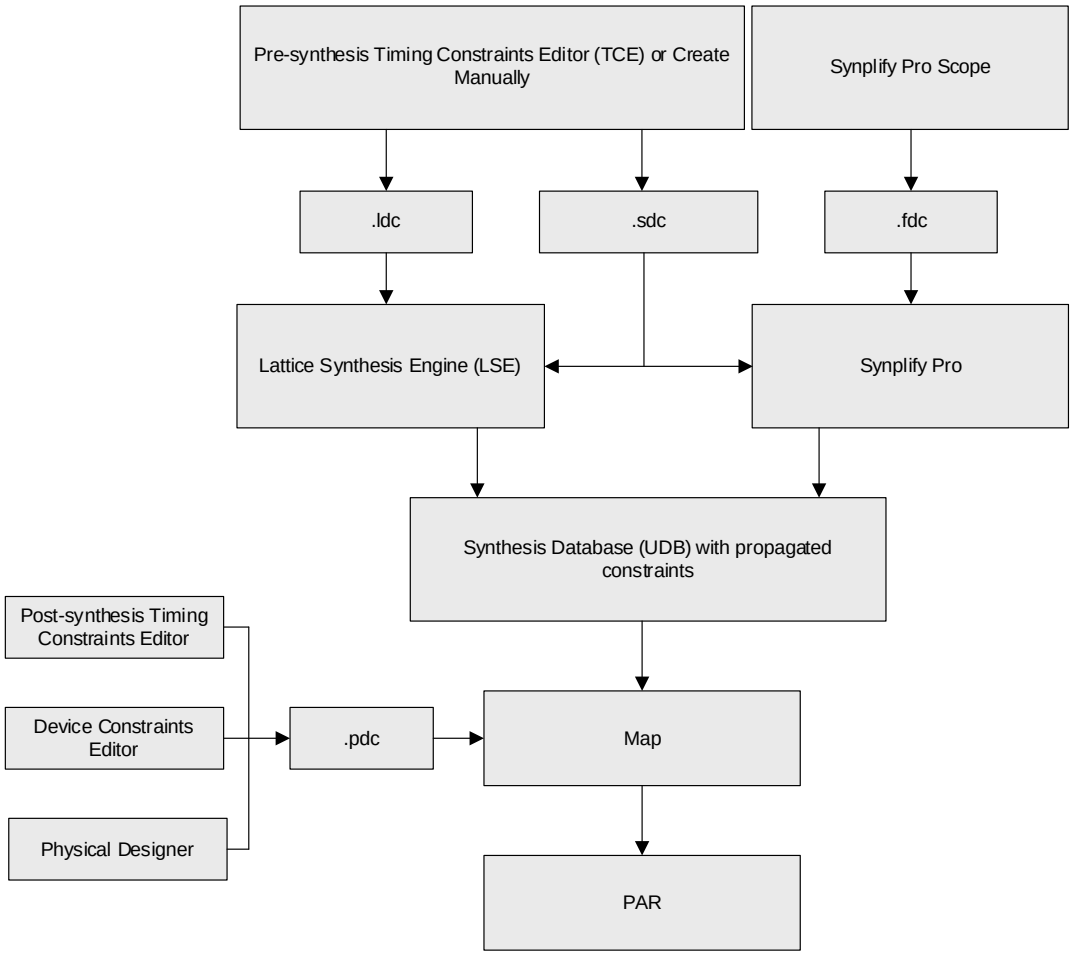

Figure 5.1. Lattice Radiant Constraints Flow

The Radiant software offers various tools to help you constrain your design. The various tools offered are as follows:

- Pre-synthesis Timing Constraint Editor (see Figure 5.2)
- Post-Synthesis Timing Constraint Editor (see Figure 5.3)
- Device Constraints Editor
- Physical Designer
- Source Editor

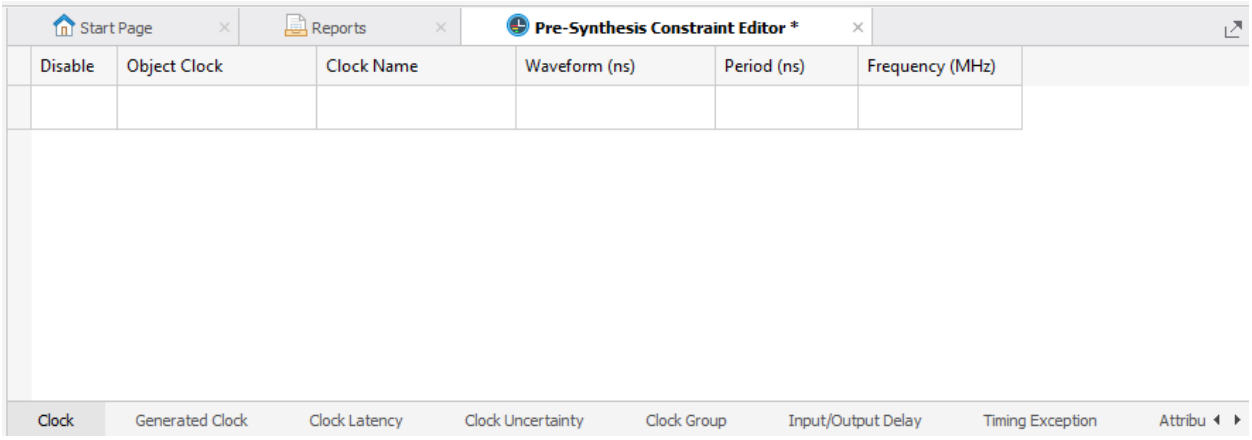

Figure 5.2. Pre-synthesis Constraint Editor

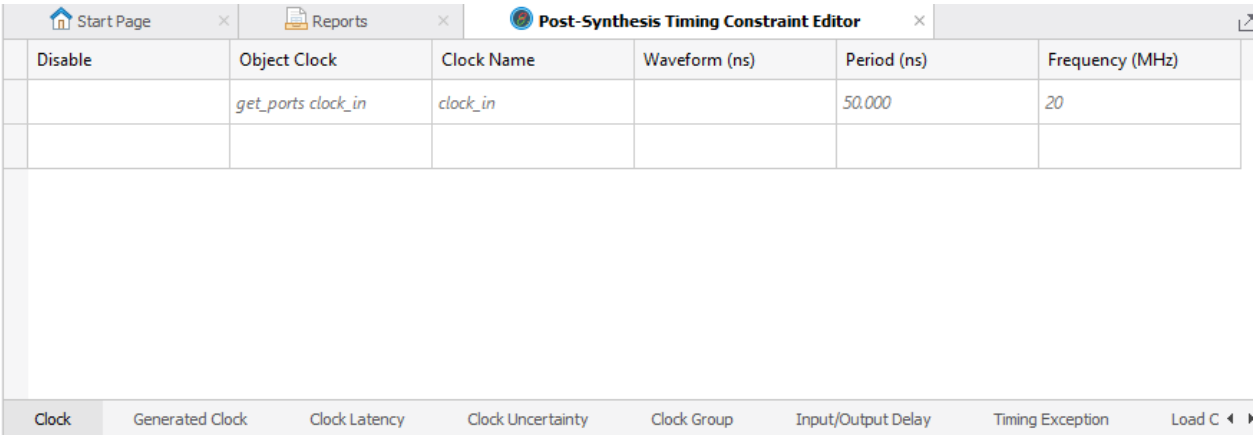

Figure 5.3. Post-synthesis Timing Constraint Editor

5.1. Timing Constraints

Table 5.1 below shows commonly used timing constraints in ISE Design Suite software and their equivalent constraints in the Radiant software. For a detailed description of each of these constraints, refer to the Radiant software Help section.

Table 5.1. ISE Design Suite Timing Constraint to Radiant Software Constraint Conversions

ISE Constraints	Constraint Functions	Radiant Equivalent Constraints
OFFSET IN	To specify input delay	set_input_delay
OFFSET OUT	To specify output delay	set_output_delay
KEEP	To prevent a net from either being absorbed by a block or synthesized out	Can be controlled using the synthesis attribute /* synthesis syn_keep = 1 */
MAXDELAY	To specify the maximum delay in a net	set_max_delay
MAXSKEW	To specify the maximum skew in a net	set_max_skew

ISE Constraints	Constraint Functions	Radiant Equivalent Constraints
PERIOD	To specify the timing relationship of a global clock such as an *fMAX* requirement	create_clock
TIG	Timing Ignore or false path	set_false_path
FROM/THRU/TO	Multicycle path constraints constrained using *FROM:* and *TO:* in the ISE Design Suite software	set_multicycle_path
SYSTEM JITTER	To specify system jitter of the design	set_clock_uncertainty

Here are some examples of timing constraint conversions:

- create_clock constraint:
  - ISE Design Suite software:
    ```
    NET "clk" TNM_NET = clk_in;
    TIMESPEC TS_clk_in = PERIOD "clk_in" 5 ns HIGH 50%;
    ```
  - Radiant software:
    ```
    create_clock -name clk_in -period 5 -waveform {0 25} [get_ports clk]
    ```
- set_input_delay constraint for an input port:
  - ISE Design Suite software:
    ```
    NET in_a OFFSET = IN 2 BEFORE clk;
    ```
  - Radiant software:
    ```
    set_input_delay 4 -clock clk [get_ports in_a]
    ```
- set_input_delay constraint for ALLPORTS:
  - ISE Design Suite software:
    ```
    OFFSET = IN 2 AFTER clka;
    ```
  - Radiant software:
    ```
    set_input_delay 2 -clock clka [get_ports IN]
    ```
- set_output_delay constraint for an output port:
  - ISE Design Suite software:
    ```
    NET out1 OFFSET = OUT 8 AFTER clk2;
    ```
  - Radiant software:
    ```
    set_output_delay 8 -clock clk2 [get_ports out1]
    ```

    Note: In the ISE Design Suite software, OFFSET = OUT performs only maximum delay analysis. In the Radiant software, set_output_delay constraint can be used with MAX and/or MIN options to perform max and min delay analysis.
- set_false_path onstraint:
  - ISE Design Suite software:
    ```
    NET reset TIG;
    ```
  - Radiant software:
    ```
    set_false_path -from [get_ports reset]
    ```

- set_max_skew constraint:
  - ISE Design Suite software:
    ```
    NET NetB MAXSKEW = 5ns;
    ```
  - Radiant software:
    ```
    set_max_skew [get_nets NetB] 5
    ```
- set_multicycle_path constraint:
  - ISE Design Suite software:
    ```
    TIMESPEC TS_01 = FROM "R_REG1_GROUP" TO "R_REG3_GROUP" TS_clk*3;
    ```
  - Radiant software:
    ```
    set_multicycle_path -from [get_cells _REG1_GROUP] -to [get_cells R_REG3_GROUP] 3
    ```

5.2. Physical Constraints

Table 5.2 shows commonly used physical constraints in ISE Design Suite software and their equivalent constraints in Radiant software.

Table 5.2. ISE Design Suite Physical Constraint to Radiant Software Constraint Conversions

ISE Constraints	Constraint Function	Radiant Equivalent Constraints
LOC	The Location (LOC) constraint	ldc_set_location
IOB	To specify whether a register should be placed within the IOB of the device	Can be controlled using HDL attribute /* synthesis syn_useioff = 1|0 */
IOSTANDARD	To specify the input/output (I/O) standard for an I/O pin.	This option is part of the ldc_set_port constraint. You can also use synthesis attributes to specify the I/O Type. Example: /*synthesis IO_TYPE = “type_name]*/
DRIVE	To control the output pin current value	This option is part of the ldc_set_port constraint. You can also use synthesis attributes to specify the DRIVE. Example: /*synthesis DRIVE= “[drive_strength]”*/
VREF	To configure listed pins as *VREF* supply pins that is used with other I/O pins	ldc_create_vref
PROHIBIT	To prohibit a placement on a site	ldc_prohibit
FAST	To turn on Fast Slew Rate Control	This option is part of the ldc_set_port constraint. You can also use synthesis attributes to specify the SLEWRATE parameters. Example: /*synthesis SLEWRATE= “FAST”*/

You can create and modify physical constraints in the .pdc file using the Device Constraints Editor tool or modify the .pdc file directly using a source editor.

6. Synthesis

The AMD ISE Design Suite software has the XST (Xilinx Synthesis Tool) to perform synthesis on designs with user logic and AMD IP cores. The software also supports Synplify Pro for synthesis.

The Lattice Radiant software has a proprietary synthesis tool Lattice Synthesis Engine (LSE) and supports a third-party synthesis tool Synplify Pro OEM. Both synthesis tools support synthesis of user logic and Lattice IP cores.

Table 6.1 shows the Synthesis tools supported by both the ISE Design Suite and the Radiant software.

Table 6.1. Comparison between ISE Design Suite and Radiant Synthesis Tools

ISE Design Suite Software	Lattice Radiant Software
Xilinx Synthesis Tool (XST)	Lattice Synthesis Engine (LSE)
Synplify Pro	Synplify Pro

You can select available synthesis tools in the ISE Design Suite software by going to **Project** > **Design Properties**.

In the Radiant software, you can do this by right-clicking the current implementation and choosing **Select Synthesis Tool** from the dropdown menu as shown in Figure 6.1.

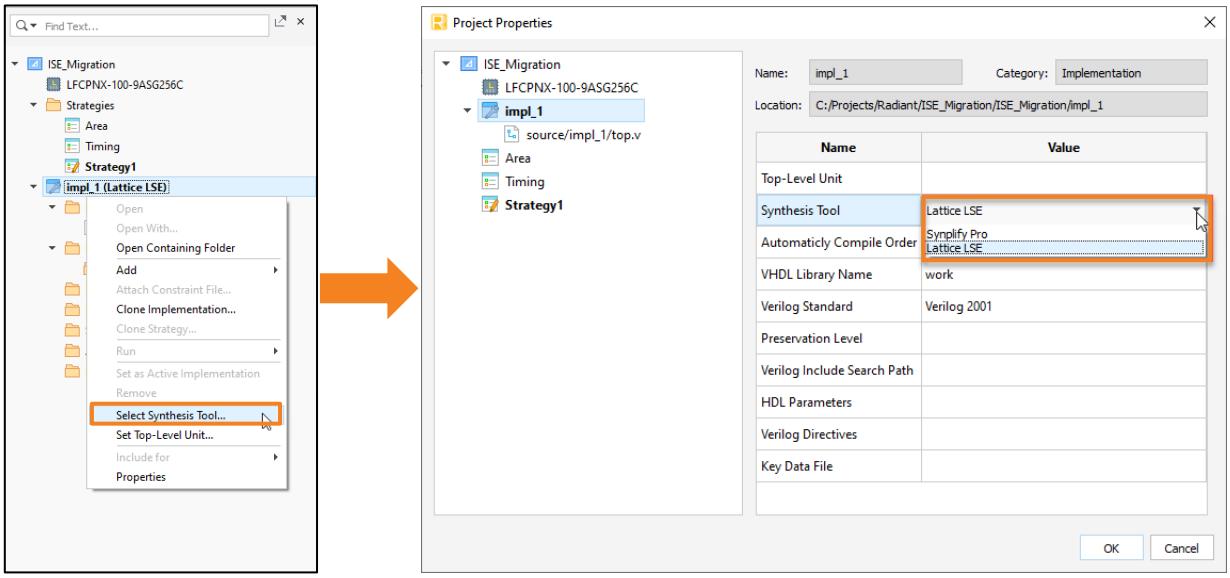

Figure 6.1. Choosing Synthesis Tool in Radiant Software

In the ISE Design Suite software, synthesis is performed by double-clicking on **Synthesize-XST process** under **Processes**.

In the Radiant software, synthesis is performed by clicking on the **Synthesize Design** play icon on the **Process** toolbar as shown in Figure 6.2.

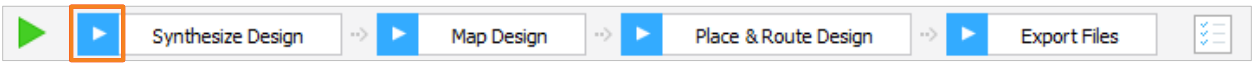

Figure 6.2. Process Toolbar in Radiant Software

7. Schematic Viewer

A generated netlist can be viewed through one or more schematic views and a browser that shows lists of modules, instances, ports, and nets.

In the ISE Design Suite software, this can be performed by going to **Tools** > **Schematic Viewer**.

In the Radiant software, this can be performed using Netlist Analyzer of LSE or HDL Analyst of Synplify Pro.

Table 7.1 compares the Schematic Viewer between the ISE Design Suite and the Radiant software.

Table 7.1. Comparison between ISE Design Suite and Radiant Software Schematic Viewer

AMD ISE Design Suite Software	Lattice Radiant Software
RTL Viewer and Technology Map Viewer	Netlist Analyzer and HDL Analyst

7.1. Netlist Analyzer

To open Netlist Analyzer, click on the **Netlist Analyzer** icon on the Radiant software toolbar as shown in Figure 7.1.

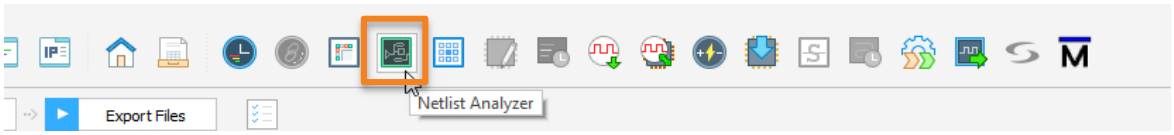

Figure 7.1. Netlist Analyzer Icon on Radiant Software Toolbar

For detailed information, refer to the Netlist Analyzer section in the Lattice Radiant User Guide from the Radiant software Help menu.

7.2. HDL Analyst

To open RTL View or Technology View in Synplify Pro, open Synplify Pro from the Lattice Radiant software toolbar as shown in Figure 7.2. Then, choose RTL View or Technology View option. The difference between the two views are as follows:

- RTL View: Provides a high-level and technology-independent graphic representation of your design after compilation by using technology-independent components like variable-width adders, registers, large multiplexers, and state machines.
- Technology View: Provides a low-level and technology-specific view of your design after mapping by using components such as look-up tables, cascade and carry chains, multiplexers, and flip-flops.

Figure 7.2. Synplify Pro Icon on Radiant Software Tool bar

8. Design Mapping

Design mapping converts the logical design into a network of physical components or configurable logic blocks.

In the ISE Design Suite software, this process is combined with the Implementation process. Double-click the **Map** process to run Map. You can click on **Implement Design** to automatically run Translate, Map, and Place and Route in a sequence.

In the Radiant software, the Map design flow can be optimized through the design strategy settings. To map a design, click the **Map Design** play icon as shown in Figure 8.1.

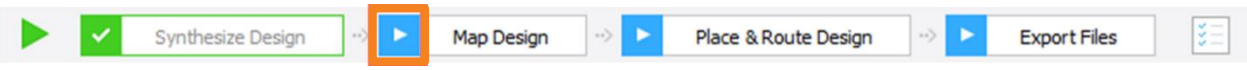

Figure 8.1. Map Design Icon on Radiant Software Process Bar

9. Place and Route

After a design has undergone the necessary translation to bring it into the physical design format during mapping, it is ready for placement and routing. Placement is the process of assigning the device-specific components produced by the mapping process to specific locations on the device floorplan.

After placement is complete, the route phase establishes physical connections to join components in an electrical network. The Place and Route process takes a mapped physical design and places and routes the design. Placement and routing of a design can be cost-based or timing driven.

Placement and routing options can influence the performance and utilization of the design implementation and ease incremental design changes. Some options affect the way the results are reported. Experimenting with Place and Route settings in the **Strategies** dialog box can help to improve the placement and routing results. Figure 9.1 shows an example of Place and Route settings.

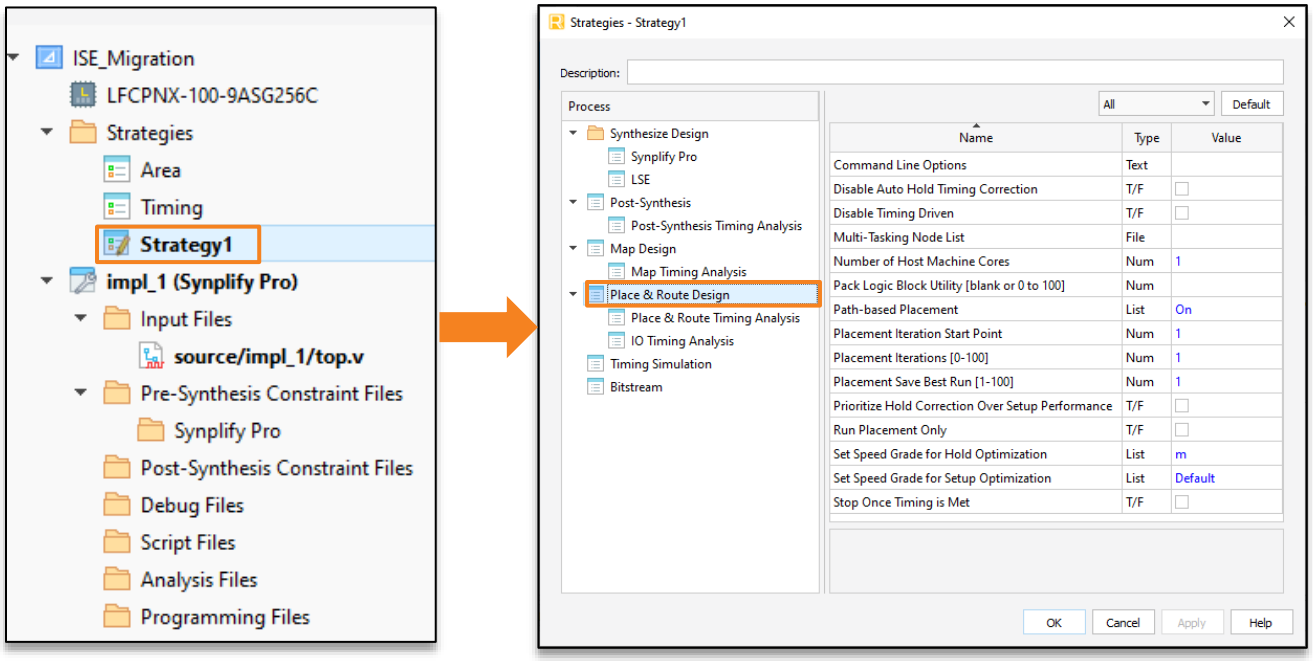

Figure 9.1. Radiant Strategy Settings for Place and Route Design

In most cases, your design requires timing-driven placement and routing, where the timing criteria specified influences the implementation of the design. In the Radiant software, the static timing analysis results show how constrained nets meet or do not meet your timing closure. The Place and Route timing analysis, as shown in Figure 9.2, is turned on by the default process.

The Place and Route timing and I/O Timing analysis reports can be accessed from the **Analysis Reports** folder of the **Reports** window. These reports help to ensure that the I/O plan meets the I/O standards and power integrity requirements of the printed circuit board (PCB) design.

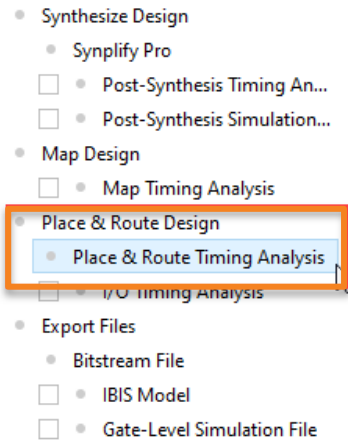

Figure 9.2. Place and Route Timing Analysis in Radiant Software

After Place and Route or Implementation stage, the AMD ISE Design Suite software has the FPGA Editor to allow editing of your design at post-implementation.

In the Radiant software environment, the equivalent tool is the Physical Designer tool, shown in Figure 9.3. This tool has a combined GUI of both the Placement Mode and Routing Mode. This tool provides one central location for you to do all the floor-planning and to view the physical layout of your design. The three modes available for this tool are as follows:

- Placement Mode
  This mode provides a large-component layout of your design. In this mode, all connections are displayed as fly-lines. The Placement Mode is for GROUPS and REGIONs assignment. The Placement Mode allows you to create REGIONs and bounding boxes for GROUPS and specify the types of components and connections to be displayed. As you move your mouse pointer slowly over the floorplan layout, details are displayed in the tool tips. The number of resources for each GROUP and REGION, the number of utilized slices for each programmable logic controller (PLC) component, and the name and location of each component, port, net, and site are some examples of details displayed in the tool tips.
- I/O Mode
  This mode is for I/O planning and I/O assignment such as Double Data Rate (DDR) interface, DDR Data Q Strobe (DQS) and clock assignments. As you move your mouse pointer slowly over the I/O Abstract layout, the number of resources for each item such as Edge Clock (ECLK), DDR, Phase Locked Loop (PLL), and I/O Banks utilization are displayed in the tool tips.
- Routing Mode
  This mode provides a read-only detailed layout of your design that includes switch boxes and physical wire connections. In this mode, routed connections are displayed as Manhattan-style lines, and unrouted connections are displayed as fly-lines. As you move your mouse slowly over the layout, the name and location of each REGION, group, component, port, net, and site are displayed in the tool tips.

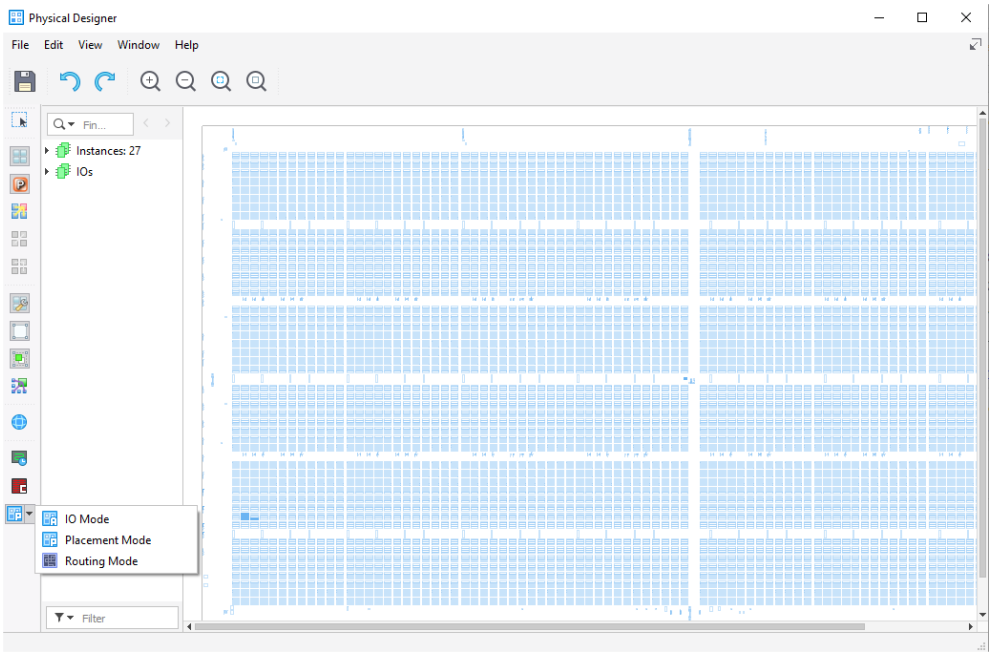

Figure 9.3. Physical Designer Tool in Radiant Software

10. Cross Probing

Cross-probing is a feature that allows the software to seamlessly have bi-directional communication between different tools within the software itself. You can select a design element from one tool and locate them in another tool. Both ISE Design Suite and Radiant software have cross-probing ability.

In the Radiant Software, aside from using tools to cross probe, you can also click a hyperlink icon in the report to cross probe to the corresponding tool. Some examples of cross probing from hyperlink icons are the following:

- From the Post-synthesis timing report and Map timing report, you can cross probe to the Netlist Analyzer tool.
- In the PAR timing report, you can cross probe to Netlist Analyzer and Physical Designer (Placement Mode and Routing Mode) tools.

To cross probe an element from one view to another, follow below steps:

1. Right-click an element in any view.
2. Choose **Show in** and choose the desired view from the pop-up menu.

11. Programming Files

After you have created and verified your design, you can use the final output data file to download or upload a bitstream to or from an FPGA device using the Radiant Programmer.

The bitstream file contains all configuration information from the physical design that define the internal logic and interconnections of the FPGA, as well as device-specific information from other files associated with the target device. Table 11.1 lists all the final output data file formats and their descriptions.

Table 11.1. Final Output Data File Formats and their Descriptions

File Formats	Descriptions
Data File	A data file can be a hex, or bitstream file. Each of these files is based upon the IEEE programming standard.
Bitstream	Data files used for configuring volatile memory (SRAM) of our FPGAs.
Hex	Hexadecimal PROM data files used to program into external non-volatile memory, such as parallel or Serial Peripheral Interface (SPI) Flash devices.

For more information, refer to the Programming Files and Programmer sections in the Lattice Radiant Programming Tools User Guide from the Radiant software Help menu.

12. Reports

In the ISE Design Suite software, the reports created during synthesis or implementation can be accessed under **Design Summary**.

In the Radiant software, you can click on the **Reports** tab, which is open by default on the Radiant software workspace. Alternately, you can go to **View** > **Reports**.

Each step on the design flow has its own set of reports from resource usage to timing analysis provided that you have enabled the timing analysis on the process toolbar. The examples of Radiant software reports are as shown in Figure 12.1 and Figure 12.2.

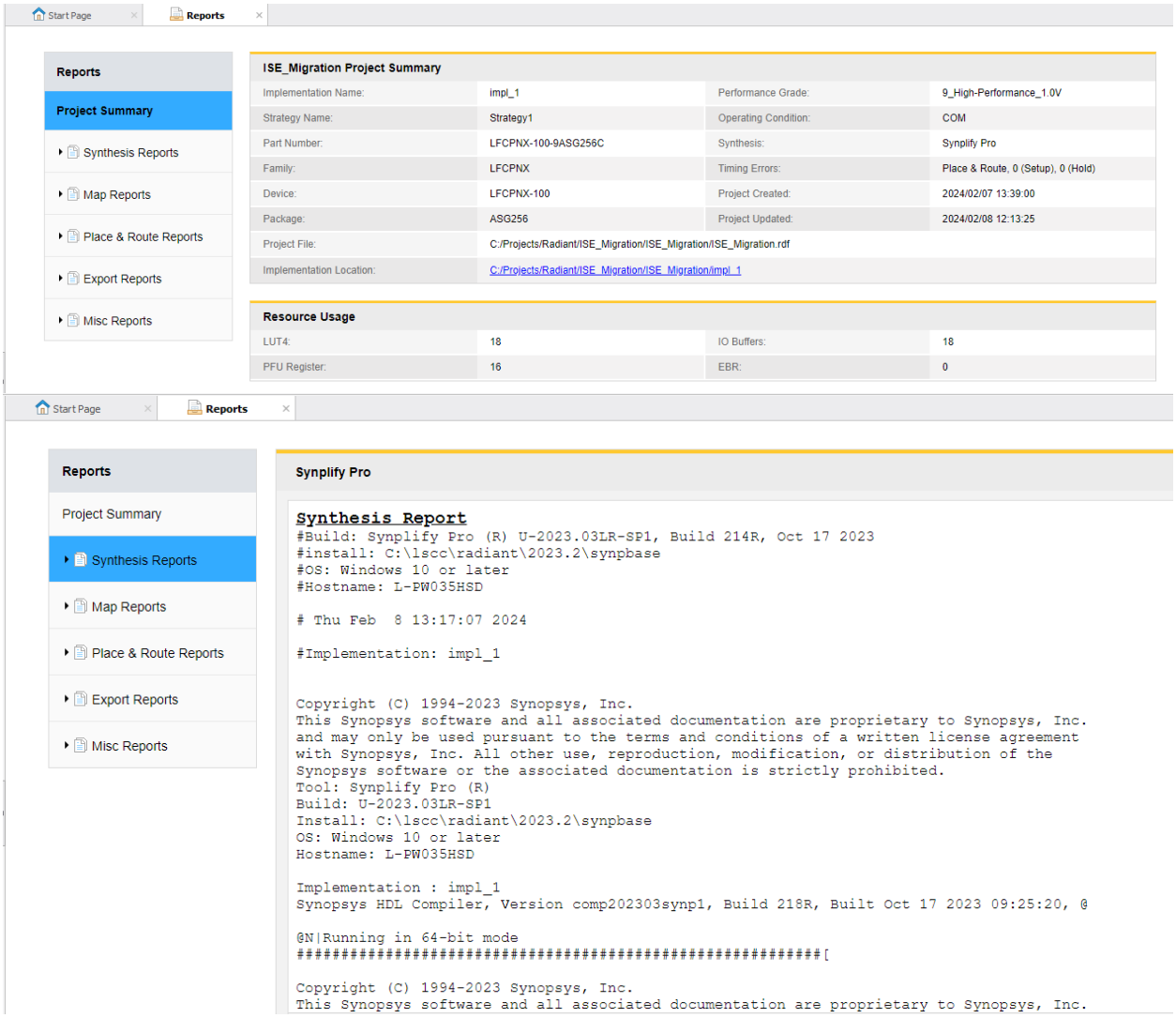

Figure 12.1. Project Summary and Synthesis Reports in Radiant Software

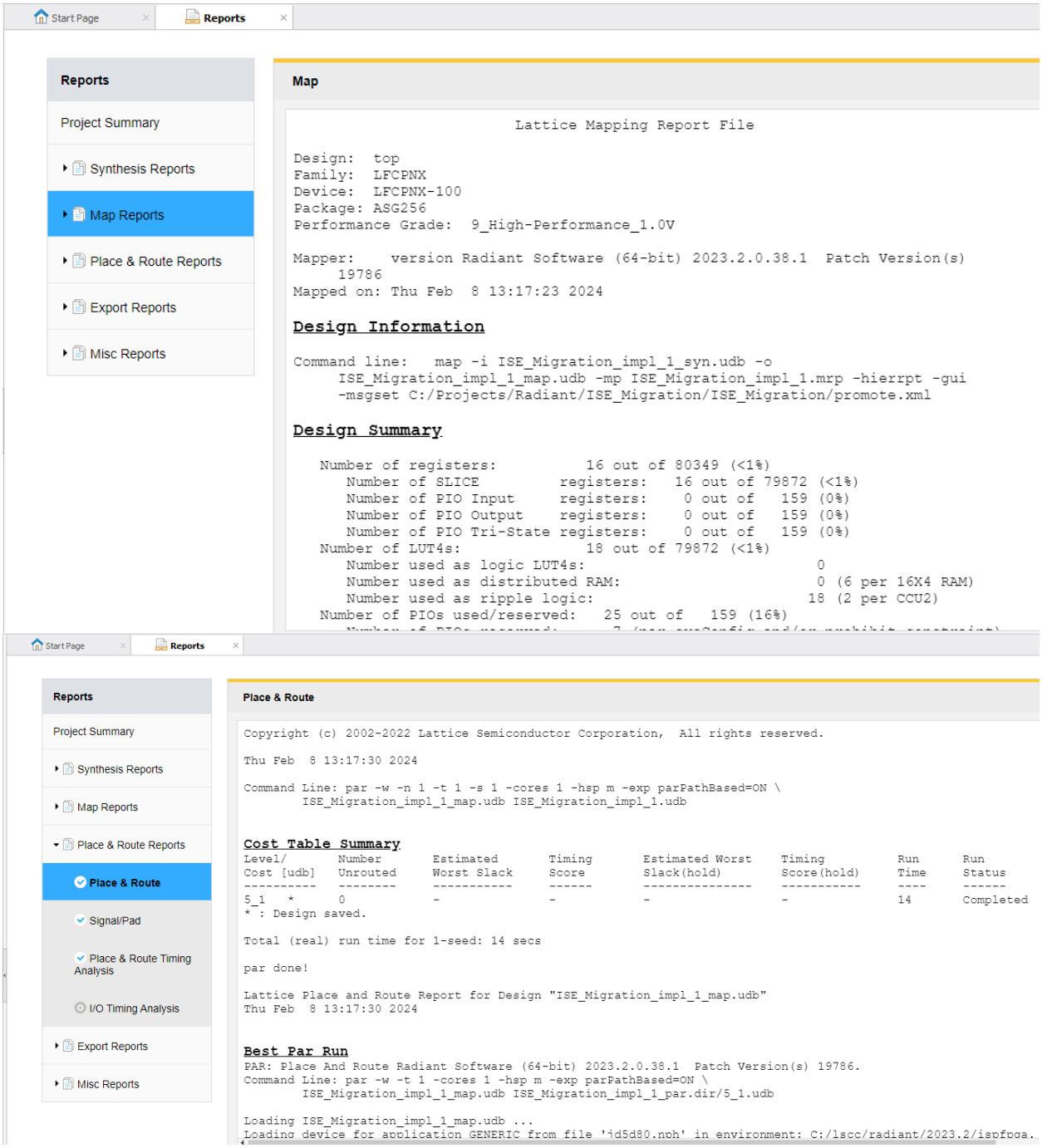

Figure 12.2. Map and PAR Reports in Radiant Software

For more information, refer to the Reports section in the Lattice Radiant User Guide from the Radiant software Help menu.

References

- Lattice Radiant Software web page
- Lattice Solutions IP Cores web page
- Lattice CertusPro-NX web page
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/en/Support/AnswerDatabase.

Revision History

Revision 1.0, March 2024

Section	Change Summary
All	Initial release.

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