Product Bulletin

November 2023 **#PB231101 Rev 1.0**

SPI Programming Failure Modes in Specific Use Scenarios with Platform Manager 2, MachXO2, and MachXO3 Products and Work-Around Solutions

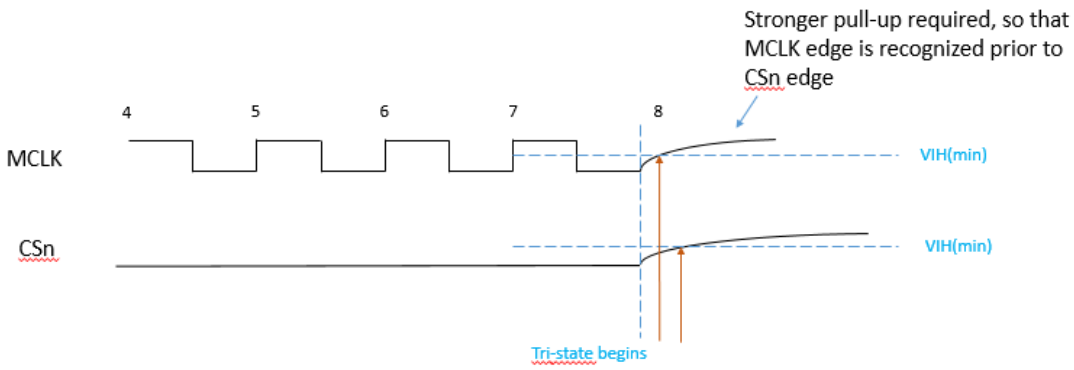
Lattice is issuing this Product Bulletin to inform that two potential failure modes are possible when programming external SPI memories via the JTAG-to-MSPI bridge feature with Platform Manager 2, MachXO2, and MachXO3 devices. The failure modes are limited use cases and only a few customers will be impacted. However, for those customers who are using one of these devices in the modes described below, there is a risk of programming and/or verification failure of the external SPI memory.

Known Issues

Issue #1: Race condition between CS and MCLK at the end of SPI transaction

This race condition occurs when the JTAG-to-MSPI bridge is used to erase/program/verify the external SPI device. The JTAG command to release control of the SPI embedded function block (EFB) will disable both CSn and MCLK outputs at the same time. If CSn wins the race, the SPI device does not see the final MCLK edge. In this situation, the SPI device ignores the final data or command and a programming error occurs. By using different strength pull-ups resistors, MCLK can be forced to rise before CSn (as shown in Figure 1), to prevent programming errors. Lattice has historically recommended that MCLK use an external 1 k pull-up resistor (FPGA-TN-02154 MachXO2 Hardware Checklist and FPGA-TN-02155 MachXO2 Programming and Configuration User Guide) and CSn relies on the weak pull-up of the I/O or an external 10 k pull-up resistor that is recommended in FPGA-TN-02078 Dual Boot and Background Programming PM2. Therefore, if the existing recommendations are followed, this issue should not be encountered for most customers. It is possible that resistor values must be adjusted depending upon design dependent routing and trace loads in order to ensure proper edge relationships.

Figure 1. Issue #1: Race Condition between CSn and MCLK



Issue #2: Race condition between MCLK OE and rising transition

A second issue is a race condition that occurs between MCLK changing logic states and the release of the internally generated MCLK output enable (OE). This issue also results from the JTAG command to release control of the SPI EFB. At the point of release, MCLK transitions from low to high at the same time MCLK's output is disabled. In some cases, the timing is such that MCLK's output is disabled while the logic level is in transition. This creates ringing on the MCLK signal (as shown in Figure 2). Newer SPI devices designed to operate at faster clock rates (above 50 MHz) and at lower supply values (such as Vcc-min = 2.3 V) will see the ringing as false clock pulses and ignore the data or command. Thus, resulting in a programming error.

Older SPI devices that operate as slower clock rates (below 50 mHz) and tighter supply values (with Vcc-min = 2.7 V) are less prone to be affected by the ringing and do not have programming errors. In older SPI devices, the input impedance and input capacitance tend to attenuate the ringing. In addition, the range in the input logic thresholds (VIN_Low and VIN_High) is wide enough that the attenuated ringing does not cross a threshold resulting in a false clock. See the Hardware Work-Around section for solutions to the MCLK ringing when using newer SPI devices.

The ringing issue has also been observed in legacy customer designs as the older SPI devices are becoming unavailable or reaching end-of-life and replaced with newer, faster, and lower voltage SPI devices.

Figure 2. Issue #2 – Race Condition between OE and Logic Level can result in ringing.

No Customer Application Issue when:

1. An external SPI memory is not used in the customer application.
2. The external SPI memory is not connected to the hardened EFB SPI connections.
3. The external SPI memory is not programmed using the JTAG-to-MSPI bridge within the FPGA device. Safe examples include:
    a. The external SPI memory is programmed before PCB assembly.
    b. The external SPI memory is programmed directly on the PCB from a bed-of-nails tester.
    c. The external SPI memory is programmed on board using a method that does not include the JTAG-to-MSPI bridge within the FPGA.

Customer Application may be exposed when:

1. The Platform Manager 2, MachXO2, or MachXO3 boots from an external SPI memory device and all the following apply:
    a. The SPI memory device is designed to operate at a clock rate of 50 MHz or more (even if the design itself uses a much lower clock frequency).

b. The SPI memory device is designed to operate at low voltage logic levels such as LVCMOS 2.5 V, LVCMOS 1.8 V, or similar (even if the design itself does not operate at a lower voltage).

c. The SPI memory is programmed using the JTAG-to-MSPI bridge within the FPGA.

Hardware Work-Around

This section provides the hardware guidelines that mitigate both of the race conditions described above: the race condition between CSn and MCLK and the race condition between the OE of MCLK and the rising transition. These guidelines provide a generic architecture that supports tuning between the two race conditions and the characteristics of the PCB and various SPI devices. The guidelines below are most suitable for new designs and design re-spins.

This architecture calls for a low-pass filter at the input of the SPI clock pin. The low-pass filter attenuates the ringing issue but adds a negative delay to the race condition between CSn and MCLK. An external delay circuit is used to restore the correct timing between CSn and MCLK and compensates for the low-pass filter delay.

Figure 3 shows the external delay circuit using a logic buffer with an R-C delay on the input. This circuit provides a wide range of RC delays by adjusting the values of RPU_CS and CDELAY. Table 1 lists some typical values and corresponding delays for prototyping. Production values will depend on board layout and component selection (including the MCLK low-pass filter values). A current limiting resistor (RLIM) is needed to isolate the capacitive loading of CDELAY from the CSSPIN driver and a value of 200 Ω will work for the supported LVCMOS I/O standards (3.3 V to 1.2 V).

Figure 3. Recommended SPI Interface Circuit with Buffer Delay.

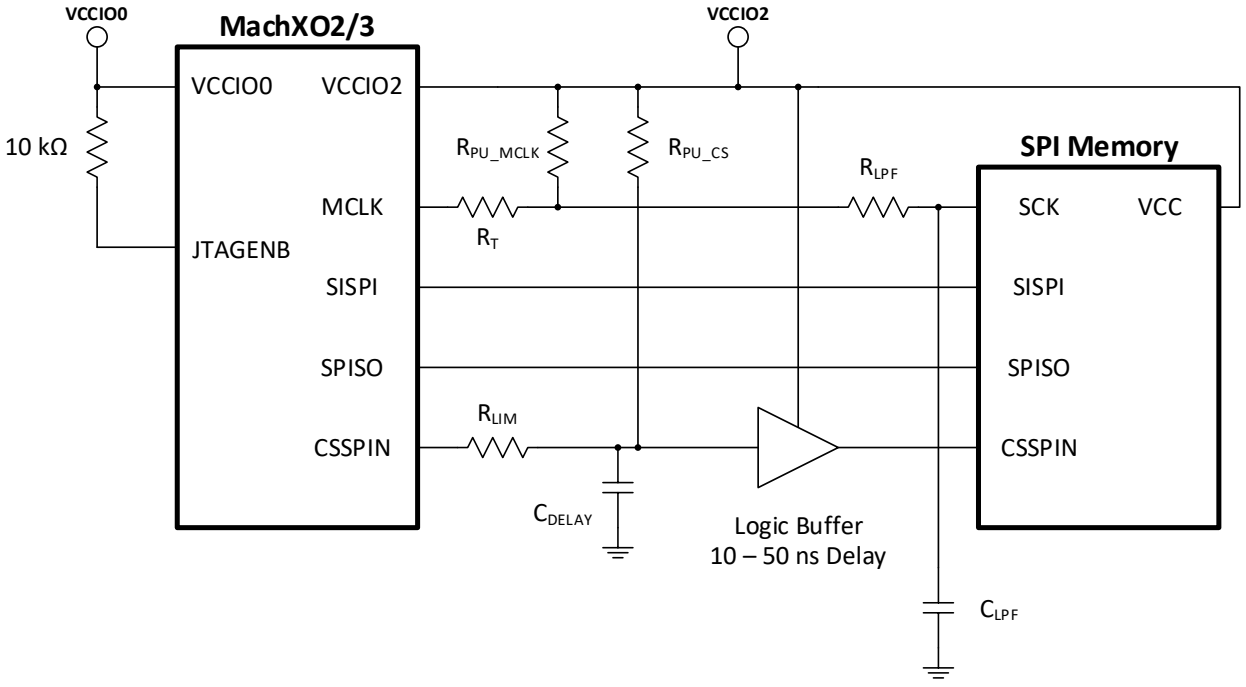


Table 1. Buffer Delay Circuit Values.

R_{PU_CS} (k Ω)	C_{DELAY} (pF)	Approximate Delay (ns)
1	10	10
2	10	20
3.3	15	50

While Figure 3 shows the use of a logic buffer as part of the delay circuit, any number of other logic elements could be used; including but not limited to the following:

- AND gate
- OR gate
- Cascaded NAND gates
- Cascaded NOR gates
- Cascaded Inverters

The final design consideration for the buffer delay circuit is the voltage divider of RPU_CS and RLIM. When CSSPIN goes low the divided voltage value must meet the input-low specification for the buffer (or other logic element). Given the value of 200 Ω for RLIM, RPU_CS should be 1 kΩ or greater for typical LVCMOS standards.

Ultimately, the design depends upon device availability and/or extra resources already in the schematic. One option that will not work is using the FPGA as a buffer because, the buffer is not in the fabric until after the device is configured by the pattern in the SPI device.

Figure 4 zooms in on the recommended SPI interface circuit for the clock signal (MCLK). On the left, the transmission line matching resistor (RT) is located as close to the MachXO2/3 as possible. The value of RT combined with the output impedance of the MachXO2/3 should match the PCB trace impedance. Typical values for RT range from 22 Ω to 33 Ω for a PCB trace impedance of 50 Ω.

The pull-up resistor (RPU_MCLK) will pull the clock signal high when MCLK's output is disabled or tri-stated. In the past, a recommended value of 1 k was used to solve the CSn to MCLK race condition. However, an external circuit is now recommended to provide the required delay and the strong pull-up value makes the ringing issue more severe. A value between 4.7 k and 10 k should be used for RPU_MCLK.

The transmission line for MCLK should be kept as short as possible (and length matched with the data SPI signals). On the right side of Figure 4 the R-C low-pass filter (RLPF & CLPF) is shown. This filter should be located as physically close to the SPI clock input as possible to maintain signal integrity of the clock signal. Table 2 lists typical values for prototyping; production values will depend on PCB layout and final component selection.

Figure 4. Recommended SPI MCLK Interface Circuit.

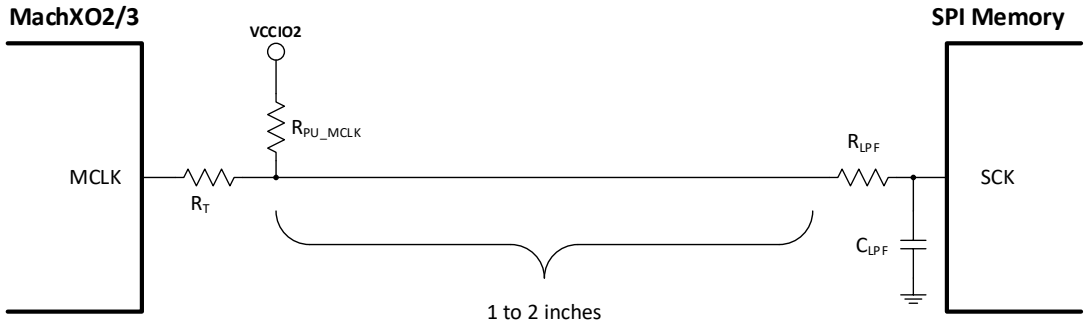


Table 2. Recommended SPI MCLK Low-Pass Filter Values.

R_{LPF} (Ω)	C_{LPF} (pF)	Low Pass Corner (f_3 MHz)	Delay (ns)
200	16	50	3.2
100	16	100	1.6
50	32	100	1.6
33	48	100	1.6

Summary

Customers are advised to use the hardware work-around described in this special product bulletin to prevent any possibility of field failures or performance marginality. Lattice Semiconductor has no plan to further update the Platform Manager 2, MachXO2, or MachXO3 product Families.

Other use cases and solutions are possible, including for legacy designs where PCB updates or rework is not possible. As necessary, contact Lattice Applications and Solutions using the contact instructions below.

RELATED DOCUMENTS

The following Lattice Semiconductor documents will be updated with a reference to this product bulletin:

FPGA-TN-02154 – MachXO2 Hardware Checklist

FPGA-TN-02155 – MachXO2 Programming and Configuration Usage Guide

FPGA-TN-02061 – MachXO3 Hardware Checklist

FPGA-TN-02055 – MachXO3 Programming and Configuration Usage Guide

FPGA-TN-02175 – L-ASC10 and Platform Manager 2 Hardware Checklist

FPGA-TN-02078 – Dual Boot and Background Programing with Platform Manager 2

AN6091 – Powering Up and Programming Platform Manager 2 and L-ASC10

CONTACT

If you have any questions or require additional information, please open a technical support case at:

www.Latticesemi.com/techsupport

Sincerely,

Lattice Semiconductor Platform Manager 2, MachXO2, and MachXO3 Product Line Management

Revision History

Date	Version	Description of Revisions
November 20, 2023	1.0	Initial Release