



Importing Platform Designer IP into MachXO3D Designs

User Guide

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ASC	Analog Sense and Control
ASCVN	Analog Sense and Control Virtual Machine
EFB	Embedded Function Block
FPGA	Field-Programmable Gate Array
GPIO	General Purpose Input/Output
PFR	Platform Firmware Resiliency
PIO	Programmed Input/Output
PTM2	Platform Manager II
RTL	Register-Transfer Level

1. Introduction

This user guide shows how to integrate power supply monitoring and sequencing into MachXO3D™ designs. While the Platform Designer tool in Lattice Diamond® does support MachXO3D based designs with L-ASC10 devices, similar to MachXO2 or MachXO3 based designs, the tool creates a top-level design based on the ASC interface and power sequence. This document describes modifications to the Platform Designer tool that supports exporting an IP package that can be easily instantiated in a separate MachXO3D top-level design, as shown [Figure 1.1](#). For example, to provide a secure power sequencing to the Platform Firmware Resiliency (PFR) solution. The exported module could also be instantiated in other Lattice FPGA designs.

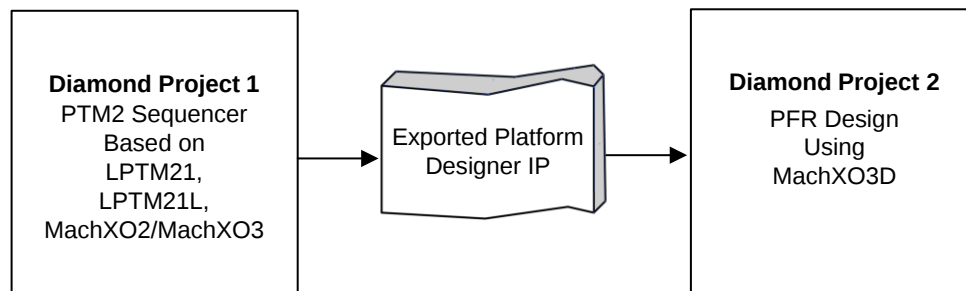


Figure 1.1. Exporting Platform Manager 2 IP

[Figure 1.2](#) shows the following key components of the exported IP:

- The ASC virtual machine (ASCVM) that handles the three-wire interface between the FPGA and the various ASC devices.
- The Clock and Reset module that generates clocks and enables the start of the sequencer. Note that the signal *ptm_enable_seq* is automatically added to the IP as part of the export process and is used to enable the power sequence after the PFR decides that it is safe to do so.
- The Logic Sequence interfaces with other signals (not in bold) that are examples of user defined handshaking signals between the Platform Designer sequence and the PFR controller. One is to signal to the PFR that the power up sequence is complete and the other provides a means for the PFR to shut the power down. Both signals need to be designed into the Platform Designer and PFR logic by the user. Additional signals to handle fault conditions, or other situations, can easily be added by the user.

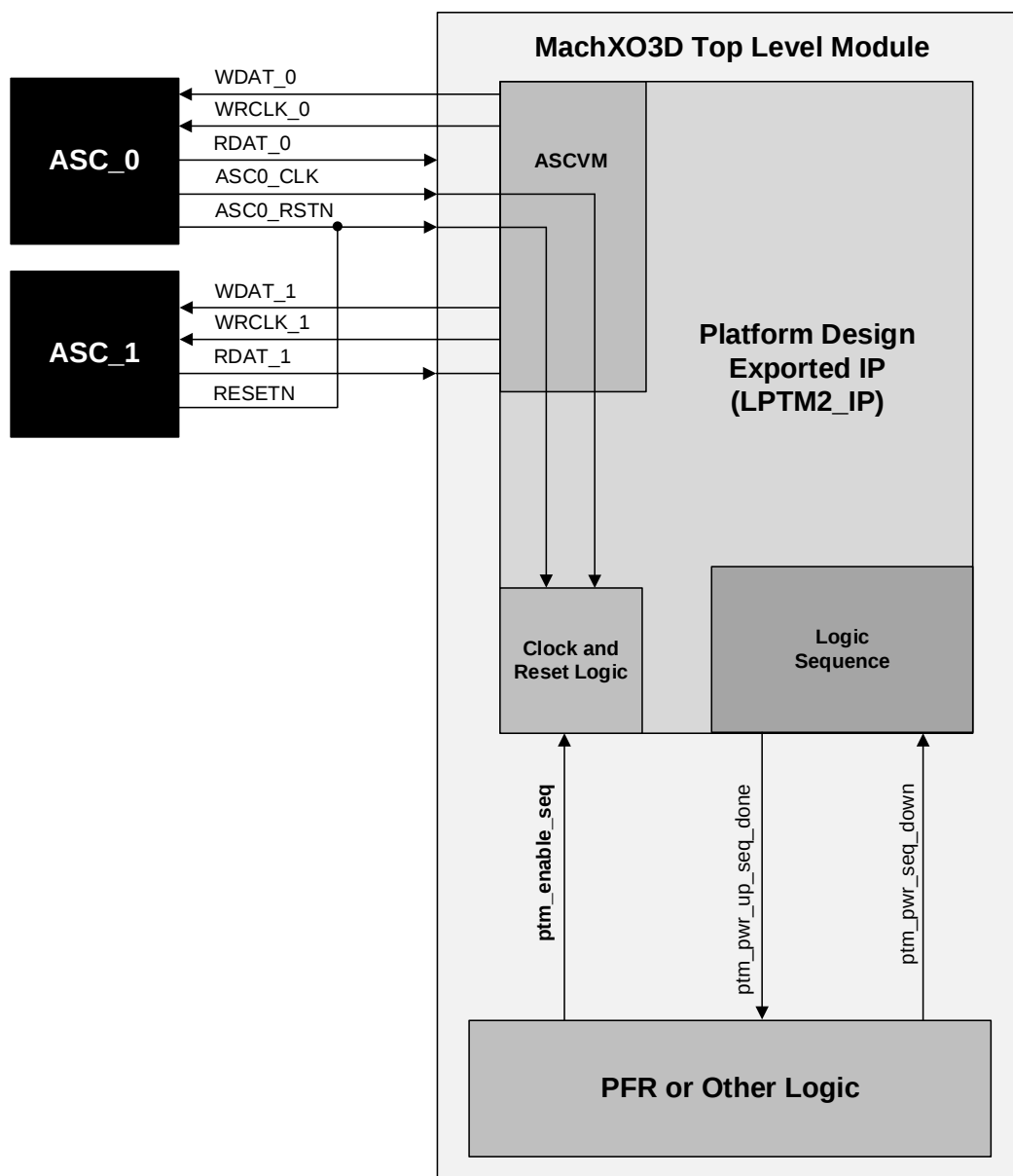


Figure 1.2. Platform Designer Exported IP within MachXO3D Top-Level Design

2. Exporting a Platform Manager 2 Design

A Platform Manager 2 design can be based on several FPGA devices and the exported module will be generic so that it can be included into a MachXO3D design. Thus, existing designs based on any of the following can be exported into the MachXO3D design: LPTM21, LPTM21L, MachXO2, MachXO3, and MachXO3D.

The export option is selected by checking *Export Platform Designer IP* in the *Global* view of the *Device Options* tab, as shown in [Figure 2.1](#).

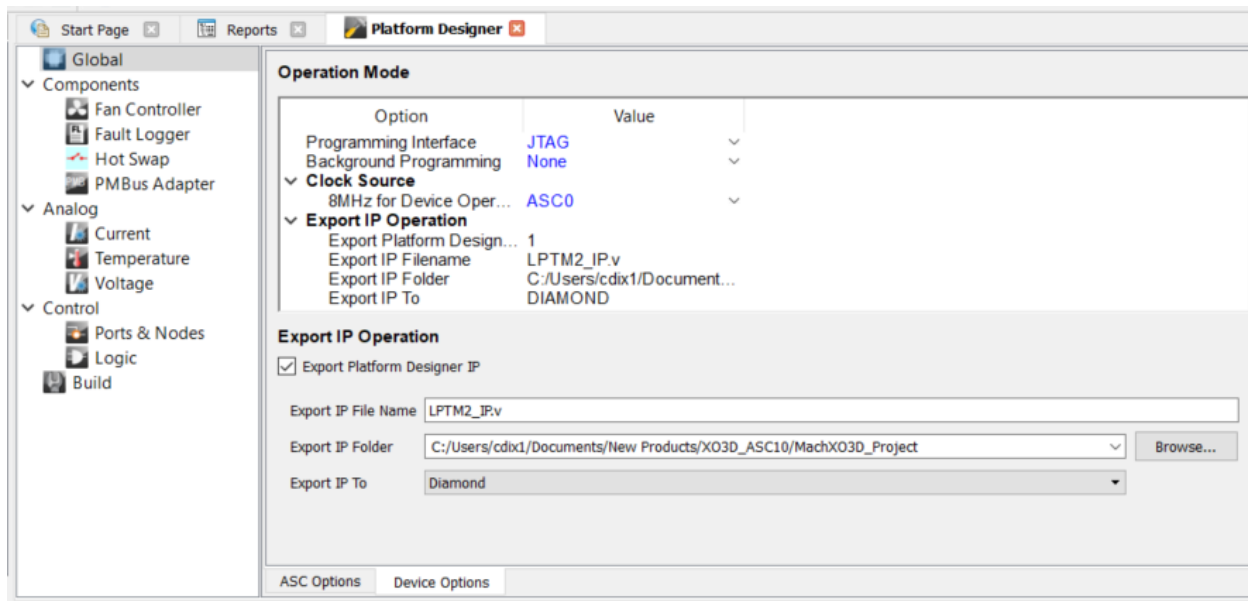


Figure 2.1. Global Device Options – Export IP

When *Export Platform Designer IP* is checked, the following fields are visible and editable:

- **Export IP File Name**
By default, Platform Designer creates a top-level design file based on the project name with the added prefix of `psb_`. This file is generated when the *Compile* button is clicked in the *Build* view. For example, a project named `Power_Sequence.ptm` results in the file name `psb_Power_Sequence.v` as the default export file name. In [Figure 2.1](#), the file name is changed to `LPTM2_IP.v` and the exported IP module name reflects the file name (`LPTM2_IP`).
- **Export IP Folder**
This supports browsing to and creating a folder for the exported files to be written into. In addition to the exported IP design file, several other files and folders are written into this location. The other files and folders are described in a later section.
- **Export To**
This drop down list allows the export function to target various Lattice devices. For the MachXO3D and other Diamond supported devices, the selection should be Diamond. The other options support exporting the Platform Designer IP to Lattice Radiant™ projects. This is covered in separate documents.

3. Excluding the EFB Module

In many designs, the embedded function block (EFB) of the MachXO2 or MachXO3 device is needed for a user function. By default, Platform Designer instantiates the EFB and connects the primary I²C port to reserve the port for programming functions. However, when the FPGA is erased, the I²C port is available for programming regardless if the EFB is part of a design or not. In order to free up the EFB for user functions, *Enable EFB Module* should be unchecked in the *Inserted HDL* tab of the *Logic* view as shown in Figure 3.1.

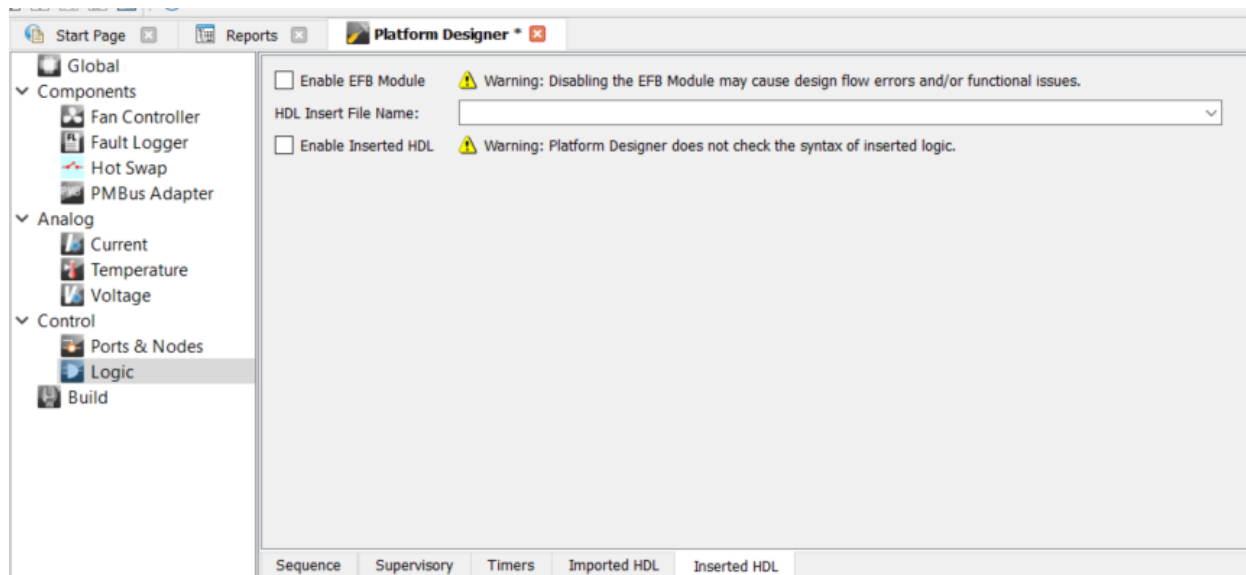


Figure 3.1. Disable the EFB Module

4. Building and Exporting

The *Compile* button, as shown in [Figure 4.1](#), in the *Build* view generates the Platform Designer IP and writes it (and associated sub-modules) into the target folder that is specified in [Figure 2.1](#).

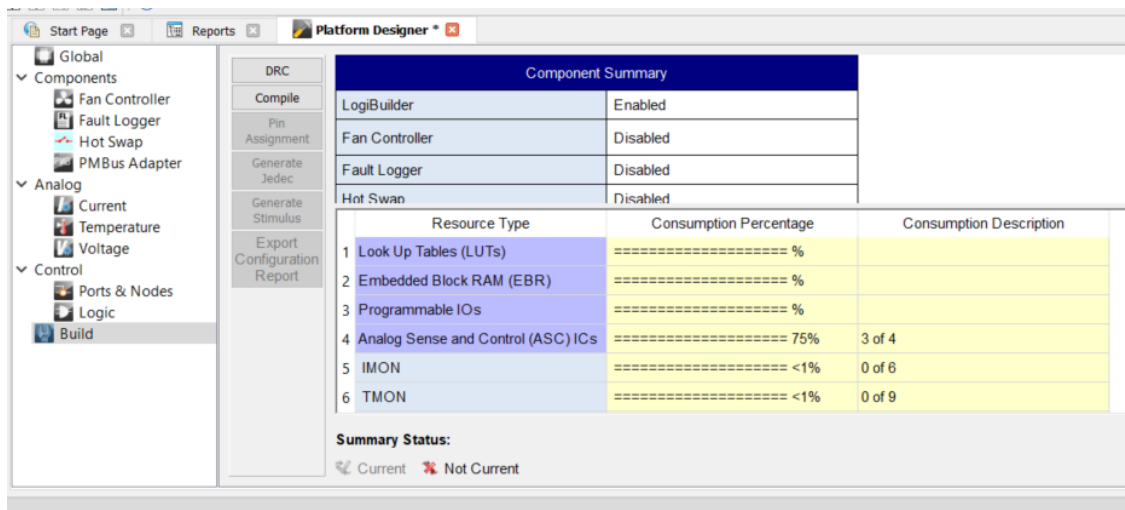


Figure 4.1. Compile and Export

5. Importing the Platform Manager 2 IP into a MachXO3D Design

A separate or new MachXO3D design should be started, or modified, in the *Device Selector* window without any external ASC devices, as shown in [Figure 5.1](#).

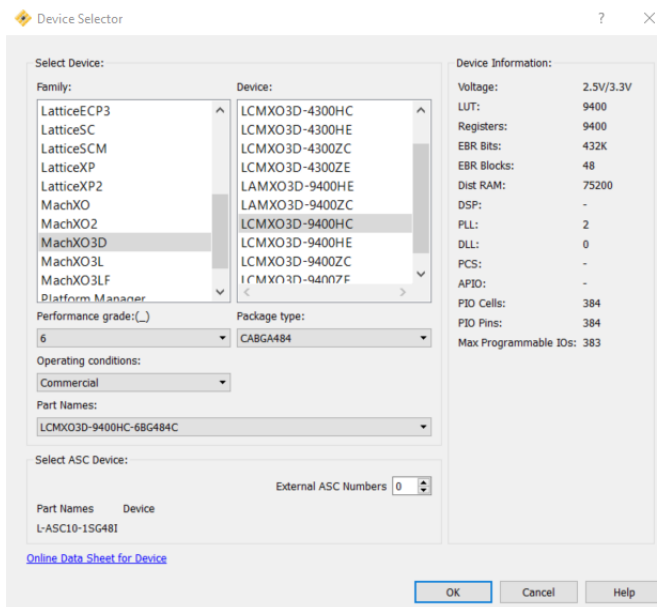


Figure 5.1. Only MachXO3D Selected in Device Selector Window

Right-click on *Input Files* and select *Add > Existing File* from the drop-down menu, as shown in [Figure 5.2](#).

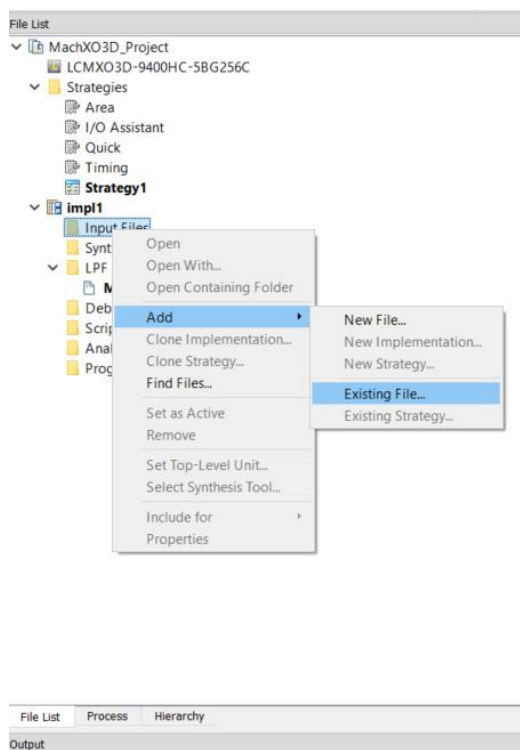


Figure 5.2. Adding Existing File - Popup Menu

Then select the following files (individually or in groups):

- LPTM2_IP.v
- LPTM2_IP_tmpl.v
- Power_Sequencer_lgb.v
- efb_timer_config.v
- RDAT.v
- WDAT.v
- CLKRST/src/rtl/Verilog/clkfst.v
- CLKRST/src/rtl/Verilog/clkfst_core.v
- ASCVM/src/rtl/Verilog/ASCVM.v
- ASCVM/src/rtl/Verilog/ASCVM_DATAPATH.v
- ASCVM/src/rtl/Verilog/ASCVM_RAM_EBR.v
- ASCVM/src/rtl/Verilog/ASCVM_RAM_DIST.v

Note that the first three file names depend on the original Platform Designer project name and the export IP file name. Right-click on the template file (PTM_IP_tmpl.v) and select *Exclude from Implementation* from the drop-down menu. The result should look similar to [Figure 5.3](#).

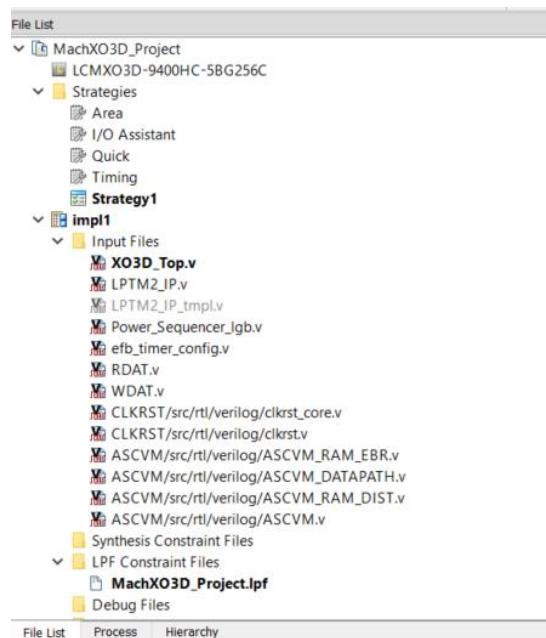
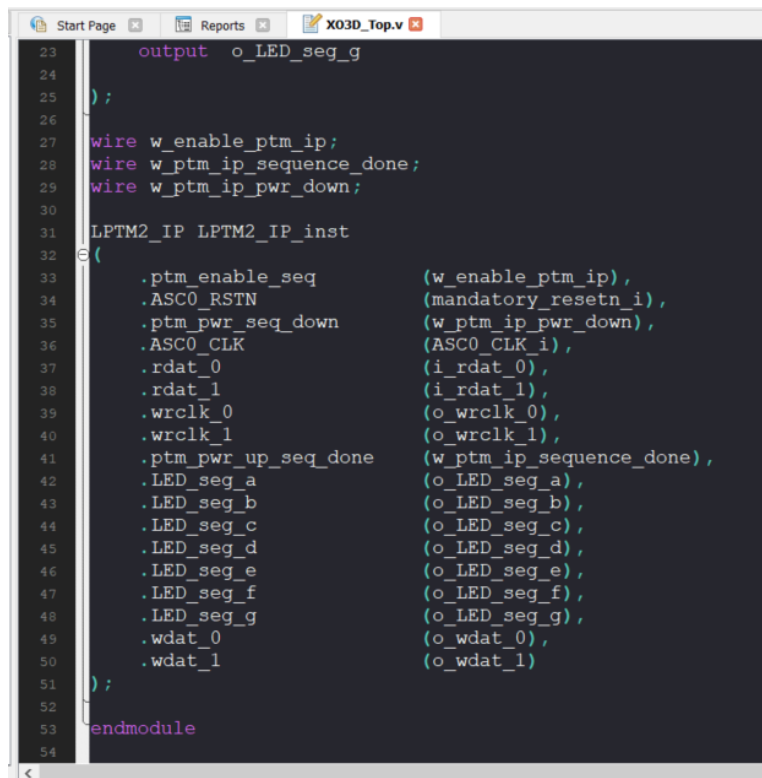


Figure 5.3. MachXO3D Project with Platform Designer IP Added to Input Files

Open the template file (PTM_IP_tmpl.v) and copy all (CTRL-A, CTRL-C) and paste (CTRL-V) into the top-level module. Insert the module name before the instantiation and connect to the top-level inputs, outputs, and wires, as shown in [Figure 5.4](#).



```

23     output o_LED_seg_g
24
25 );
26
27 wire w_enable_ptm_ip;
28 wire w_ptm_ip_sequence_done;
29 wire w_ptm_ip_pwr_down;
30
31 LPTM2_IP LPTM2_IP_inst
32 (
33     .ptm_enable_seq      (w_enable_ptm_ip),
34     .ASC0_RSTN          (mandatory_resets_i),
35     .ptm_pwr_seq_down   (w_ptm_ip_pwr_down),
36     .ASC0_CLK           (ASC0_CLK_i),
37     .rdat_0             (i_rdat_0),
38     .rdat_1             (i_rdat_1),
39     .wrclk_0            (o_wrclk_0),
40     .wrclk_1            (o_wrclk_1),
41     .ptm_pwr_up_seq_done (w_ptm_ip_sequence_done),
42     .LED_seg_a          (o_LED_seg_a),
43     .LED_seg_b          (o_LED_seg_b),
44     .LED_seg_c          (o_LED_seg_c),
45     .LED_seg_d          (o_LED_seg_d),
46     .LED_seg_e          (o_LED_seg_e),
47     .LED_seg_f          (o_LED_seg_f),
48     .LED_seg_g          (o_LED_seg_g),
49     .wdat_0             (o_wdat_0),
50     .wdat_1             (o_wdat_1)
51 );
52
53 endmodule
54

```

Figure 5.4. Platform Manager 2 IP Inserted into MachXO3D Top-Level Design

The signal `.ptm_enable_seq` is generated as part of the Export Platform Design IP process. The MachXO3D top-level module has the responsibility of setting this signal true and keeping it true. Either tie it true with `1'b1`, and the Platform Design IP starts at the same time as the rest of the MachXO3D IP. Another option is to connect it to a wire or register that is driven true after the IP within the MachXO3D starts up. For example, after the PFR IP determines it is safe to start the power up sequence for the platform. This signal is connected to the ASCVM reset logic and should only transition from false to true. If this signal transitions from true to false (1 to 0), then power supplies on the platform assume the reset state without sequencing off and damage could occur to some components.

The signal `.ptm_pwr_up_seq_done` is a user created PIO port, in Platform Designer, just like the seven-segment LED outputs (`.LED_seg_a` - `.LED_seg_g`). It is up to the user to create the name of this output and to reset the signal at power up and set the signal when the sequence is complete in the Platform Designer Logic Sequence.

The signal `ptm_pwr_seq_down` is also a user created PIO port in Platform Designer, as shown in [Figure 5.5](#). It is up to the user to create the name of this input signal and to sequence off the power supplies in Platform Designer logic when the MachXO3D logic activates this signal.

The MachXO3D design can interface with these Platform Designer ports either directly in RTL or indirectly thru the GPIO interface of the PFR solution.

	PIO Count	Logical Name	Group By	Type	Register Type	Reset Level
374	373	PIO370	N/A	IN...	Registered	Don't Care
375	374	PIO371	N/A	IN...	Registered	Don't Care
376	375	PIO372	N/A	IN...	Registered	Don't Care
377	376	PIO373	N/A	IN...	Registered	Don't Care
378	377	PIO374	N/A	IN...	Registered	Don't Care
379	378	PIO1930	N/A	IN...	Registered	Don't Care
380	379	PIO1940	N/A	IN...	Registered	Don't Care
381	380	ptm_pwr_seq_down	N/A	IN...	Registered	Don't Care
382	381	ptm_pwr_up_seq_done	N/A	OUT	Registered	Set Low

Ports Nodes GPIO HV Outputs

Figure 5.5. User Defined PIO Ports in Platform Designer

6. Summary

With the Platform Designer IP imported into the MachXO3D top-level module, both the Power Sequence design and the MachXO3D design can undergo the typical iterative design process. Changes to the Power Sequence are updated with the *Compile* button in the *Build* view ([Figure 4.1](#)) and the MachXO3D firmware or RTL can be updated and rebuilt using the standard Diamond interface without any hand-modifications to generated RTL.

References

- [L-ASC10 Data Sheet \(FPGA-DS-02038\)](#)
- [Platform Manager 2 Data Sheet \(FPGA-DS-02036\)](#)
- [MachXO2 Family Data Sheet \(FPGA-DS-02056\)](#)
- [MachXO3 Family Data Sheet \(FPGA-DS-02032\)](#)
- [MachXO3D Family Data Sheet \(FPGA-DS-02026\)](#)
- [Lattice Sentry Root of Trust Demo Setup for MachXO3D User Guide \(FPGA-UG-02114\)](#)
- [Lattice Sentry PLD Interface IP Core - Lattice Propel Builder User Guide \(FPGA-IPUG-02106\)](#)
- [MachXO3D Platform Firmware Resiliency Manifest and Log Management \(FPGA-UG-02025\)*](#)
- [MachXO3D Platform Firmware Resiliency Out-of-Band I2C Command Protocol \(FPGA-UG-02032\)*](#)

***Note:** To access this document, contact your Lattice representative

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, October 2022

Section	Change Summary
All	Initial release.



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