DisplayPort and Video Scaler Demonstration

User Guide

FPGA-UG-02201-1.0

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AXI	Advanced eXtensible Interface
BPC	Bits Per Color
CLINT	Core-local Interrupt Controller
DP Rx	DisplayPort Receiver
DP Tx	DisplayPort Transmitter
EDID	Extended Display Identification Data
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
GUI	Graphical User Interface
HBR	High bit rate
MPCS	Multi-protocol physical coding sublayer
MSA	Main Stream Attribute
MST	Multi-Stream Transport
PLIC	Platform-level Interrupt Controller
PLL	Phase locked loop
PPC	Pixels Per Clock
RISC-V	Reduced instruction set computer version five
SERDES	Serializer de-serializer
SST	Single Stream Transport
UART	Universal asynchronous receiver-transmitter
VS	Video Scaler

1. Introduction

This demonstration illustrates the integration of the Lattice DisplayPort (DP) IP and Lattice Video Scaler IP. The Lattice Semiconductor CertusPro™-NX Evaluation Board allows designers to evaluate the features of the CertusPro-NX Field Programmable Gate Array (FPGA) and assists them with rapid prototyping of their designs. The DisplayPort and Video Scaler demonstration showcases an end-to-end Video Scaling system. It includes Lattice DP IP and Lattice Video Scaler IP as the primary components. The demonstration system is schematically shown in Figure 1.1. It takes in a video from a DisplayPort source, like a desktop, scales the resolution up or down and re-transmits the scaled video through a DisplayPort connector to a DisplayPort sink, like a computer monitor. As shown in the Figure 1.1, the DP input is received by the DisplayPort IP receiver (DP Rx), scaled by Video Scaler and sent to the DisplayPort IP transmitter (DP Tx) to be sent to the DP connector. There are additional components in the demonstration system, like a RISC-V processor, AXI interconnect and UART, which are used to read the status of DP IP and display that in an external terminal.

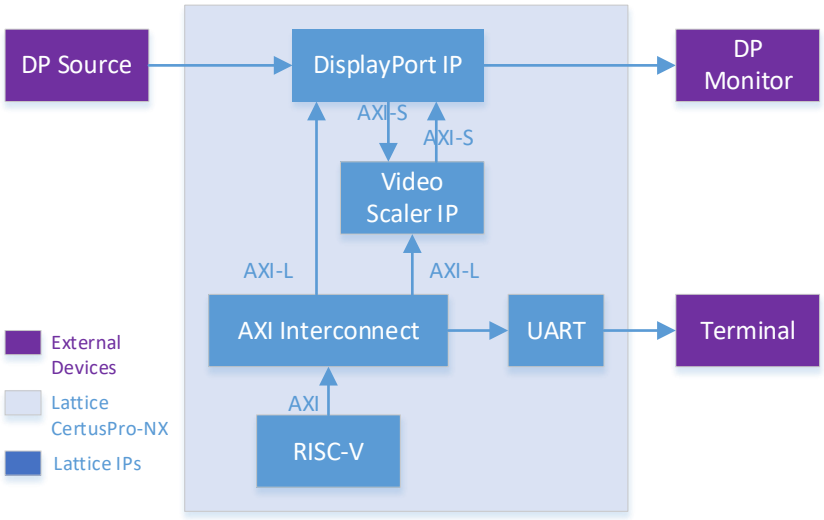

Figure 1.1. DP Video Scaler Hardware Top Level Diagram

The demonstration system is built on Lattice CertusPro-NX Evaluation board, along with the Lattice Modular FMC Adapter, Lattice DisplayPort Transmitter Daughter Card, and Lattice DisplayPort Receiver Daughter Card (collectively referred to as DP FMC Daughter Card Kit). The demonstration design is a SoC (System on a Chip) design created as a Lattice Propel™ project. The propel project can be opened, modified if necessary and implemented using Lattice Radiant. The final bitstreams are also provided which can be directly programmed on the board and tested out. The design supports an external UART terminal for controlling the demo and for status display. The details of the Propel design, the included bitstreams, and the bring-up procedure are given in the following chapters.

1.1. Demonstration Requirements

The hardware, software and cable requirements for this demonstration are provided in the following section.

1.1.1. Hardware

This demonstration requires the following hardware components:

- CertusPro-NX Evaluation Board
- Lattice Modular FMC Adapter
- Lattice DisplayPort Transmitter Daughter Card
- Lattice DisplayPort Receiver Daughter card
- HBR2 (5.4 Gbps x4) capable DP source and sink devices
- Power supply for the evaluation board

1.1.2. Software

This demonstration requires the following software components:

- Lattice Propel Builder Software version 2023.1 or higher
- Lattice Radiant Software version 2023.1 or higher
- Radiant Programmer System software for downloading the FPGA bitstream
- A terminal application like PuTTY

1.1.3. Cable

Two DisplayPort cables supporting version 1.4 or higher

1.2. Configurations and Hardware Description

1.2.1. Supported configurations

The included Propel project is built using 2 pixels per clock (PPC) data path for DP and Video Scaler IPs. The project can also be modified to support 4 PPC data path. Two bitstreams, one for 2 PPC data path and the other for 4 PPC data path are included in the demo package. Both versions support dynamic configuration of Video Scaler and input/output resolutions.

The bitstream for 2 PPC supports live video scaling for the following configurations (Bicubic algorithm):

- 720p to 1080p upscaling
- 1080p to 720p downscaling
- 1080p to 1080p pass through
- 720p to 1440p upscaling
- 1440p to 720p downscaling
- 720p to 720p pass through
- 1080p to 1440p upscaling
- 1440p to 1080p downscaling
- 1440p to 1440p pass through

The bitstream for 4 PPC supports live video scaling for the following configurations (Nearest neighbor algorithm):

- 1080p to 2160p upscaling
- 2160p to 1080p downscaling
- 2160p to 2160p pass through
- 1440p to 2160p upscaling
- 2160p to 1440p downscaling
- 1440p to 1440p pass through
- 1080p to 1440p upscaling
- 1440p to 1080p downscaling
- 1080p to 1080p pass through

1.2.2. Hardware setup

Figure 1.2 shows the hardware configuration used for this demonstration. This demonstration works on the CertusPro-NX Evaluation board with the DP FMC Daughter Card kit connected to it. The kit consists of Modular FMC Adapter, DisplayPort Transmitter Daughter Card, and DisplayPort Receiver Daughter Card. After mounting the DP FMC daughter board kit on to the CertusPro-NX evaluation board, connect DP source and sink through two different DP cables. A commonly used DP source is a desktop or Laptop PC with DP output and a common DP sink is a computer monitor supporting DP input.

1.2.3. LEDs Description

The LEDs on the evaluation board and the Modular FMC adapter are used to indicate status of the demonstration system. All used LEDs must be glowing steadily (without blinking) to indicate proper running state of the demo. Please refer to the

LED Troubleshooting Guide section to interpret the status of the demonstration system based on LEDs.
The eight green LEDs on the evaluation board are used as described in Table 1.1 and the four green LEDs used on the Modular FMC adapter are used as described in Table 1.2.

Table 1.1. Eval Board LEDs Description

LED	Description
D6	SERDES reference clock PLL locked
D7	System (RISC-V) clock PLL locked
D8	Not used
D9	Pixel Clock PLL locked
D10	RX video stream valid
D11	Clock recovery running status
D12	Video Scaler IP ready
D13	Video Scaler IP frame valid

Table 1.2. Modular FMC adapter LEDs Description

LED	Description
LED0	Not used
LED1	Not used
LED2	Tx training done
LED3	Not used

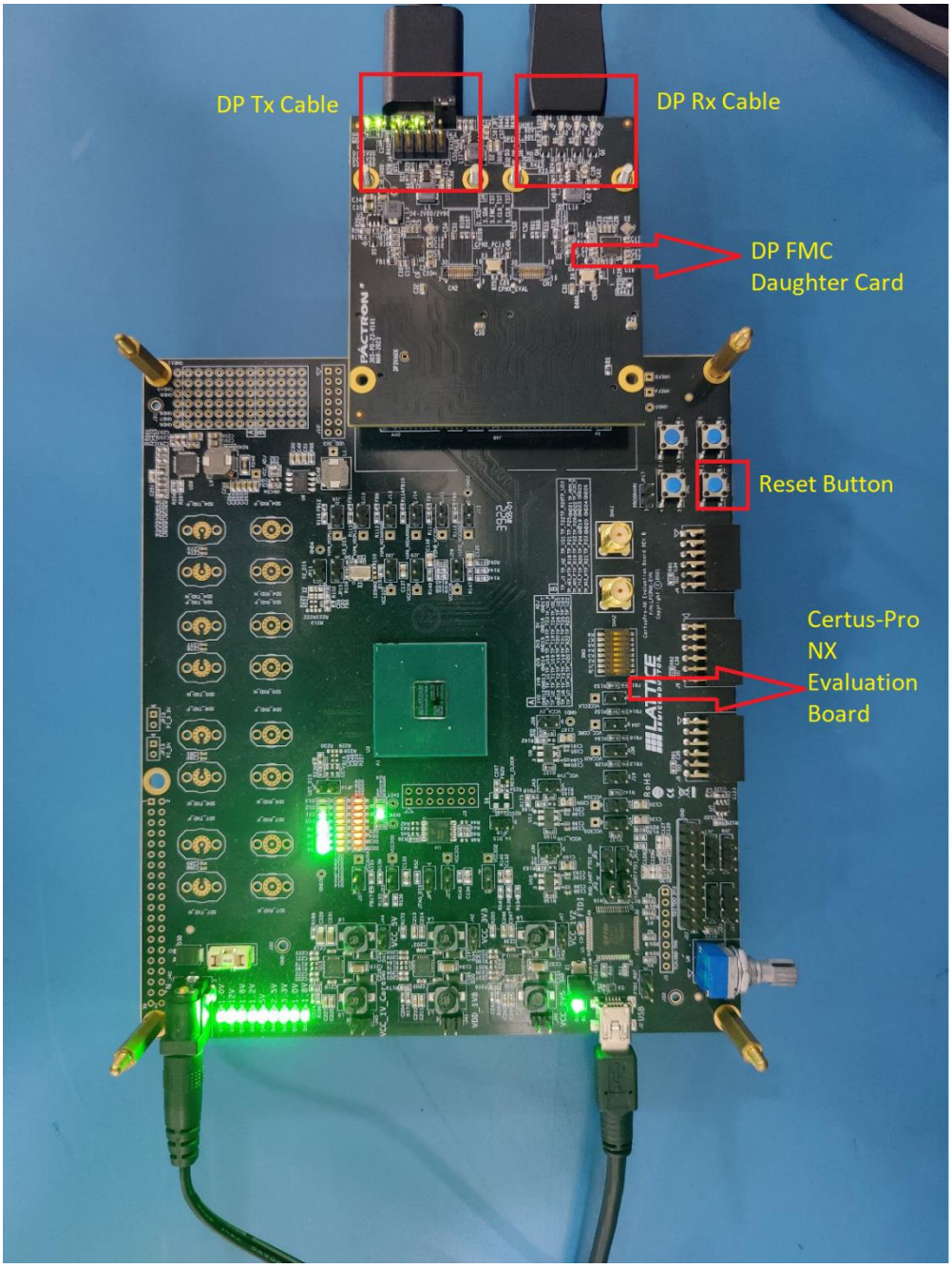

Figure 1.2. Demonstration Hardware Setup

2. SoC Design Details

An SoC design created using Lattice Propel™ Builder is provided for this demo. Users can take this working system and modify the design or the parameters of the building block IPs as necessary.

2.1. Top-level design

The top-level SoC design is shown in Figure 2.1.

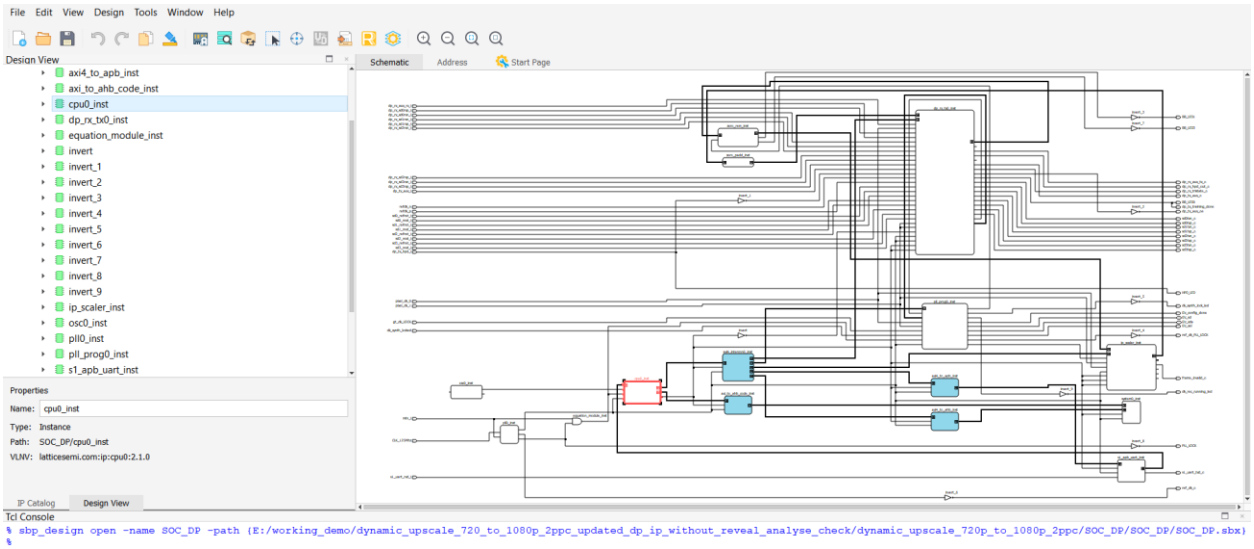

Figure 2.1. Soc Design

2.2. Top-level ports

Table 2.1 shows the ports used in the SoC Design in the Lattice Propel Builder.

Table 2.1. SoC Design Ports Description

Port Name	Direction	Width	Description
refclk_p	In	1	P port of 135 MHz differential reference clock. Note: This should be 108 MHz for 1.62Gbps Data Rate
refclk_n	In	1	N port of 135 MHz differential reference clock. Note: This should be 108 MHz for 1.62Gbps Data Rate
pixel_clk_0	In	1	Pixel clock input. The frequency depends on the video resolution.
pixel_clk_1	In	1	Pixel clock input. The frequency depends on the resolution.
rstn_i	In	1	Active low asynchronous reset of minimum 100 us duration.
dp_tx_aux_o	Out	1	Output signal for AUX channel.
dp_tx_aux_oe_o	Out	1	Tri-state control for AUX channel. If the value is '1', the AUX output is driven, otherwise it is undriven and held at high impedance state.
dp_tx_aux_i	In	1	Input signal from AUX channel
dp_tx_hpd_i	In	1	Hot plug detect signal to inform DP source that DP sink is connected.
dp_tx_training_done	Out	1	Training done output signal to inform that training has been done at at DP Tx side.
dp_rx_sd0rxp_i	In	1	This is lane0 serial data_p signal of DP Rx main channel.
dp_rx_sd0rxn_i	In	1	This is lane0 serial data_n signal of DP Rx main channel.

Port Name	Direction	Width	Description
dp_rx_sd1rxp_i	In	1	This is lane1 serial data_p signal of DP Rx main channel.
dp_rx_sd1rxn_i	In	1	This is lane1 serial data_n signal of DP Rx main channel.
dp_rx_sd2rxp_i	In	1	This is lane2 serial data_p signal of DP Rx main channel.
dp_rx_sd2rxn_i	In	1	This is lane2 serial data_n signal of DP Rx main channel.
dp_rx_sd3rxp_i	In	1	This is lane3 serial data_p signal of DP Rx main channel.
dp_rx_sd3rxn_i	In	1	This is lane3 serial data_n signal of DP Rx main channel.
sd0txp_o	Out	1	This is lane0 serial data_p signal of DP Tx main channel.
sd0txn_o	Out	1	This is lane0 serial data_n signal of DP Tx main channel.
sd1txp_o	Out	1	This is lane1 serial data_p signal of DP Tx main channel.
sd1txn_o	Out	1	This is lane1 serial data_n signal of DP Tx main channel.
sd2txp_o	Out	1	This is lane2 serial data_p signal of DP Tx main channel.
sd2txn_o	Out	1	This is lane2 serial data_n signal of DP Tx main channel.
sd3txp_o	Out	1	This is lane3 serial data_p signal of DP Tx main channel.
sd3txn_o	Out	1	This is lane3 serial data_n signal of DP Tx main channel.
dp_rx_hpd_out_o	Out	1	Hot plug signal to inform DP source that DP sink is connected. (part of dp cable)
dp_rx_aux_oe_o	Out	1	Tri-state control for AUX channel output. If the value is '1', the AUX output is driven, otherwise it is undriven and held at high impedance state.
dp_rx_aux_i	In	1	AUX channel input.
dp_rx_aux_o	Out	1	AUX channel output.
sd0_refret_i	In	1	Analog reference return for PMA PLL for Lane 0
sd0_rext_i	In	1	External resistance for Lane 0
sd1_refret_i	In	1	Analog reference return for PMA PLL for Lane 1
sd1_rext_i	In	1	External resistance for Lane 1
sd2_refret_i	In	1	Analog reference return for PMA PLL for Lane 2
sd2_rext_i	In	1	External resistance for Lane 2
sd3_refret_i	In	1	Analog reference return for PMA PLL for Lane 3
sd3_rext_i	In	1	External resistance for Lane 3
clk_synth_locked	In	1	Video Clock PLL lock
gt_clk_LOCK	In	1	Reference Clock PLL lock
s1_uart_rxd_i	In	1	UART Rx pin to receive data
training_done_LED	Out	1	This is to connect to an LED to indicate dp_tx_training_done
ip_scaler_ready_LED	Out	1	Video_scaler ready LED
dp_tx_valid_LED	Out	1	DP Tx valid LED
HPD_LED	Out	1	Hot plug detect LED
clk_synth_lock_led	Out	1	Video Clock PLL lock LED
i2c_config_done	Out	1	I2C configuration done
i2c_scl	Out	1	I2C serial clock
i2c_sda	Out	1	I2C serial data
i2c_sel	Out	1	I2C select
ref_clk_PLL_LOCK	Out	1	Reference Clock PLL lock LED
frame_invalid_o	Out	1	Video Scaler frame invalid LED to inform regarding frame invalidity.
clk_rec_running_led	Out	1	Clock running status LED
PLL_LOCK	Out	1	PLL locked LED
s1_uart_txd_o	Out	1	UART Tx pin to transmit data

2.3. IP Description

The SoC design is created by connecting multiple Lattice IPs including DisplayPort, Video Scaler, PLL, RISC-V, AXI4 Interconnect, AXI4 to AHB-Lite Bridge, Oscillator, AXI4 to APB Bridge and UART. In addition to the standard Lattice IPs, two custom modules namely, Clock Controller and DP to VS Converter, are also used in this design. The custom modules are distributed as IP package files (.ipk files) in the demonstration package. The following subsections describe each of the IPs or custom designs used in the SoC design. The parameters of the IPs that are used in the provided SoC design are shown under Default column in the Attributes description tables of the IPs. User changeable parameters or other comments related to customization are given under Options column in those tables.

2.3.1. DisplayPort

DisplayPort IP helps users implement DisplayPort video interface as defined by VESA DisplayPort specifications. This IP supports standard interfaces for configuration and video data, namely AXI-Lite and AXI-Stream. These standard interfaces allow the user to easily connect with other Lattice IPs using Propel Builder.

Table 2.2. DP Attributes Description

Attribute	Selectable Values	Default	Options
General			
Enable SIM Mode	Enabled, Disabled	Disabled	-
Mode	Tx only Rx only Tx and Rx	Tx and Rx	-
External Reference Clock (MPCS)	0, 1	1	-
Lane ID for MPCS	0, 4	0	-
AXI-Lite Interface Data Width	-	32	-
AXI-Lite Interface Address Width	-	32	-
AXI-Lite DPTX Base Address	32	0x10080000	AXI-Lite DP TX Base Address
AXI-Lite DPRX Base Address	32	0x100B0000	AXI-Lite DP RX Base Address
DP TX Settings			
General			
Implementation of FIFO	EBR, LUTs	EBR	-
Resolution Lock Frame Count	0 - 20	3	-
User Data Interface			
Video Interface	AXI-STREAM, Native Video	AXI-STREAM	-
Pixels Per Clock	1, 2, 4	2	User selectable
IP Capability			
eDP Enable	Enabled, Disabled	Disabled	-
eDP Fast Link Training	Enabled, Disabled	Disabled	-
eDP ASSR Enable	Enabled, Disabled	Disabled	-
eDP Reduced AUX Timing	Enabled, Disabled	Disabled	-
Enable Interlaced video	Enabled, Disabled	Disabled	-
Enable MST	Enabled, Disabled	Disabled	-
MST Stream Count	1, 2, 3, 4	1	
Enable Audio	Enabled, Disabled	Disabled	-
Audio Channel Count	2/8	Disabled	-
Maximum Lane Count	1, 2, 4	4	-
Maximum Link Rate (Gbps)	1.62, 2.7, 5.4, 8.1	5.4	-
Color Format			
Enable RGB Format	Enabled, Disabled	Enabled	-
Enable YCbCr444 Format	Enabled, Disabled	Disabled	-

Attribute	Selectable Values	Default	Options
Enable YCbCr422 Format	Enabled, Disabled	Disabled	-
Enable RAW Format	Enabled, Disabled	Disabled	-
Bits per Component/Bits per Pixel			
Enable 6 BPC	Enabled, Disabled	Disabled	-
Enable 7 BPC	Enabled, Disabled	Disabled	-
Enable 8 BPC	Enabled, Disabled	Enabled	-
Enable 10 BPC	Enabled, Disabled	Disabled	-
Enable 12 BPC	Enabled, Disabled	Disabled	-
Enable 14 BPC	Enabled, Disabled	Disabled	-
Enable 16 BPC	Enabled, Disabled	Disabled	-
DP RX Settings			
General			
DP Rx Activate	Enabled, Disabled	Disabled	-
Implementation of FIFO	EBR, LUT	EBR	-
Resolution Lock Frame Count [0-20]	0-20	3	-
Pixel Clock Rate Compensation	Enabled, Disabled	Enabled	-
User Data Interface			
Video Interface	AXI-STREAM, Native Video	AXI-STREAM	-
Pixels Per Clock	1, 2, 4	2	User selectable
IP Capability			
eDP Enable	Enabled, Disabled	Disabled	-
eDP Fast Link Training	Enabled, Disabled	Disabled	-
eDP ASSR Enable	Enabled, Disabled	Disabled	-
eDP Reduced AUX Timing	Enabled, Disabled	Disabled	-
Enable Interlace	Enabled, Disabled	Disabled	-
Enable MST	Enabled, Disabled	Disabled	-
MST Stream Count	1-4	1	-
Enable Enhanced Frame	Enabled, Disabled	Enabled	-
Enable Audio	Enabled, Disabled	Disabled	-
Maximum Lane Count	1, 2, 4	4	-
Maximum Link Rate(Gbps)	1.62, 2.7, 5.4, 8.1	5.4	-
Color Format			
Enable RGB Format	Enabled, Disabled	Enabled	-
Enable YCbCr444 Format	Enabled, Disabled	Disabled	-
Enable YCbCr 422 Format	Enabled, Disabled	Disabled	-
Enable RAW Format	Enabled, Disabled	Disabled	-
Bits per Component/Bits per Pixel			
Enable 6 BPC	Enabled, Disabled	Disabled	-
Enable 7 BPC	Enabled, Disabled	Disabled	-
Enable 8 BPC	Enabled, Disabled	Enabled	-
Enable 10 BPC	Enabled, Disabled	Disabled	-
Enable 12 BPC	Enabled, Disabled	Disabled	-
Enable 14 BPC	Enabled, Disabled	Disabled	-
Enable 16 BPC	Enabled, Disabled	Disabled	-
TX Video Settings			
General			
Default Resolution	1920x1080p, RGB, 8BPC,	1280x720p, RGB, 8BPC	-

Attribute	Selectable Values	Default	Options
	1280x720p , RGB, 8BPC, 3840x2160p, RGB, 8BPC.		
DP TX Activate	Enabled, Disabled	Enabled	-
Set MSA based on Default Resolution	Enabled, Disabled	Disabled	-
Pixel clock frequency (in MHz)	-	74.25	-
Main Stream Attribute			
Pixel Format and BPC	-	RGB, 8BPC	-
Total Horizontal Size	-	1650	-
Total Vertical Size	-	750	-
Horizontal Width	-	1280	-
Vertical Height	-	720	-
Horizontal Active Start Point	-	330	-
Vertical Active Start Point	-	25	-
Horizontal Sync Width	-	40	-
Vertical Sync Width	-	5	-

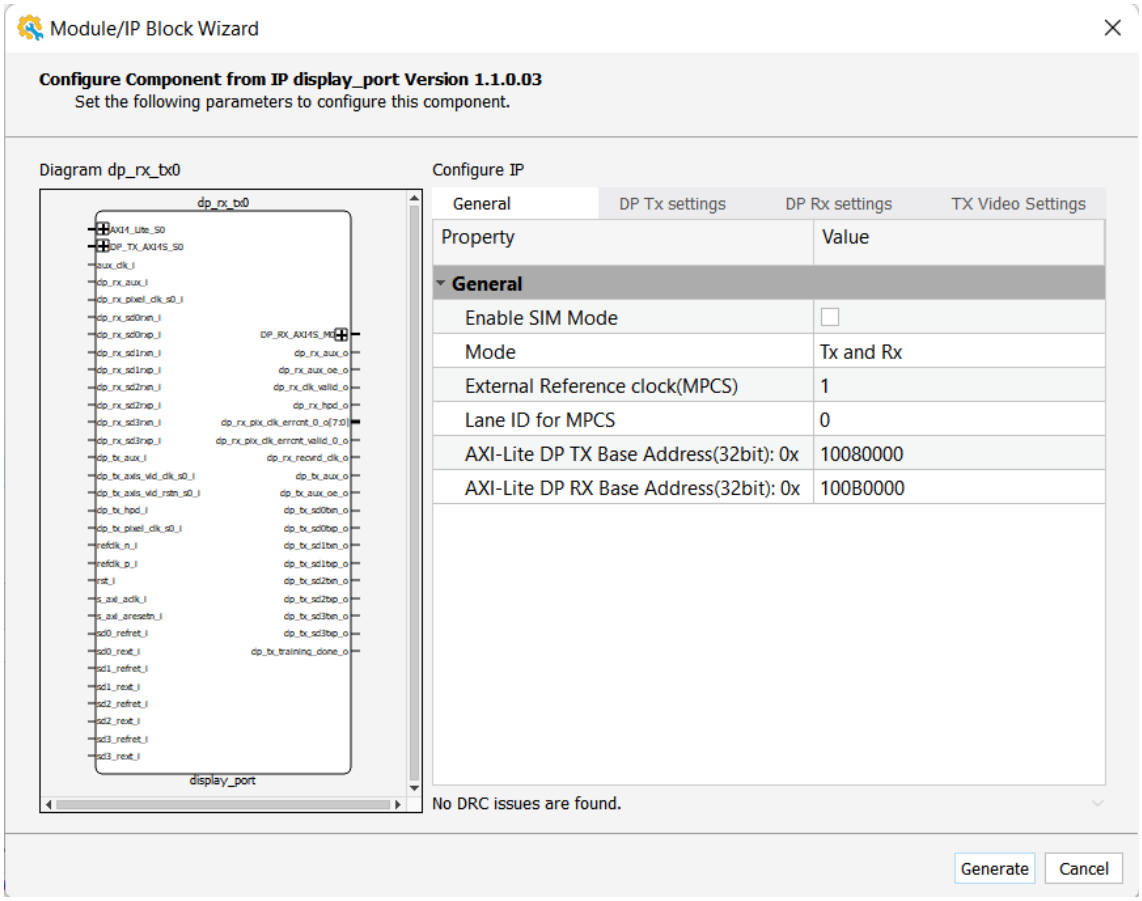

Figure 2.2. GUI for DisplayPort IP

For more information, refer to the DisplayPort IP Core - User Guide (FPGA-IPUG-02236).

2.3.2. Video Scaler

The Video Scaler IP Core is used to scale up or scale down the resolution of a video stream. The IP supports scaling from an arbitrary input resolution to a wide range of output resolutions as configured by the user. This demonstration supports dynamic scaling.

Table 2.3. Video Scaler Attributes Description

Attribute	Selectable Values	Default	Options
Architecture			
General			
Streaming Interface	AXI4, Native	AXI4	-
Video format	YCbCr4:2:2, YCbCr4:4:4, RGB	RGB	-
Pixels Per Clock	1, 2, and 4	2	User Selectable
Bits Per Color	8, 10, 12, and 16	8	-
Enable dynamic reconfiguration	Enabled, disabled	Enabled	-
Frame Dimensions			
Input active pixels	4096	2560	User Selectable
Input active lines	32-4096	1440	User Selectable
Output active pixels	32-4096	2560	User Selectable
Output active lines	32-4096	1440	User Selectable
Output Hblank Pixels	0-4096	740	User Selectable
Output Vblank Lines	0-4096	60	User Selectable
Algorithm			
Scaling method	Nearest, Bilinear, Bicubic, and Lanczos	Bicubic	User Selectable
Number of vertical filter taps	-	4	-
Number of horizontal filter taps	-	4	-
Number of vertical filter phrases	16, 32, 64, 128, 256	16	-
Number of horizontal filter phrases	16, 32, 64, 128, 256	16	-
Coefficient width	6, 7, 8, 9, 10, 11, 12, 13, 14, 15	9	-
AXI4 Lite Configuration			
AXI4-Lite Base Address	32	0x1000B000	AXI4-Lite Base Address
Implementation			
Memory type			
Line Buffer type	EBR/Distributed	EBR	-
Vertical coefficient memory type	EBR/Distributed	Distributed	-
Horizontal coefficient memory type	EBR/Distributed	Distributed	-
Multiplier type			
Multiplier type	DSP/LUT	DSP	-
FIFO Configuration			
Automatic FIFO Depth	Enabled, Disabled	Enabled	-
Input FIFO Depth	8-8192	1280	-
Output FIFO Depth	32-8192	1280	-

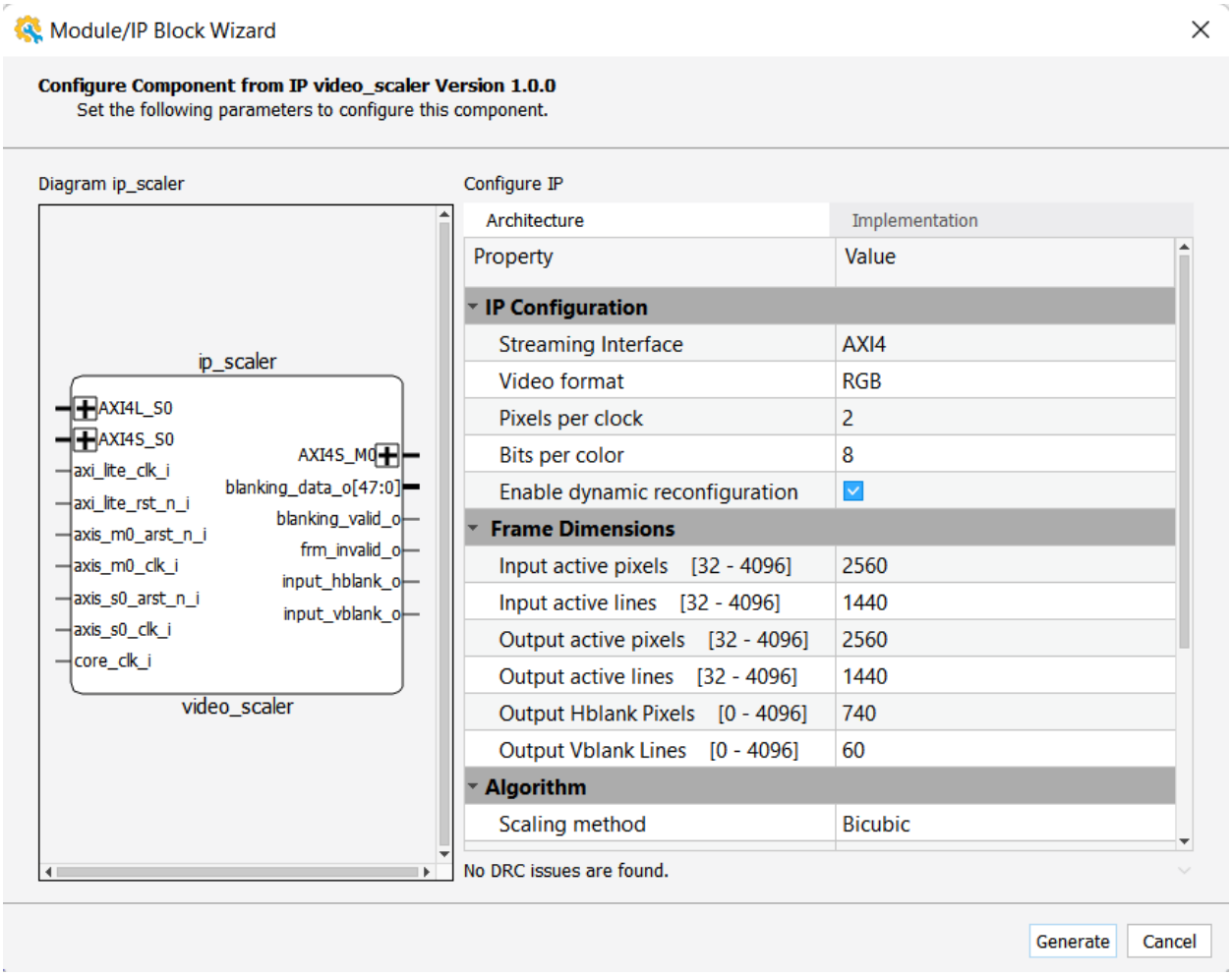

Figure 2.3. GUI for Video Scaler IP

For more information, refer to the Video Scaler IP-User Guide (FPGA-IPUG-02234) user guide.

2.3.3. DP to VS Converter

This custom IP facilitates the pixel clock recovery algorithm and creates outputs for debug LEDs. The parameters under **Default** column shown in Table 2.4 are set for this demonstration.

Table 2.4. DP to VS Converter Attribute Description

Attribute	Selectable Values	Default	Options
General			
Pixel Per Clock	1, 2, 4	2	User Selectable

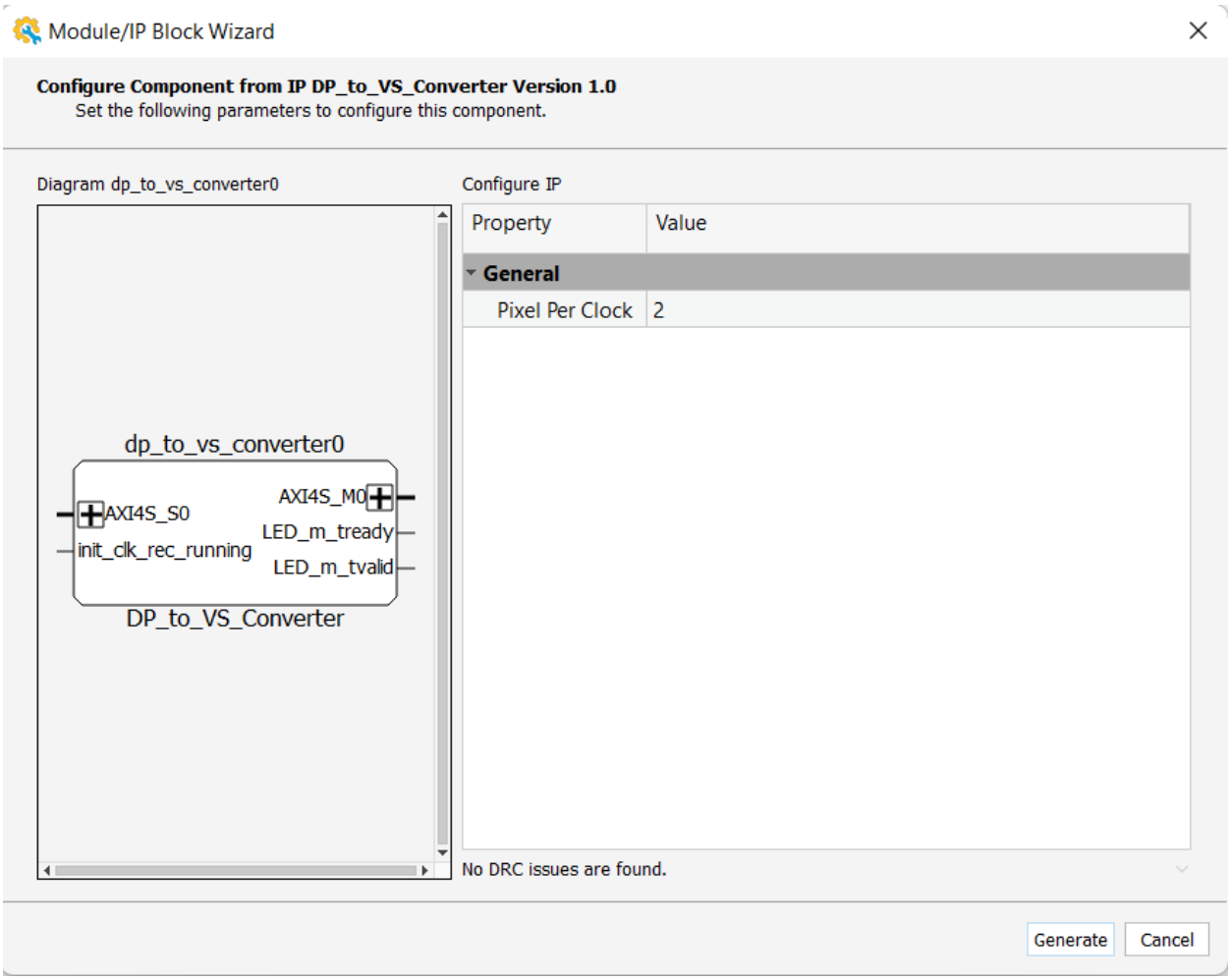

Figure 2.4. GUI for DP to VS Converter IP

2.3.4. Clock Controller

This custom IP consists of an I2C module, a Clock recovery module for External Clock generation and a ppm error correction module. This IP also has DCS for dynamically selecting core_clk_i for the video scaler IP. There are two external clocks, namely “Pixel Clk 0” and “Pixel Clk 1” required for Video Scaler IP. These clocks are configured by the I2C module based on the values of Input and Output Resolutions selected.

The following configuration is used for this Demonstration:

Table 2.5. Clock Controller Attribute Description

Attribute	Selectable Values	Default	Options
General			
Base Address	32 bits	0x10000000	Base Address

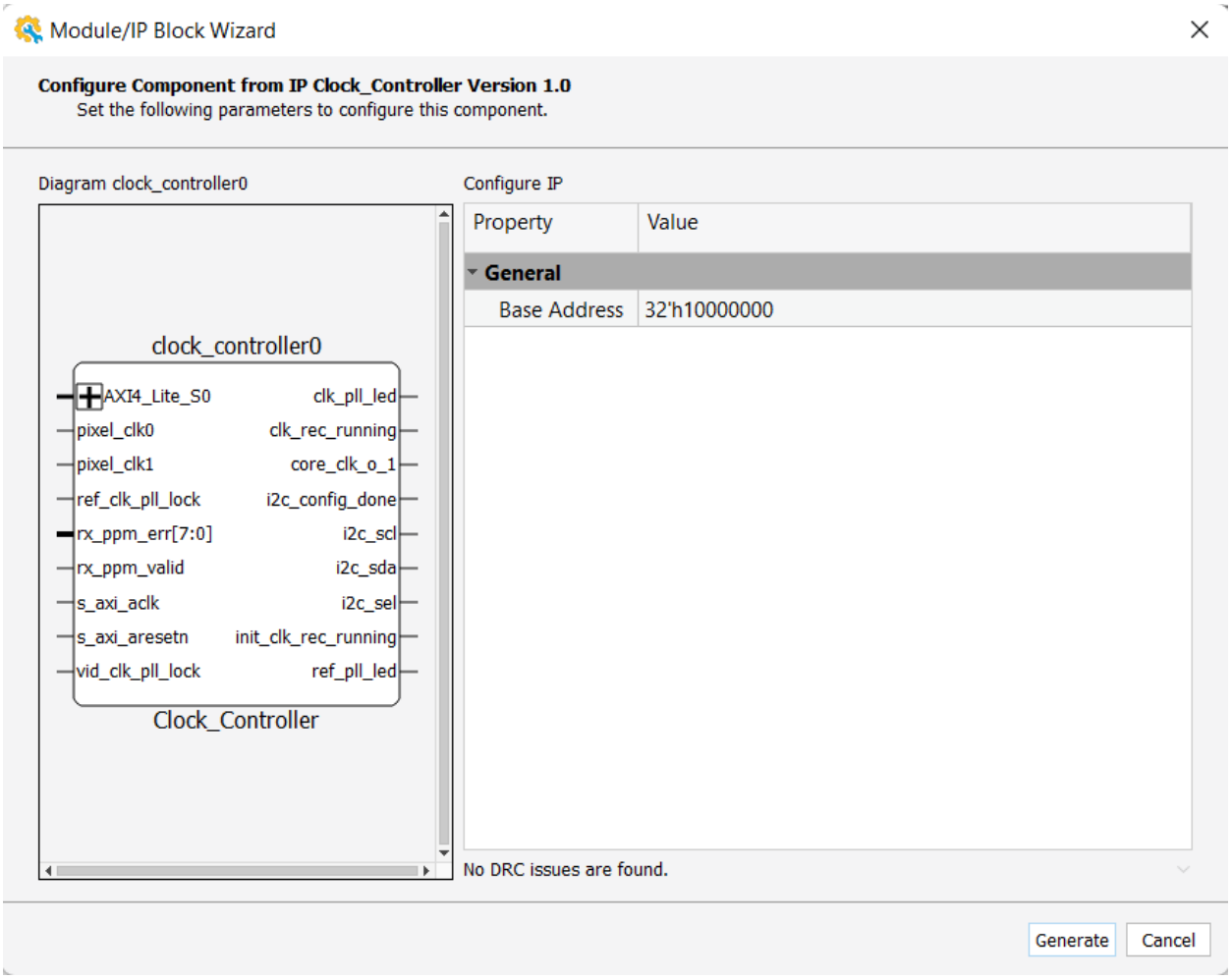

Figure 2.5. GUI for Clock Controller IP

2.3.5. Oscillator

This IP is a part of the RISC-V RX FreeRTOS Project template. The Low Frequency Clock (LFCLK) of 32kHz is connected to the real time clock (low-speed real-time clock input) of RISC-V RX RTOS.

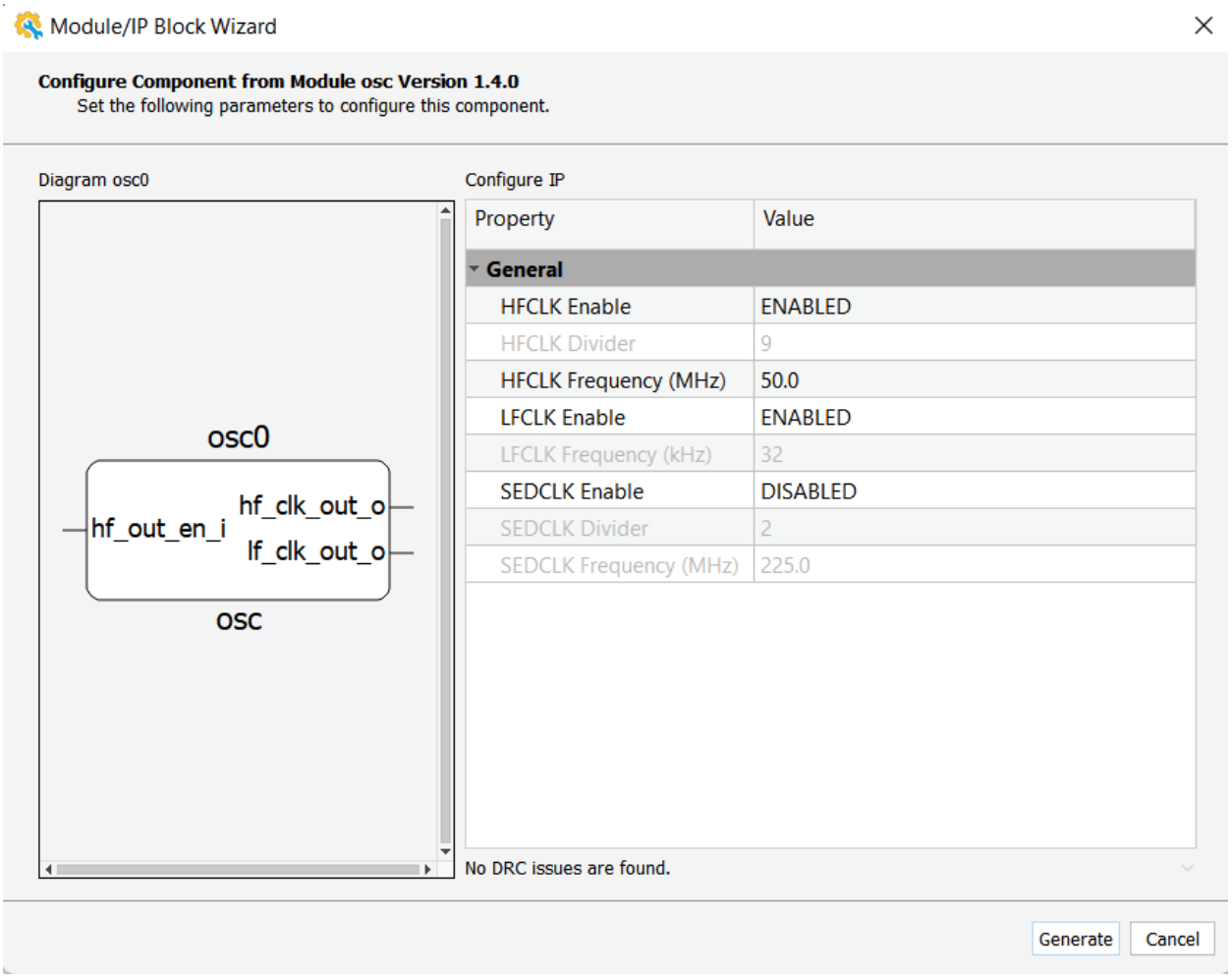

Figure 2.6. GUI for Oscillator IP

2.3.6. PLL

This IP is a part of the RISC-V RX FreeRTOS Project template. In this IP, the reference clock frequency is set to 50 MHz for the generation of primary clock frequency of 100 MHz. The GUI for this IP is shown in Figure 2.7.

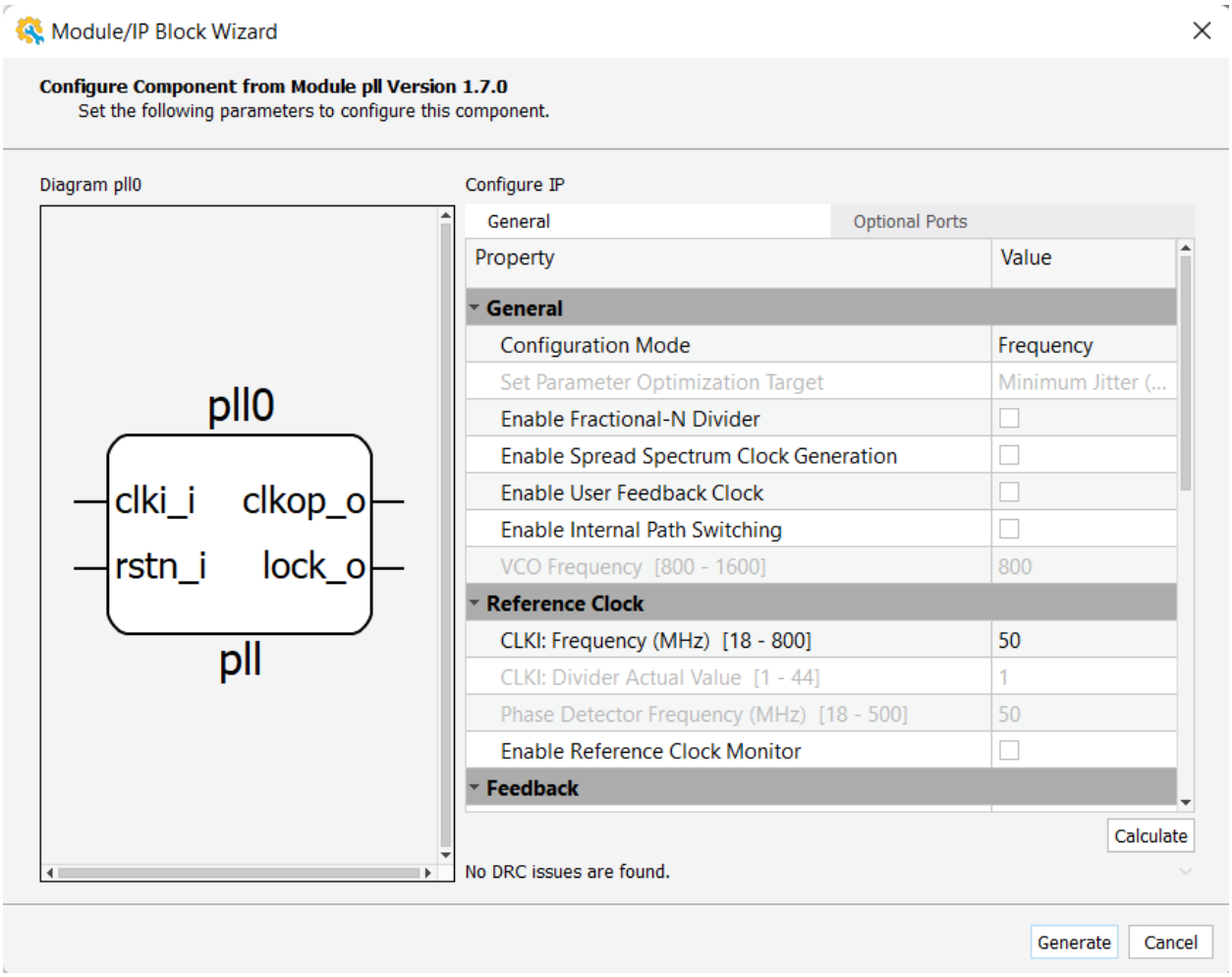

Figure 2.7. GUI for PLL IP

2.3.7. AXI Interconnect

This is part of RISC-V RX FreeRTOS template. This IP has one External AXI Manager and five External AXI Subordinates, labelled 0 to 5. Ports 0 and 1 are AXI Managers connected to Subordinate ports of AXI to AHB Bridge and AXI to APB Bridge respectively. Ports 2, 3, and 4 are AXI-Lite Managers connected to subordinate ports of Clock Controller, DP and Video Scaler IPs respectively. The GUI for this IP is shown in Figure 2.8.

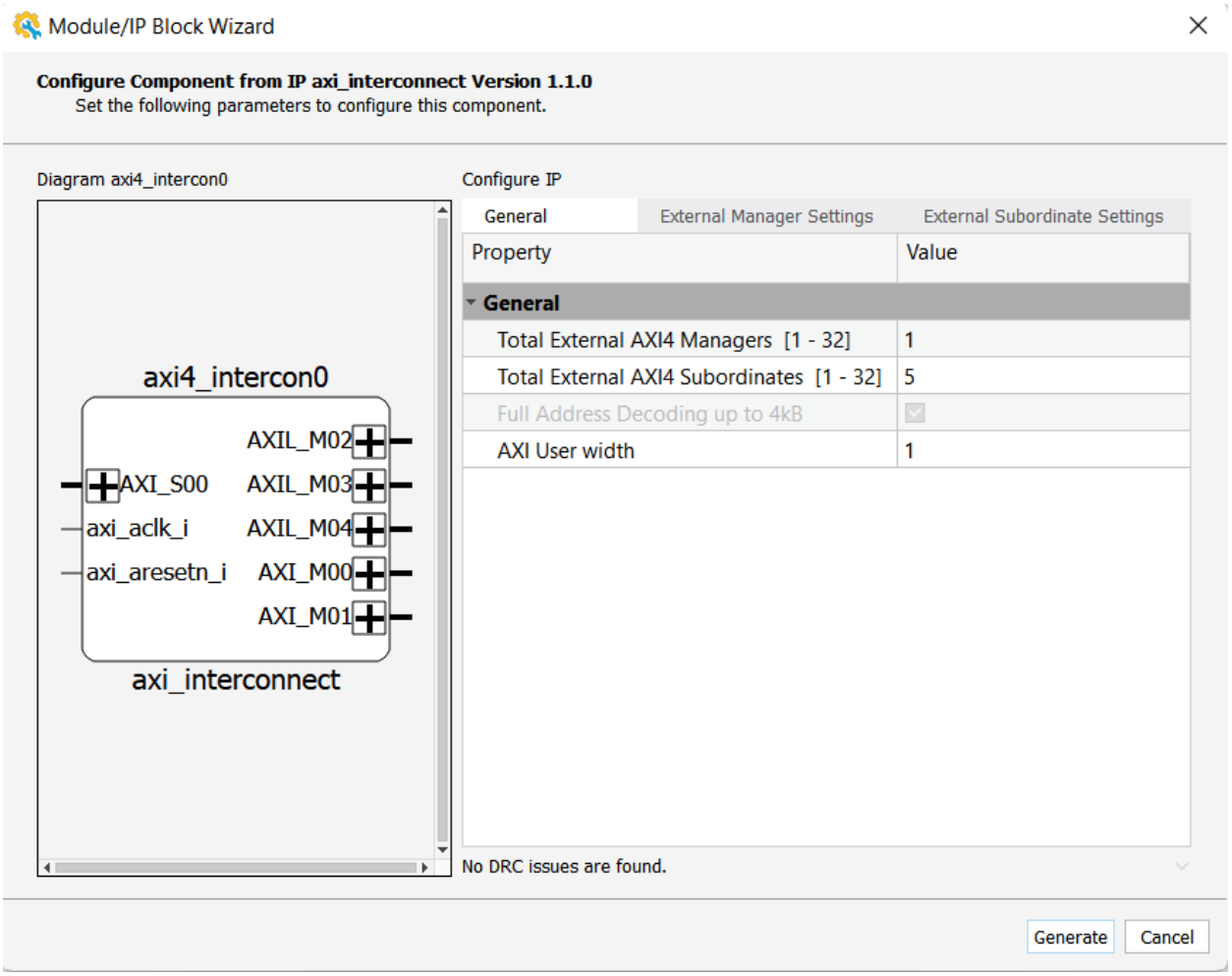

Figure 2.8. GUI for AXI Interconnect IP

2.3.8. AXI to AHB-Lite Bridge

This IP comes with the RISC-V RX FreeRTOS template for AXI to AHB conversion. There are two IPs of this type in this demonstration design. One IP acts as a bridge between RISC-V RTOS and System memory, and the other between AXI Interconnect and System memory, for bridging AXI interface to AHB interface. The GUI for this IP is shown in Figure 2.9.

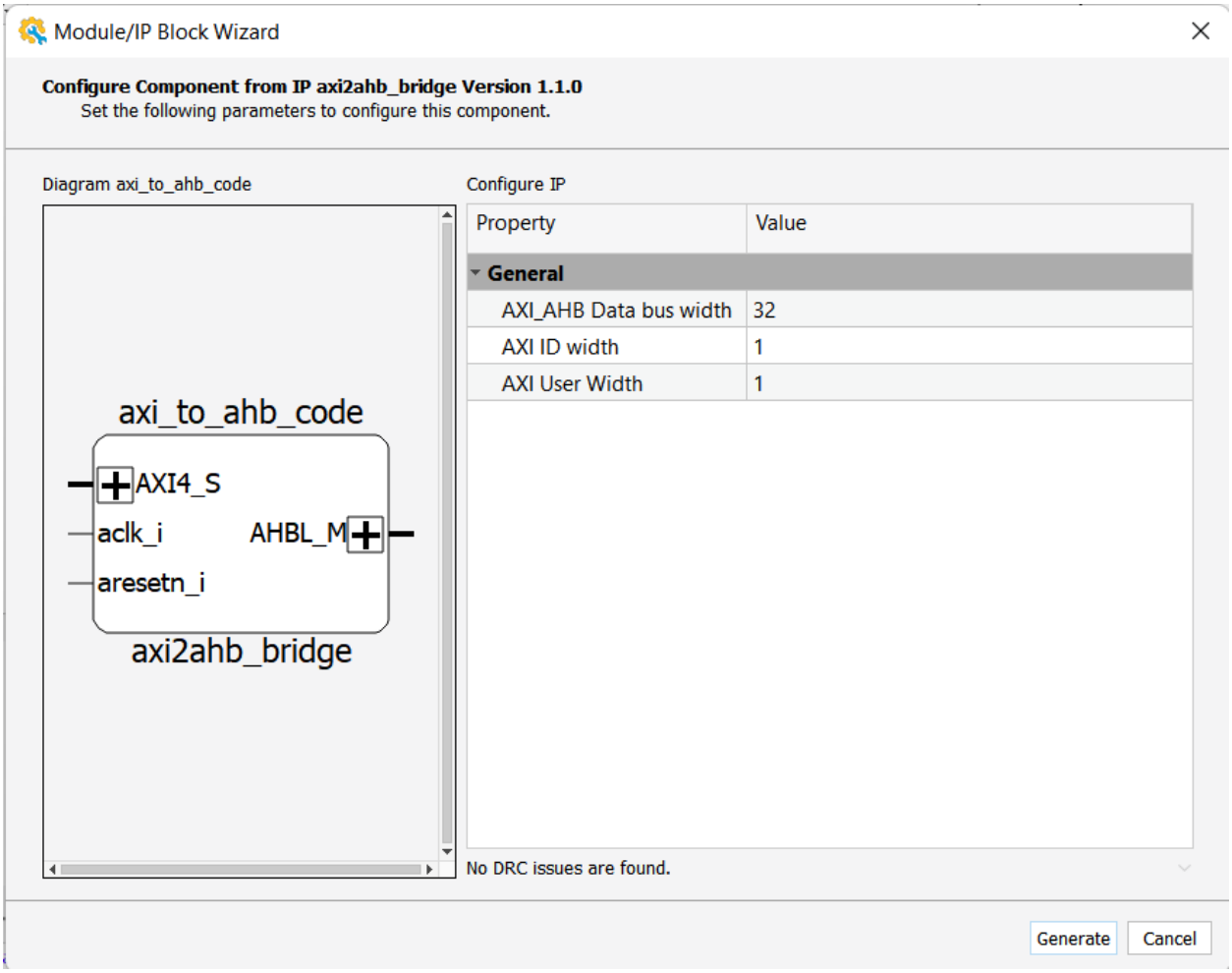

Figure 2.9. GUI for AXI to AHB-Lite Bridge IP

2.3.9. AXI to APB Bridge

This IP comes with the RISC-V RX FreeRTOS template for AXI to APB conversion. It acts as a bridge between AXI Interconnect and UART. The GUI for this IP is shown in Figure 2.10.

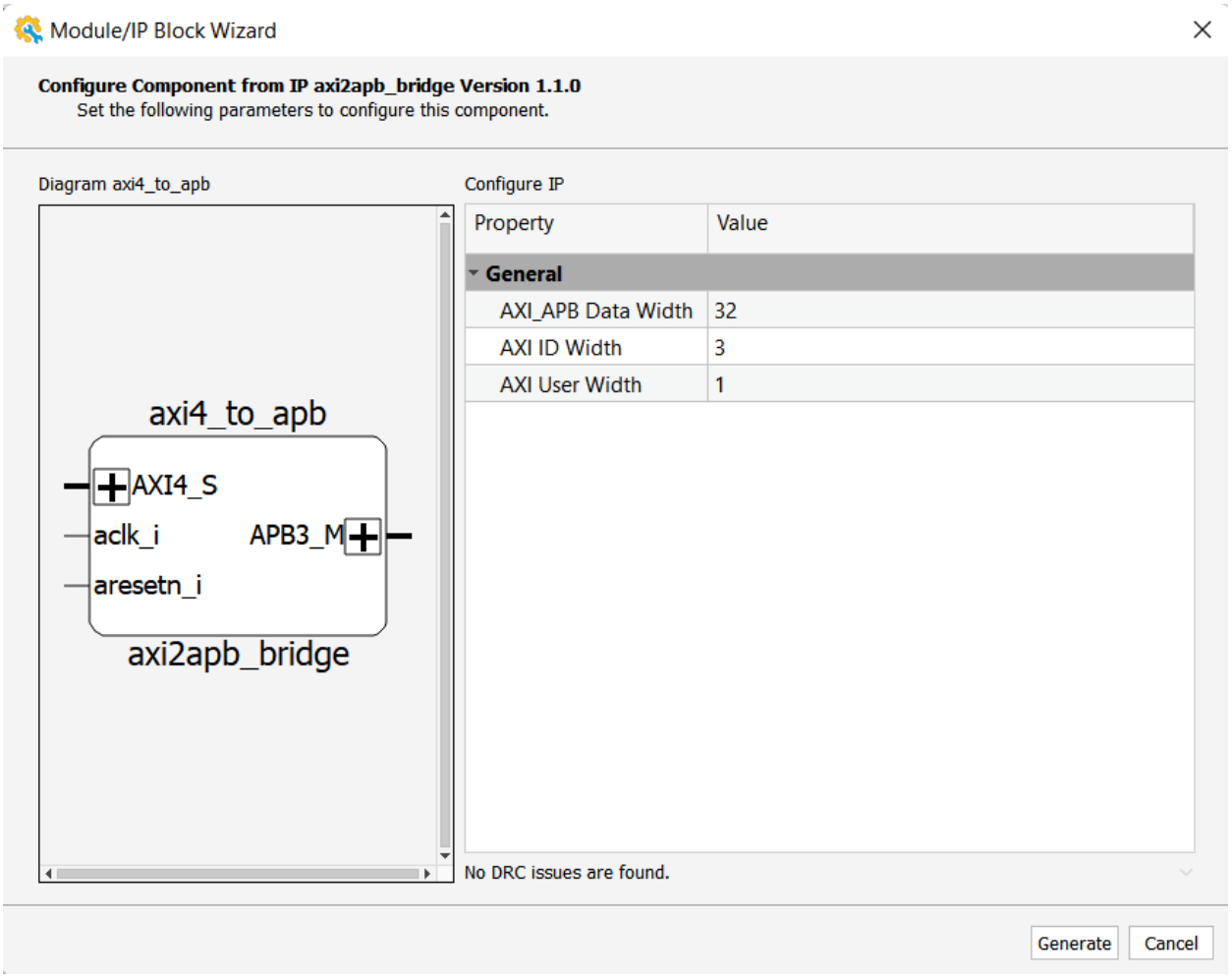

Figure 2.10. GUI for AXI to APB Bridge IP

2.3.10. System memory

This IP comes with the RISC-V RX FreeRTOS template. The user must specify the correct RISC-V memory initialization file (.mem file) in the IP GUI. The default memory type is set as **LRAM** and address depth as **102400**. Note that once the project is opened in your environment, this IP needs to be re-generated with the correct path of the .mem file. The GUI for this IP is shown in Figure 2.11.

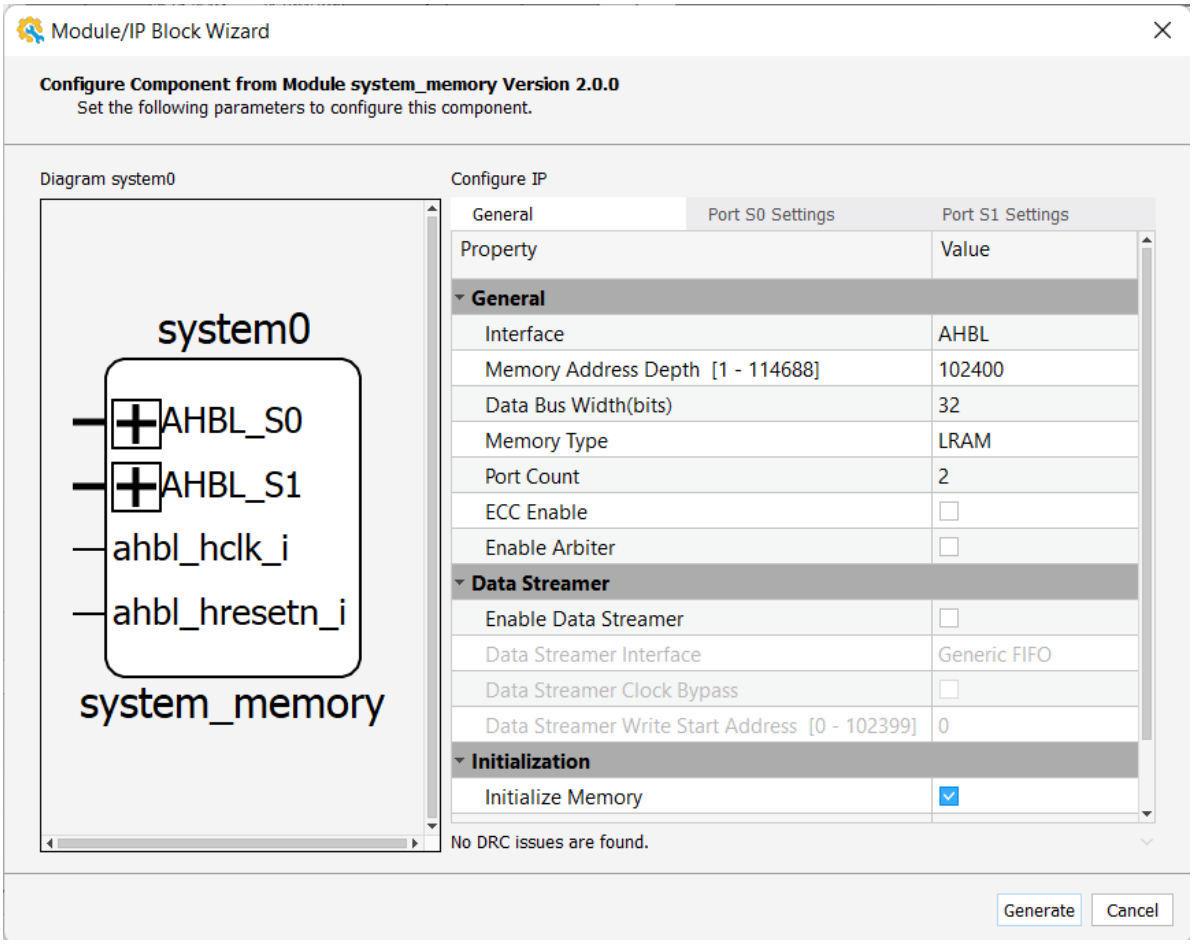

Figure 2.11. GUI for System Memory IP

2.3.11. RISC-V RX

This IP is the main RISC-V RX IP core. The RISC-V RX IP processes data and instructions while monitoring the external interrupts. The CPU IP has 32-bit processor core and submodules. Among the submodules, PLIC and CLINT/Watchdog are required, while Local UART is optional. The 32-bit processor uses the AXI Instruction Port to fetch the instructions and AXI Data Port to access data. Here the optional port, Tightly Coupled Memory (TCM), is disabled. The GUI for this IP is shown in Figure 2.12.

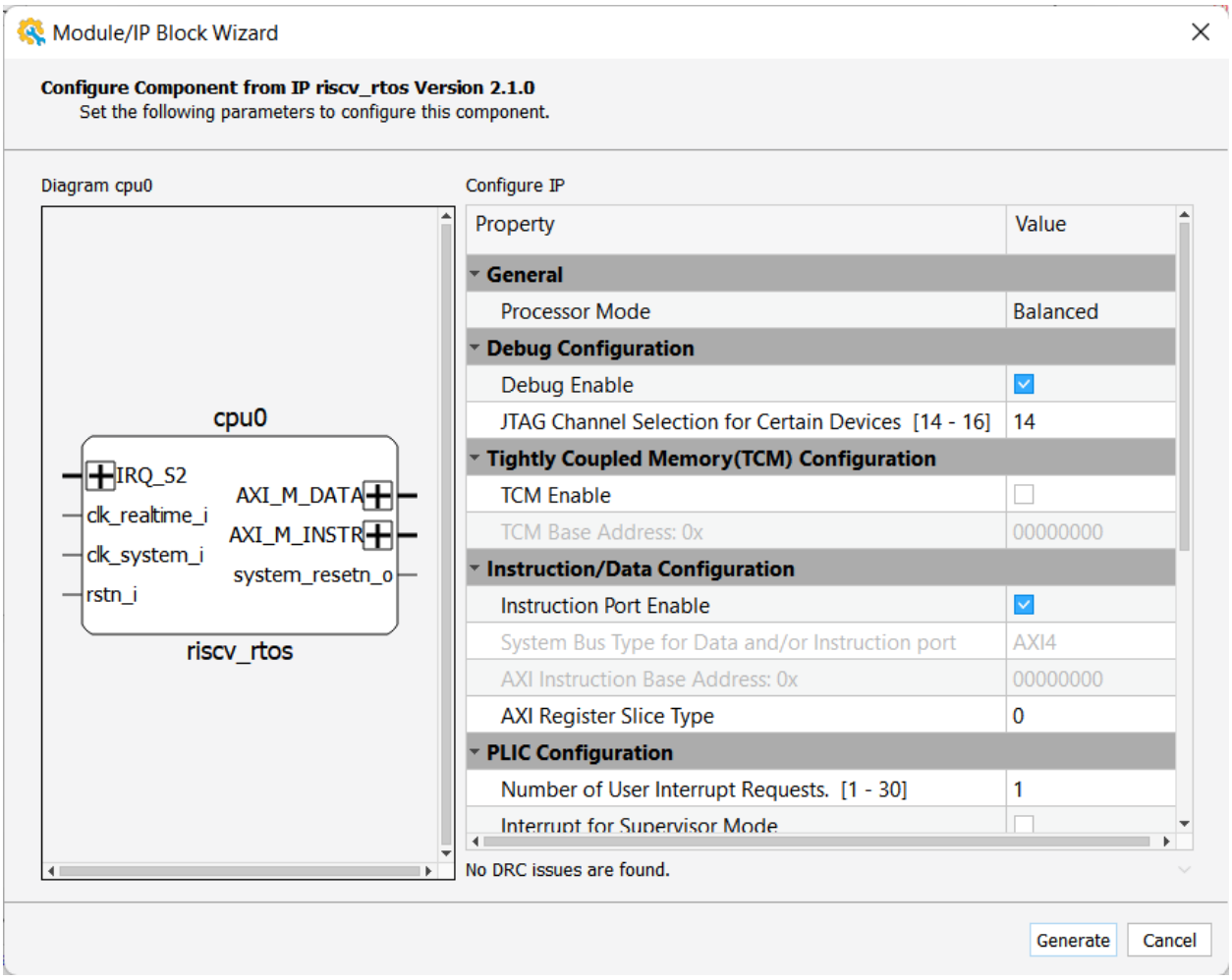

Figure 2.12. GUI for RISC-V RX IP

For more information, refer to RISC-V RX CPU IP - Lattice Propel Builder (FPGA-IPUG-02230).

2.3.12. UART

This IP is a part of RISC-V RX FreeRTOS template. The UART is used for serial communication and the Baud Rate is selected as **115200**. It supports APB interface and a common interrupt line for all internal UART data and error events. The GUI for this IP is shown in Figure 2.13.

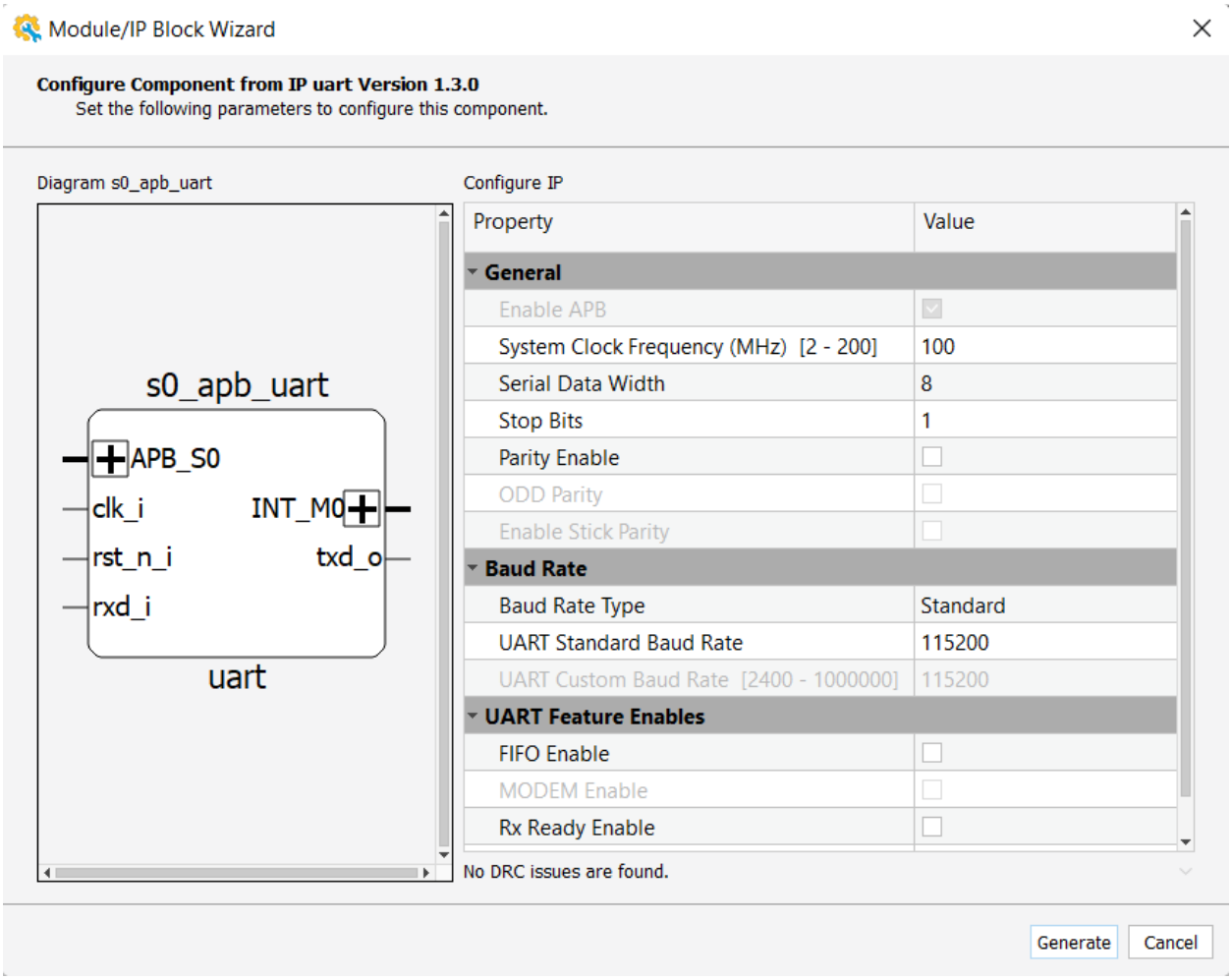

Figure 2.13. GUI for UART IP

For more information, refer to UART IP Core - Lattice Propel Builder (FPGA-IPUG-02105).

3. Modifying and Implementing the SoC Design

3.1. Opening the Sbx project

1. Click **FILE > Open Design** from the Lattice Propel Builder GUI Menu, or Click **Open Design icon** from Propel Builder toolbar. The **Open Sbx Dialog** opens.

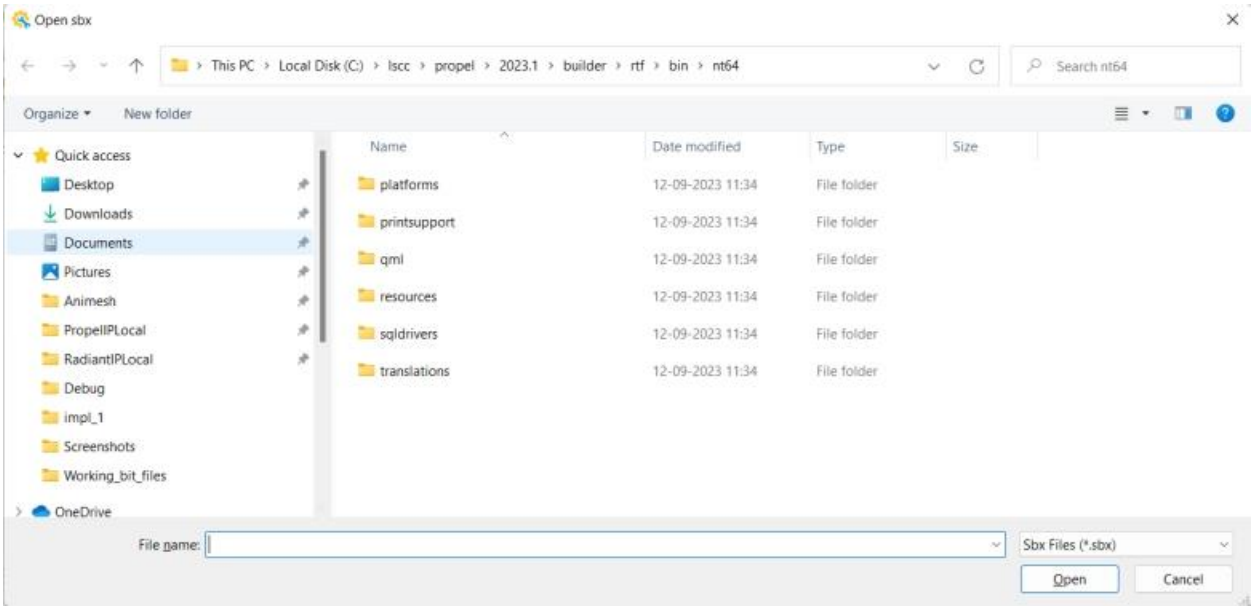

Figure 3.1. Sbx Dialog Box

2. Browse to find the project workspace folder. Choose the **SOC_DP.sbx** file.

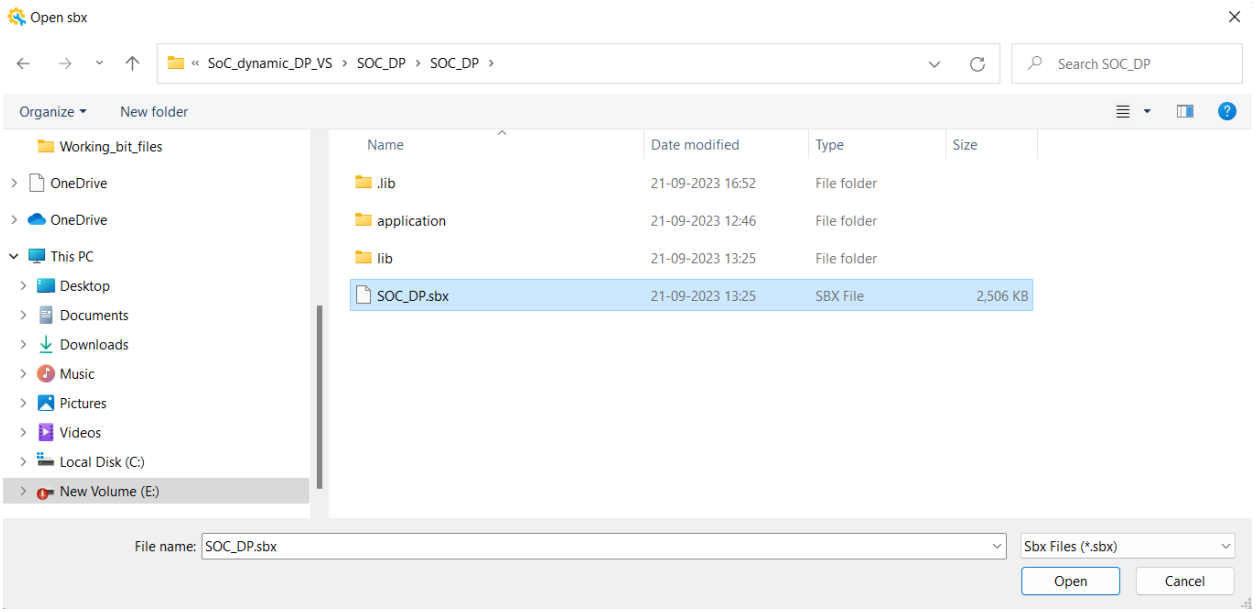

Figure 3.2. Project Sbx file Dialog Box

3. Click **IP Catalog**. If the four IPs used in this design are already installed in the local machine, skip to step 7. If one or more IPs are not installed, continue to step 4.

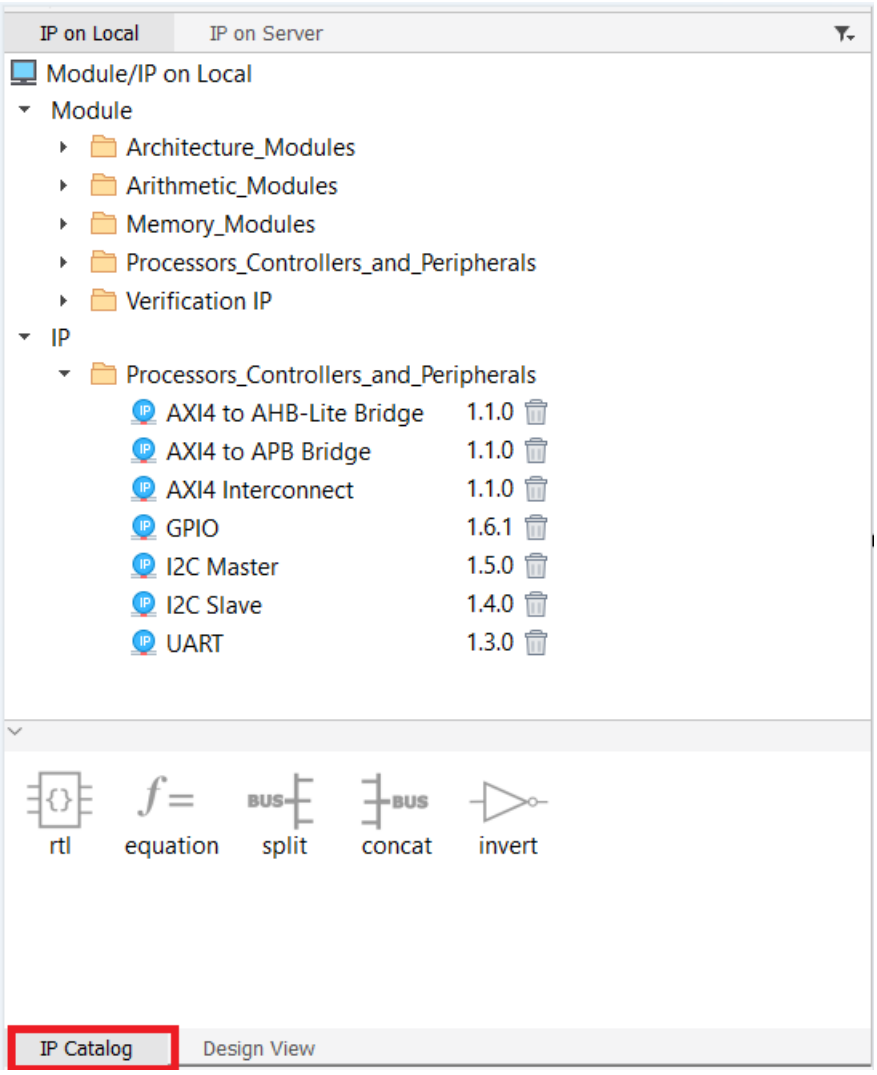

Figure 3.3. IP Catalog tab

4. Click on the  icon (install a user IP) .
5. Install DisplayPort IP, Video Scaler IP and the two custom IPs (Clock Controller and DP to VS Converter). Browse to the location of all four IPs and Select the **.ipk** IP packages. Click **Open**.

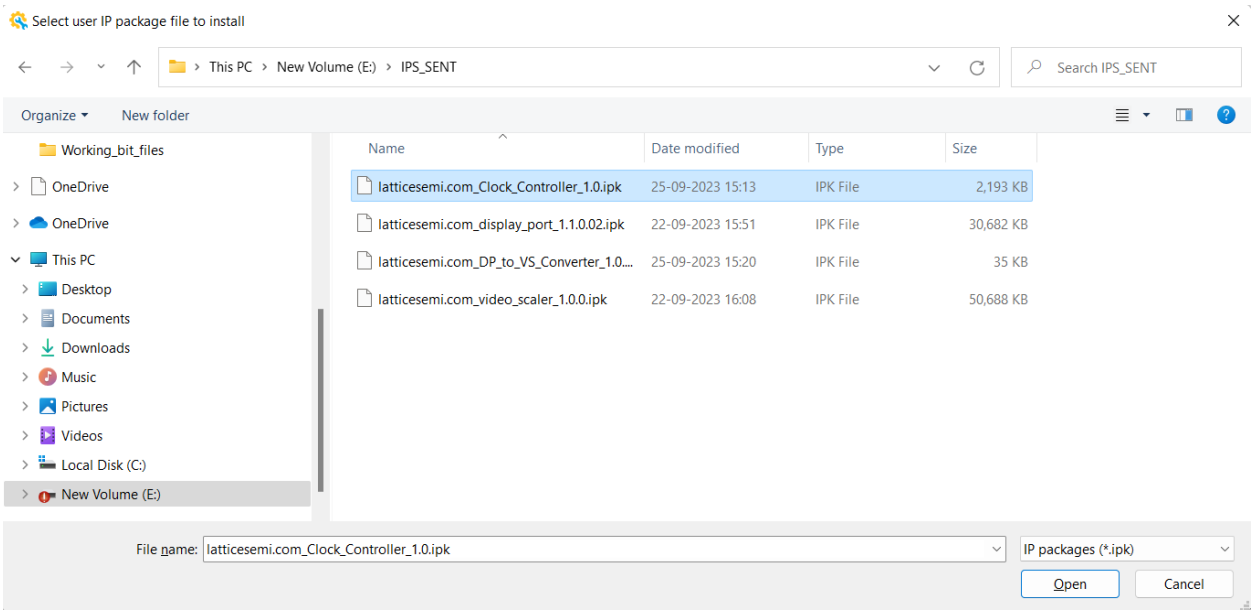

Figure 3.4. IPK Dialog Box

6. Once all the IPs are installed, users can see the IPs under the **IP** column.

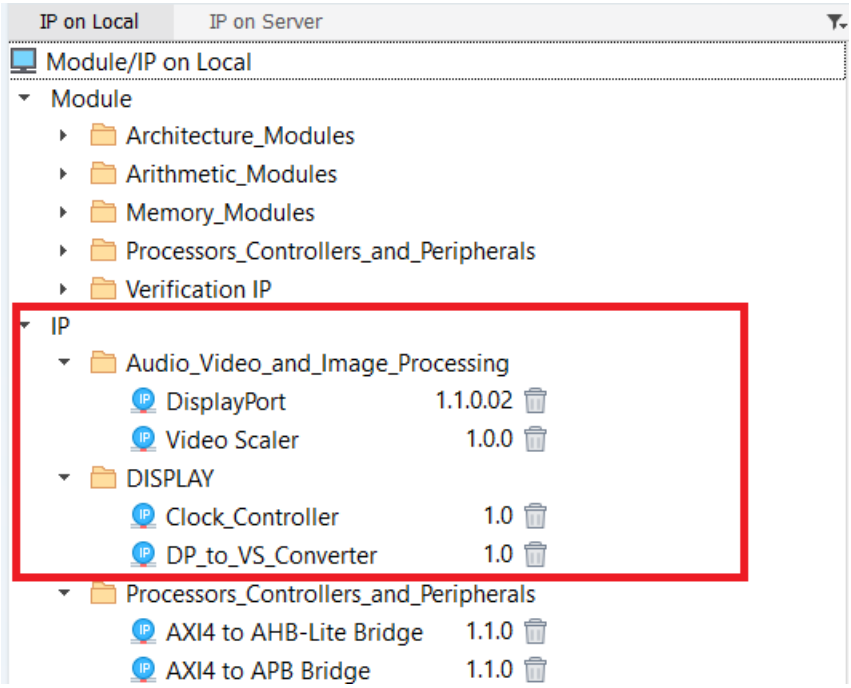

Figure 3.5. IP Column in Propel Builder

7. Open the schematic tab of the design to generate these four IPs. Open the **IP Block Wizard**, click the **Generate** button for each.

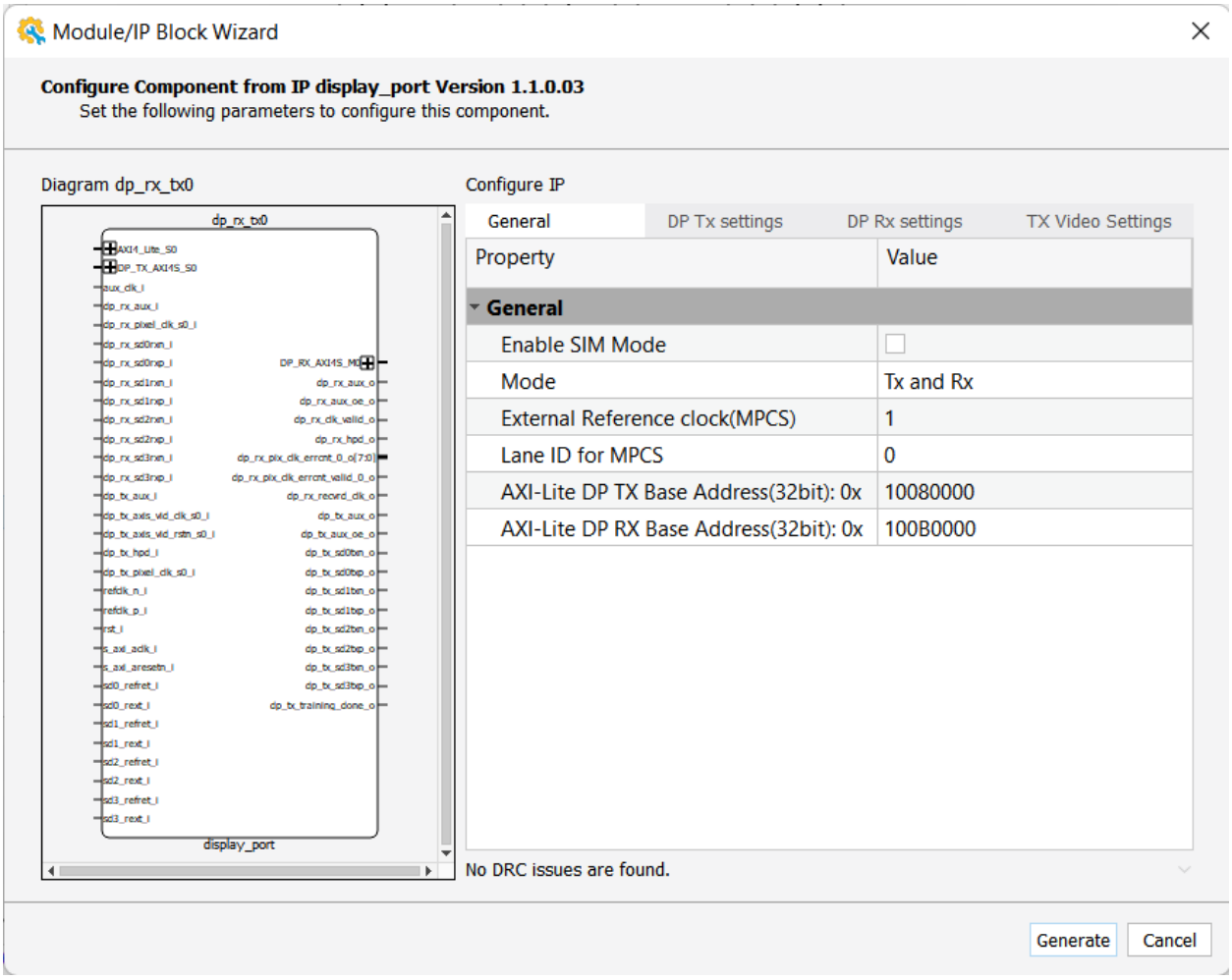

Figure 3.6. Generating IP in Builder

3.2. Modifying the SoC

The provided SoC design can be directly used without modification for 2 PPC data path. The design can be modified to support a different configuration. This section describes the modifications for running and implementing a 4 PPC design. The parameter modification for each IP is shown in the following subsections.

3.2.1. DisplayPort

Table 3.1. DisplayPort IP Modified Parameters

Attribute	Selectable Values	Default	Modified
DP TX Settings			
User Data Interface			
Pixels Per Clock	1, 2, 4	2	4
DP RX Settings			
User Data Interface			
Pixels Per Clock	1, 2, 4	2	4

3.2.2. Video Scaler

Table 3.2. Video Scaler IP Modified Parameters

Attribute	Selectable Values	Default	Modified
Architecture			
General			
Pixels Per Clock	1, 2 and 4	2	4
Frame Dimensions			
Input active pixels	4096	2560	3840
Input active lines	32-4096	1440	2160
Output active pixels	32-4096	2560	3840
Output active lines	32-4096	1440	2160
Output Hblank Pixels	0-4096	740	740
Output Vblank Lines	0-4096	60	90
Algorithm			
Scaling method	Nearest, Bilinear, Bicubic, Lanczos	Bicubic	Nearest
Number of vertical filter taps	-	4	1 (Default for Nearest)
Number of horizontal filter taps	-	4	1 (Default for Nearest)
Number of vertical filter phrases	16, 32, 64, 128, 256	16	16 (Default for Nearest)
Number of horizontal filter phrases	16, 32, 64, 128, 256	16	16 (Default for Nearest)
Coefficient width	6, 7, 8, 9, 10, 11, 12, 13, 14, 15	9	9

3.2.3. DP to VS Converter

Table 3.3. DP to VS Converter IP modified Parameters

Attribute	Selectable Values	Default	Modified
General			
Pixels Per Clock	1, 2, 4	2	4

Note - For 4 PPC design, after modifying the above parameters, the users can proceed as mentioned in the Opening Project in Radiant section.

3.3. Validating and generating the design

Click on the **Validate Design** icon**,** and then the **Generate** icon at the top of the builder GUI as shown.

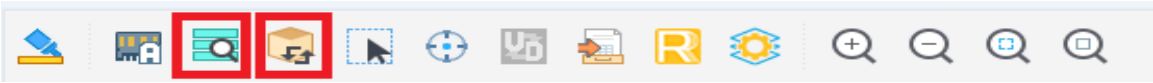

Figure 3.7. GUI Icon in Propel Builder

Note: If the user is changing the parameter of any IP, they should first click the **Validate Design** icon, and then the **Generate** icon. After **Generate** is complete, proceed to the Opening Project in Radiant section.

3.4. Opening Project in Radiant

After clicking **Generate** in Propel Builder, a Radiant project file (.rdf file) for the SoC design is automatically created by the Propel Builder.

Figure 3.8. Radiant Icon in Propel Builder

To launch Radiant Software:

- Click on the **Radiant** icon as shown in Figure 3.8.
- Lattice Radiant is launched with a Radiant project generated for SoC at background as shown in Figure 3.9.

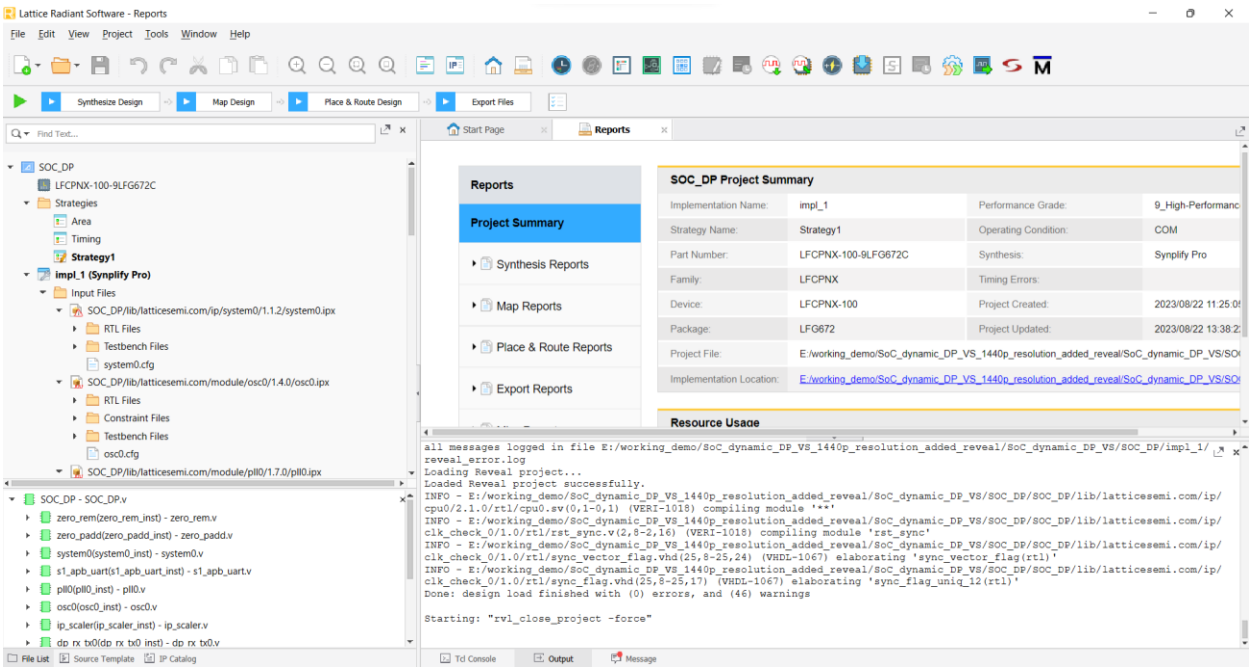

Figure 3.9. Radiant Project

- Click **Synthesize Design**.

Figure 3.10. Synthesize Design

Note: Once the design is synthesized, the user needs to open **Post Synthesis Timing Constraint Editor** as shown:

Figure 3.11. Post Synthesis Timing Constraint Editor Dialog Box

- Click on the **Generated Clock** tab and generate Tx core and Rx core clocks, namely **CH0_PIPE_PCS_TXCLKOUT** and **CH3_RXOUTCLK** by double clicking on "…" and opening **Object Edit** as shown in Figure 3.12 and Figure 3.13. Click **OK** after selecting the relevant clock pin.

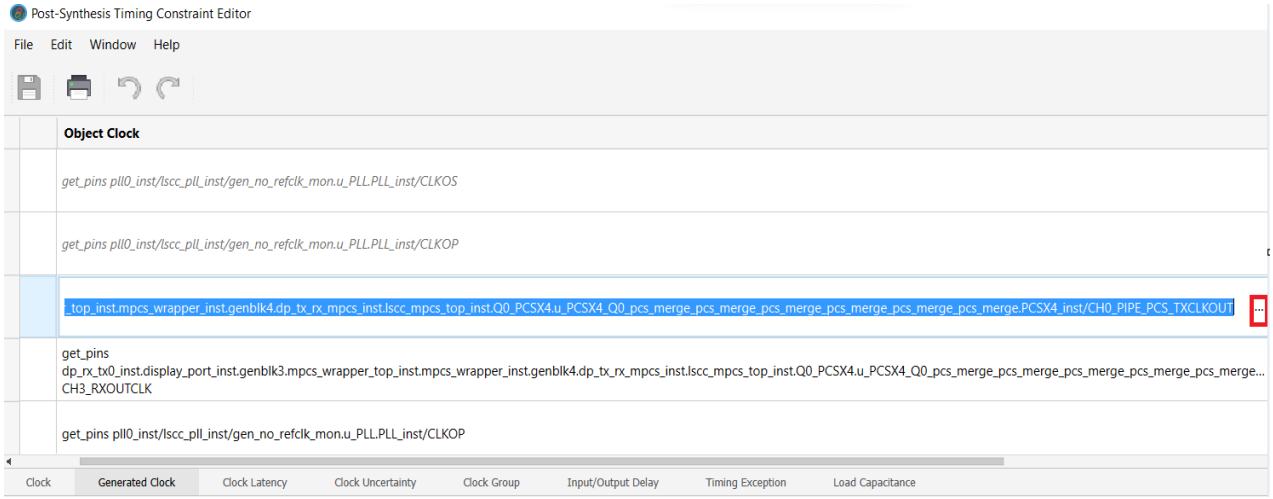

Figure 3.12. Generated Clock Tab

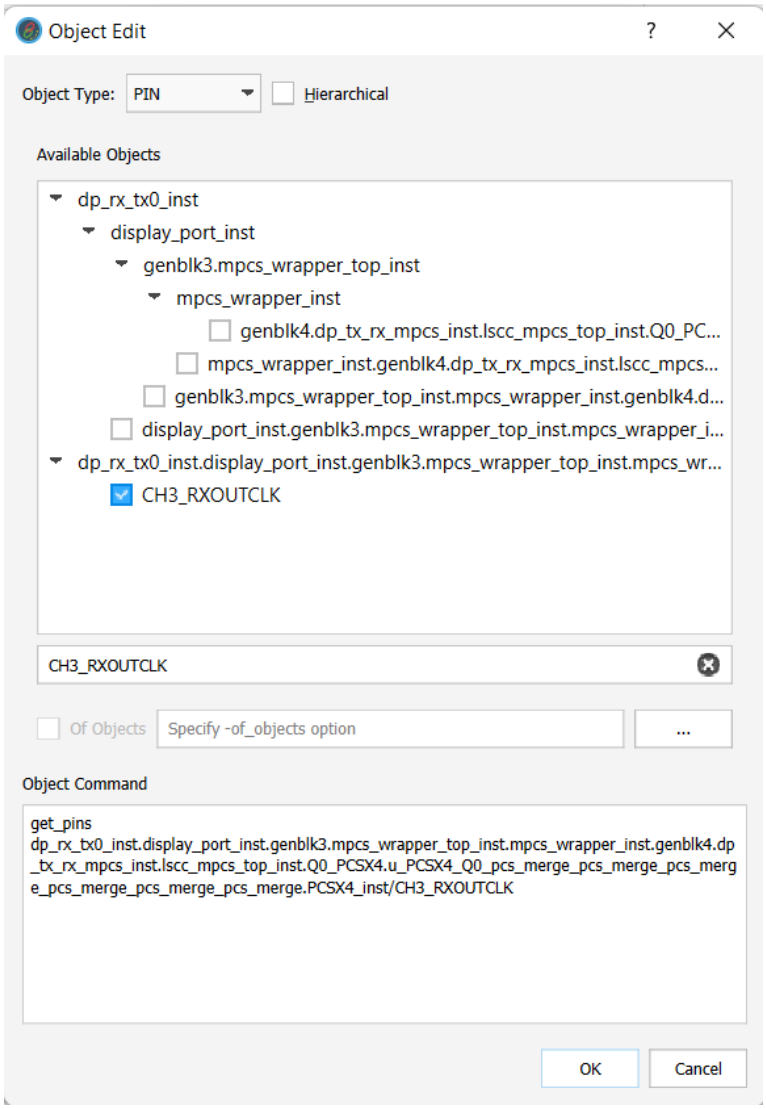

Figure 3.13. Object Edit Dialog Box

- After adding the clock constraints, save and close the Post Synthesis Timing Constraint Editor.

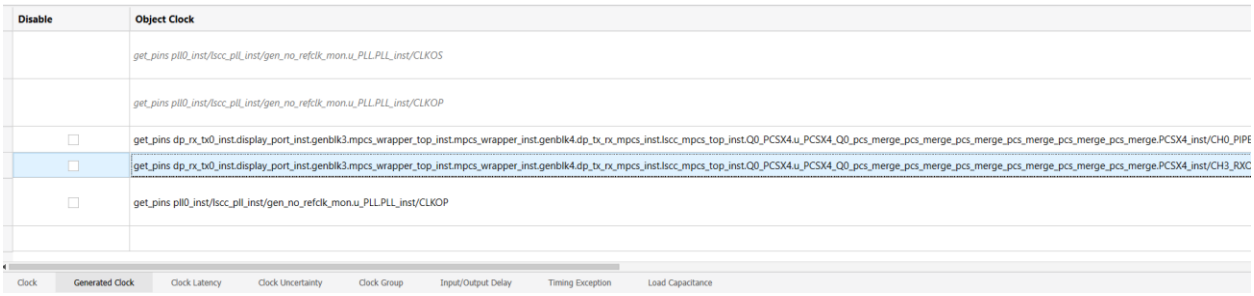

Figure 3.14. Saving the Post Synthesis Timing Constraint Editor Dialog Box

- Click **Export Files** to generate the bitstream.

Figure 3.15. Export Files

3.5. Uploading the bit file to the FPGA

This section guides the users through the process of uploading the bitstream (.bit file) through fast configuration. Follow the instructions below:

1. Click on the windows button, search and open the **Lattice Radiant Programmer** software. It opens a dialog box as shown in Figure 3.16 and select the project name, location and click on **OK**.

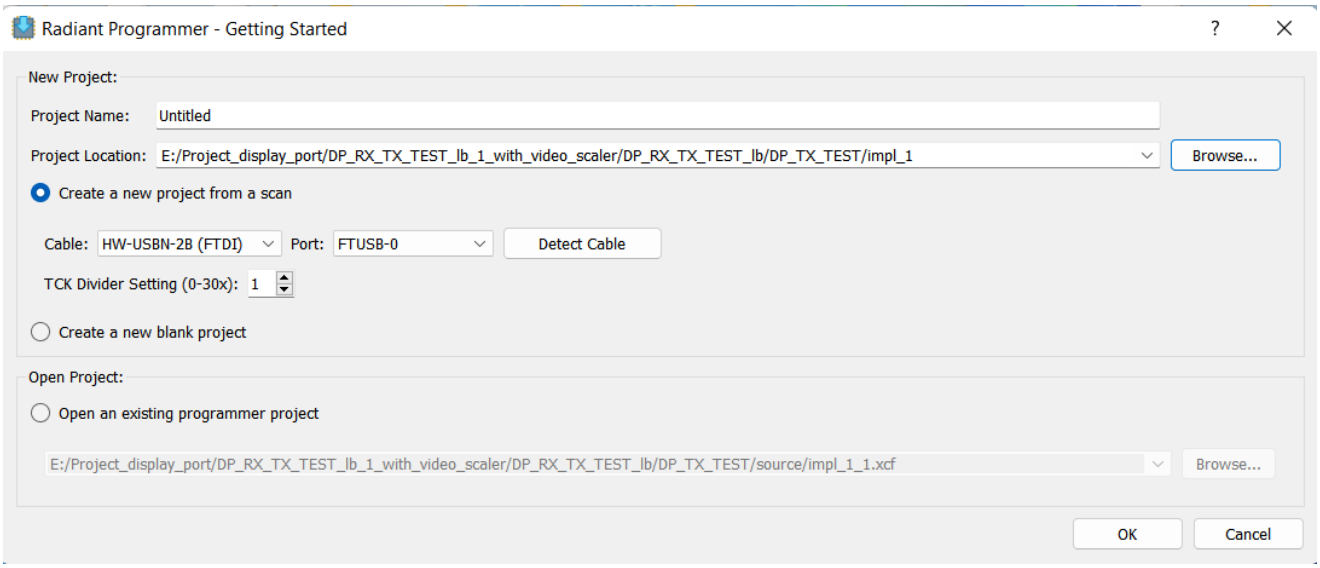

Figure 3.16. Radiant Programmer Dialog Box

2. Select the device name as LFCPNX-100 and choose the bit file to be programmed from the implementation directory as shown in Figure 3.17.

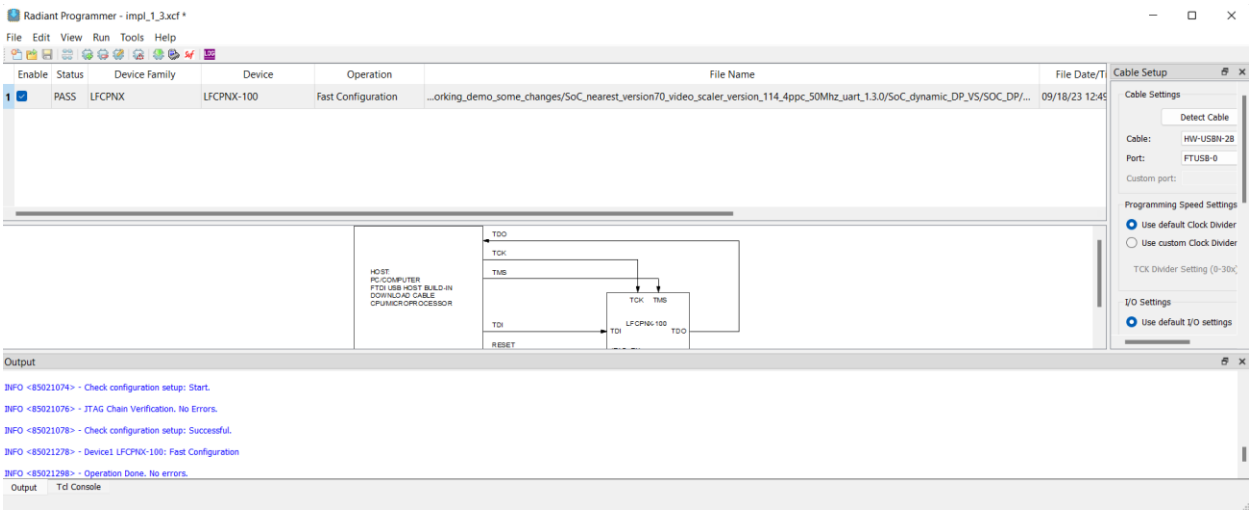

Figure 3.17. Radiant Programmer Window

3. Click on the **Program Device** toolbar icon ( ).

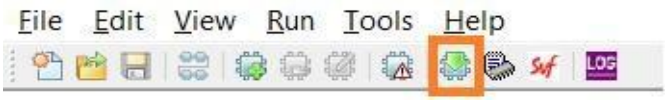

Figure 3.18: Program Device Toolbar Icon

4. Check on the output window, where the status of the program device should be "**Operation: successful"** as shown.

Figure 3.19. Output Window

4. Demonstration

This chapter discusses the running of demonstration using RISC-V. The demo has various IPs such as DP, Oscillator, Video Scaler, and Clock Controller IPs. The demo supports dynamic configuration of Video Scaler IP. The LEDs can be observed to know the status of the demonstration. The sequence of operation in the Demo is described in the following steps.

1. Any terminal program using USB based serial port can be used to display the status of the demonstration. This document describes the steps when using the terminal application, PuTTY, a free and open-source software for Windows.
2. On opening PuTTY, the app asks for connection type and speed as shown in Figure 4.1. Select Connection Type as **Serial**, enter the appropriate serial port and set the speed to **115200**.

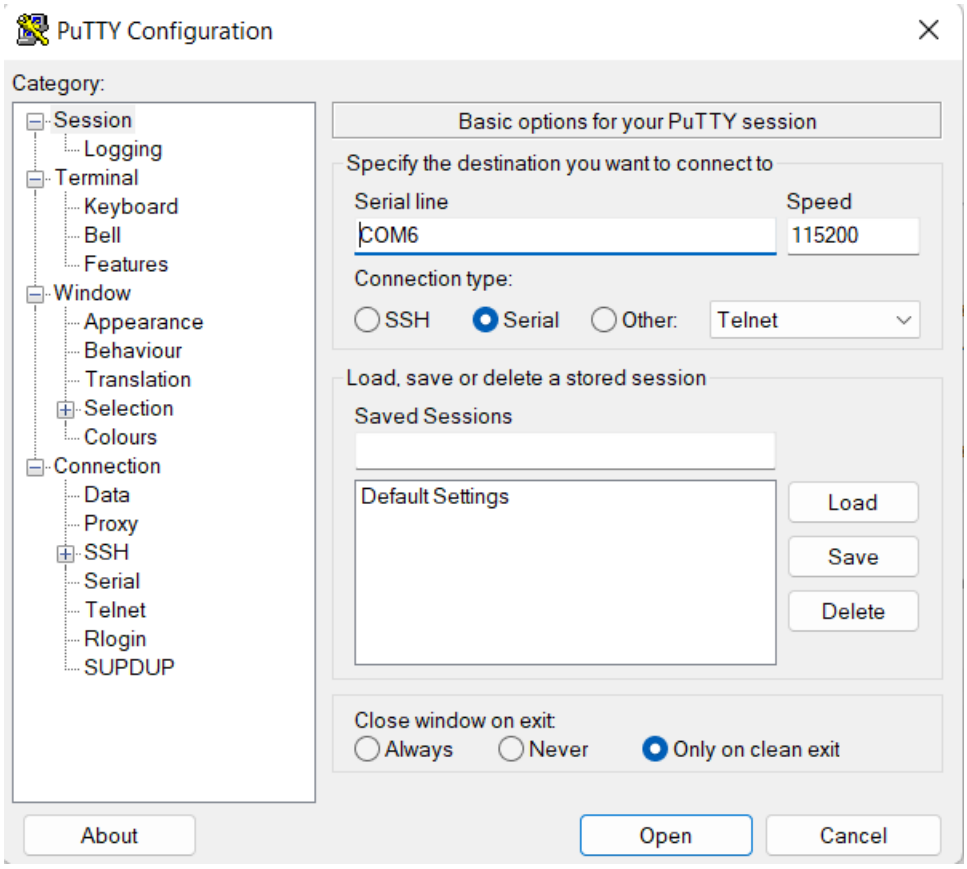

Figure 4.1. PuTTY Configuration Window- Port Selection

3. Click on the **Open** button and the PuTTY terminal opens. Press the reset push button (SW1) on the evaluation Board and the demo starts as shown in Figure 4.2.

```
************************************************************
*        Lattice Semiconductor. All rights reserved.       *
*                                                          *
*                  DP Video Scaler DEMO                    *
************************************************************
```

Figure 4.2. PuTTY Window

4. Current Bitfile Configuration (PPC, BPC and Pixel Format) is shown. The users are asked to select both Input and Output resolutions. Press 1 for 720p, 2 for 1080p, and 3 for 1440p resolution.

```
*              Current Bitfile configuration                *
PPC              : 2
BPC              : 8
Pixel Format : RGB

Select Input resolution :
Press 1 for 1280 x 720p
Press 2 for 1920 x 1080p
Press 3 for 2560 x 1440p

Input resolution selected : 1280 x 720p

Select Output resolution :
Press 1 for 1280 x 720p
Press 2 for 1920 x 1080p
Press 3 for 2560 x 1440p

Output resolution selected  : 1920 x 1080p
```

Figure 4.3. Input and Output Configuration

5. Pixel Clk 0 and Pixel Clk 1 are set according to the resolution given by user and PPC of the bitstream.

```
Pixel Clk 0 set to 37.125MHz
Pixel Clk 1 set to 74.25MHz
```

Figure 4.4. Pixel Clock Set Information

6. Parameters related to Video Scaler (FRMWIDTH, FRMHEIGHT, OUTWIDTH, OUTHEIGHT, HBLANKOUT, VBLANKOUT, VSFACTOR, HSFACTOR, and UPDATE) are printed. The information related to DP Rx is shown.

```
Video Scaler Parameters

************************************************************
FRMWIDTH set to 1280
FRMHEIGHT set to 720
OUTWIDTH set to 1920
OUTHEIGHT set to 1080
HBLANKOUT set to 280
VBLANKOUT set to 45
VSFACTOR set to 1365
HSFACTOR set to 2730
UPDATE bit set to 1
************************************************************
```

Figure 4.5. Video Scaler Parameters

7. DP Rx capabilities (EDID info, Max Lane rate and Max Lane count) are printed.

```
################################################################
########              DP Rx EDID Info                  ########
################################################################
       Manufacturer:  LSC
       Monitor Name:  LATTICE_DP
Prefered Resolution:  3840x2160p(4k)
################################################################

RX - Max_lane_rate : 5.4 Gbps(HBR2)

Enhance Framing Enabled!

RX - Max link count is configured : 0x4
```

Figure 4.6. Rx EDID Information

8. DP Rx training is initialized. If a valid DP source device is not connected user will get an error as shown in Figure 4.7.

```
################################################################
########      DP Rx Link Training                   ########
################################################################
Upstream (DP source to board) link up process started!
Upstream link training started!

Upstream training is unsuccessful

DP RX State : Ready for training state
MPCS is not ready.

Press On board reset/power cycle the board to restart the demo!

Trying to retrain Upstream link

To Restart the Demo press On board reset or power cycle the board!
Press 1 to Refresh
Press 2(RT) to restart training
Press 3(RS) to restart demo
```

Figure 4.7. DP Rx Training Unsuccessful

9. At this point, check if the DP Rx cable is properly connected to the source and the FMC card on the Evaluation board, then press (2) or (3) to continue the process. If the DP source is set to output the selected resolution and the cable is properly connected, DP Rx completes the training and gives the result as shown in Figure 4.8.

```
########      DP Rx Link Training                    ########
############################################################
Upstream (DP source to board) link up process started!
Upstream link training started!

Upstream link training is successful!
Lane Count : 4 Lanes
Link Rate  : 5.4 Gbps

Lane 0 Clock Recovery Done
Lane 1 Clock Recovery Done
Lane 2 Clock Recovery Done
Lane 3 Clock Recovery Done
Lane 0 Channel Equalization Done
Lane 1 Channel Equalization Done
Lane 2 Channel Equalization Done
Lane 3 Channel Equalization Done
Lane 0 Symbol Locked
Lane 1 Symbol Locked
Lane 2 Symbol Locked
Lane 3 Symbol Locked
Lane Alignment Done
```

Figure 4.8. The Demonstration - DP Rx Link Training

10. MSA will be detected, and RX video stream will start. The resolution received by DP Rx IP will be displayed as shown in Figure 4.9.

```
Waiting for SST based Main Video Stream

MSA Detected
Waiting for Valid video frames

############################################################
########      Main Video Info                    ########
############################################################
RX Video Stream Started:

Resolution    : 1280x720
Scan Type     : Progressive
Pixel Format  : RGB888
BPC           : 8
input_resolution :  1
RX Video Stream Resolution validated : 1280x720p
```

Figure 4.9. MSA Detection and Main Video Streaming

11. If the Rx stream resolution does not match the expected input resolution, user will get error as shown in Figure 4.10.

```
Waiting for SST based Main Video Stream

MSA Detected
Waiting for Valid video frames

#################################################################
########      Main Video Info                          ########
#################################################################
RX Video Stream Started:

Resolution   : 1920x1080
Scan Type    : Progressive
Pixel Format : RGB888
BPC          : 8
Invalid Resolution of RX video Stream
Please configure following resolution :1280 x 720p
Press 1 to Restart Demo or Press On Board Reset Button
```

Figure 4.10. MSA Detection and Incorrect Resolution Detected

12. If a Windows PC is used as the DP source, the user needs to make sure that the **Desktop Resolution** is equal to the **Active signal resolution** in the laptop/desktop as shown in Figure 4.11 and Refresh rate as 60 Hz.

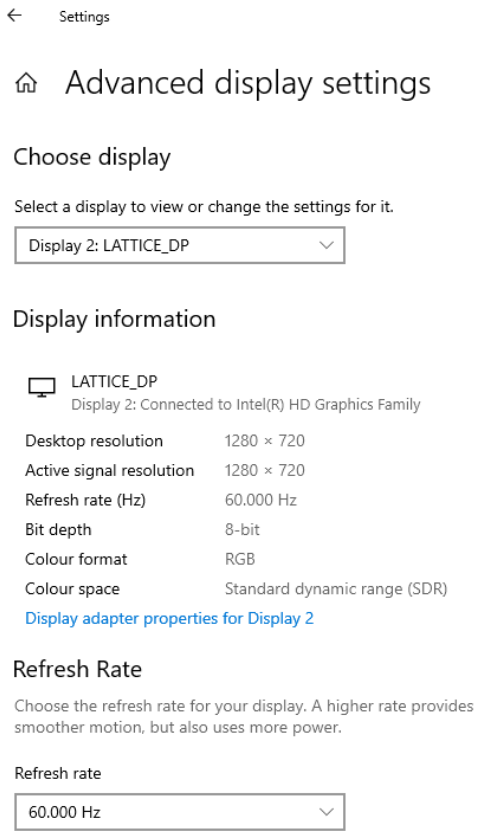

Figure 4.11. Display Settings

13. Then the DP Tx is initialized and the demo waits for the detection of a DP Sink device (such as a monitor). When a valid sink device is detected, it is reported in the terminal as in Figure 4.12.

```
################################################################
########            DP TX Initialized              ########
################################################################
Sink is detected
EDID validated
```

Figure 4.12. DP Tx Initialized (Sink Detected)

14. If a valid sink is not detected, an error message as shown in Figure 4.13 is displayed. Please make sure that a valid DP Sink device is connected to the DP Tx port on the FMC daughter card.

```
############################################################
########           DP TX Initialized            ########
############################################################
Sink is not connected
Trying to detect the sink again
Sink is not connected
```

Figure 4.13. DP Tx Initialized (Sink not Detected)

15. Once the Sink is detected, its maximum capabilities (link rate, lane count and resolution) are displayed as shown in Figure 4.14.

```
Max link rate capability of DP Sink Device  : 5.4 Gbps (HBR2)
Max lane count capability of DP Sink : 0x4
Max resolution capability of DP Sink : 3840x2160
```

Figure 4.14. DP Tx Max Capability

16. Then the onboard PLL status is checked.
17. Once PLL is locked, Tx training will be done, and training configuration is displayed as shown in Figure 4.15.

```
Checking PLL Lock Status

PLL Locked

Transmitter Configuration is Done

Link Up process Started

Training is done
Clock Recovery Successful
Channel Equalization Successful
Symbol Locked

Lane rate and Lane count at which training is done: 5.4 Gbps (HBR2) and 0x4
```

Figure 4.15. DP Tx Training

18. Tx video streaming is enabled, and users should see a scaled output on the monitor.
19. Press 1 in the terminal to restart the whole process.

```
Video Enabled
Press 1 to restart the process
```

Figure 4.16. Video Enabled

20. A picture of the input and output monitors for a 720p to 1080p scaling is shown in Figure 4.17.

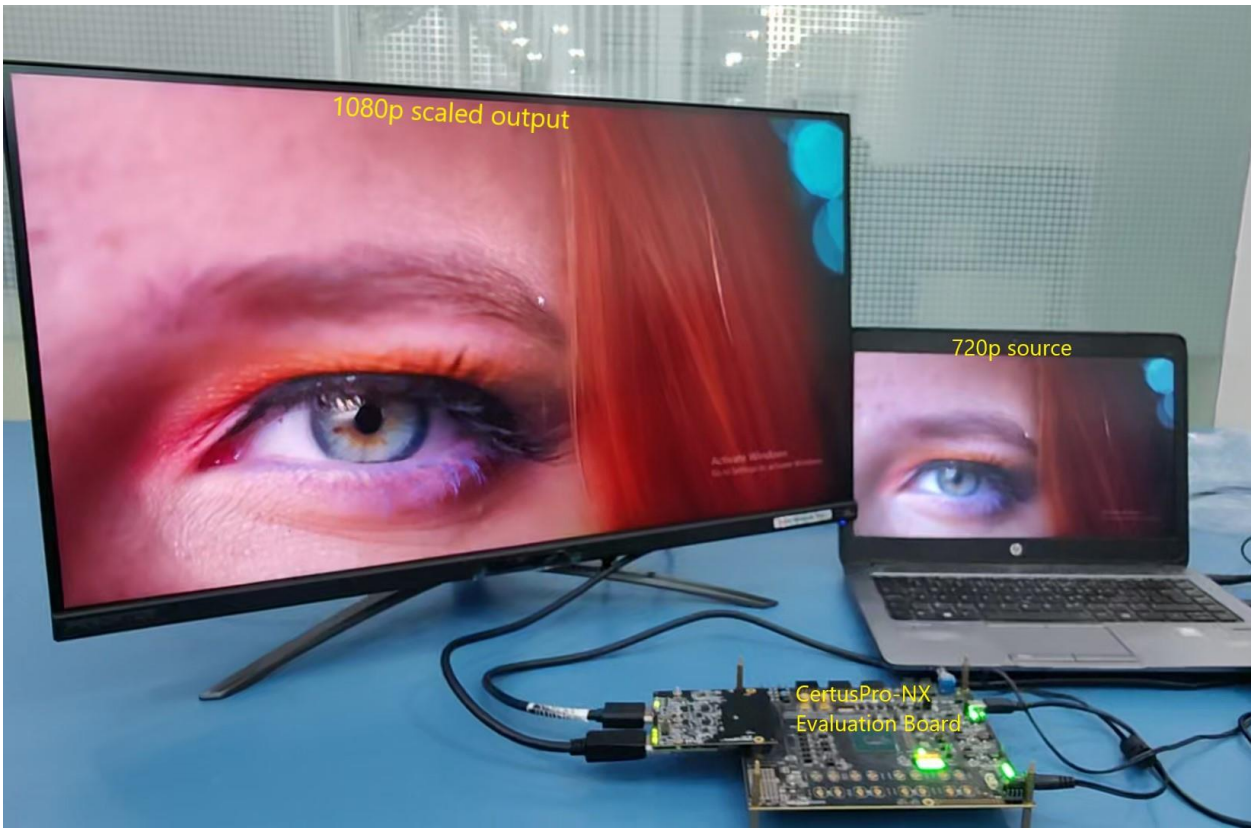

Figure 4.17. 720p to 1080p Live Video Upscaling Dynamically

5. Troubleshooting

Following are some commonly encountered problems in the demonstration and possible solutions.

5.1. LED Troubleshooting Guide

Table 5.1. LED troubleshooting

Evaluation Board	
LED not glowing	**Indication**
D6	Make sure FMC daughter card is properly seated.
D7	Make sure FMC daughter card is properly seated.
D9	Make sure FMC daughter card is properly seated.
D10	If D11 is glowing, then make sure DP Source is connected to a proper input resolution and RX training is completed.
D11	This LED might blink intermittently, indicating the clock recovery algorithm is running. This is completely normal.
D12	Make sure DP Tx training is completed successfully and a valid monitor supporting HBR2 is connected.
D13	Make sure the correct resolution is configured in the DP source device.
FMC Daughter Card	
LED not glowing	**Indication**
LED2	Make sure FMC daughter card is properly seated

5.2. Unresponsive board or terminal

1. Make sure the bitfile is programmed.
2. Also, make sure that Active signal resolution of Rx should match with its Display Resolution and Refresh rate as 60 Hz.
3. Reload the bitstream from the demonstration bitstream directory.
4. Power cycle the board.
5. Make sure that all the connections are proper.
6. Reload the bitstream or press the reset button on the board.

Appendix A: Resource Utilization

Table A.1. Resource Utilization for DP Video Scaler Demo shows the configuration and resource utilization for LFCPNX-100-9LFG672C using Synplify Pro of Lattice Radiant Software 2023.1.

The Configurations listed in the resource utilization table uses the following parameters: SST mode, AXI-Stream Interface, AXI-Lite Interface, 4 lanes, and 5.4 Gbps data rate per lane.

Table A.1. Resource Utilization for DP Video Scaler Demo

Configuration				Resource Utilization		
Pixels per clock	**Bits per component**	**Algorithm**	**Color Format**	**Registers**	**LUTs**	**EBRs**
2	8	Bicubic	RGB	37764	54047	91
4	8	Nearest	RGB	36951	52572	86

References

- DisplayPort IP Core - User Guide (FPGA-IPUG-02236)
- Video Scaler IP-User Guide (FPGA-IPUG-02234)
- ISC-V RX CPU IP - Lattice Propel Builder (FPGA-IPUG-02230)
- UART IP Core - Lattice Propel Builder (FPGA-IPUG-02105)
- CertusPro-NX web page
- Lattice Radiant Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plan.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, December 2023

Section	Change Summary
	Initial release.

www.latticesemi.com