



DisplayPort and Video Scaler

Reference Design

FPGA-RD-02276-1.2

January 2024

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This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AXI	Advanced Extensible Interface
AUX	Auxiliary Channel in DisplayPort
BPC	Bits per color component
DP	DisplayPort
DP Rx	Receiver part of DisplayPort IP
DP Tx	Transmitter part of DisplayPort IP
DUT	Device Under Test
FPGA	Field Programmable Gate Array
GUI	Graphical User Interface
IP	Intellectual property
MPCS	Multiple-Protocol Physical Coding Sublayer
PPC	Pixels per clock

1. Introduction

The DisplayPort and Video Scaler reference design provides a fully simulatable design containing Lattice DisplayPort IP and Lattice Video Scaler IP. The design receives DisplayPort traffic from an external model using DisplayPort IP's receiver part (DP Rx), performs up or down scaling of the video, and generates DisplayPort output using DisplayPort IP's transmitter part (DP Tx). The reference design is delivered as a Lattice Radiant project which includes a full test environment to perform simulation. The reference design is set to perform upscaling from 720p, 60 FPS video to a 1080p, 60 FPS video using bicubic algorithm. However, the design can be easily modified to support other use cases by changing the parameters of the DisplayPort and Video Scaler IPs, and regenerating them. As the IPs are independently configurable, care must be taken to configure them consistently to ensure correct functionality of the connected system.

1.1. Quick Facts

Table 1.1. Quick Facts

IP Requirements	Supported FPGA Families	CertusPro™-NX
Supported FPGA Families	Targeted Devices	LFCPNX-100
Design Tool Support	Lattice Implementation	Lattice Synthesis Engine
	Synthesis	Synopsys® Synplify Pro for Lattice
	Simulation	For a list of supported simulators, see the Lattice Radiant software user guide.

1.2. Features

The key features of DisplayPort and Video Scaler reference design are as follows.

- Up scaling
- Down scaling
- Scaling from/to a wide range of resolutions
- Easy reconfiguration of DP and Video Scaler IPs through respective IP GUIs
- Dynamic reconfiguration of input/output resolutions
- Full self-checking testbench with data generator and data checker included

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal Names that end with:

- `_n` are active low
- `_i` are input signals
- `_o` are output signals
- `_io` are bi-directional input/output signals

2. Functional Description

The DisplayPort and Video Scaler reference design is also referred to as DisplayPort-Video Scaler top level design (DS_VS_TOP) or device under test (DUT) in this document. The DUT is comprised of DP Rx, Video Scaler IP, and DP Tx. The included testbench, referred to as top-level testbench (TB_TOP) in this document, comprises of AXI-Stream Data Generator, AXI-Stream Data Checker, DP Tx and DP Rx. The functional blocks in the reference design and testbench with their connectivity are shown in [Figure 2.1](#). The testbench initially configures the two DP IPs over the AXI-Lite interface with the parameters calculated according to the input and output resolutions selected by the user. Training sequence is initiated for both the serial data links by configuring the corresponding register in the DP IPs. Once training is completed, DP Tx sends the data generated by the AXI-Stream Data Generator. DP Rx receives and sends the video stream to Video Scaler IP for either up scaling, down scaling or direct pass through (based on user selected parameters). The output of Video Scaler IP is sent to DP Tx. The serial output of DP Tx comes out of DP_VS_TOP and received by DP Rx of the test bench. Finally, the video data from DP Rx is compared with the original data transmitted by the AXI-Stream data generator by the AXI-Stream Data Checker.

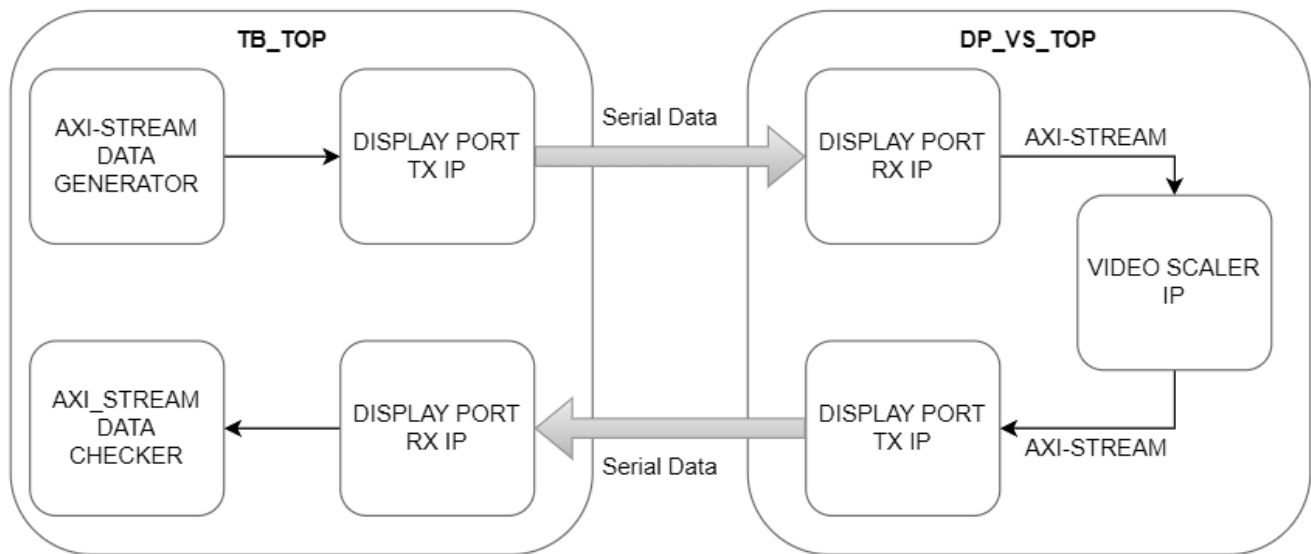


Figure 2.1. DP Video Scaler Reference Design with Testbench

The major functional blocks of the reference design and test bench are described below:

2.1. TB_TOP

This is the top-level module for the test bench. The tb_top module has AXI-Stream Data Generator, AXI-Stream Data Checker and DP IP. Here, DP IP is used to generate serial data from AXI-Stream and vice-versa. The test bench is connected to the DUT (DP_VS_TOP module).

2.1.1. AXI-Stream Data Generator

This module generates different types of patterns according to the resolution that is tested. A pseudo random pattern is generated when the parameter, VS_ATTACH (refer to [Parameter Settings](#)) is set to 0. Otherwise, video data is generated using the Video Scaler IP.

For more information on the Video Scaler IP, refer to the [Video Scaler IP User Guide \(FPGA-IPUG-02234\)](#).

2.1.2. AXI-Stream Data Checker

This module checks the AXI data received by DP Rx and compares it with the appropriate golden output. When Video Scaler is attached, the received data is compared with the golden data generated by video scaler IP. Otherwise, the received data is compared with the generated pseudo random bit sequence.

2.2. DP_VS_TOP

This module is the top DUT module. It contains DP Rx, DP Tx and Video Scaler IPs. It receives the video data from the test bench through DP main channel serial interface, passes it through the cascaded combination of DP Rx, video scaler and DP Tx and sends the output data to the testbench through DP main channel serial interface.

For more information on the Video Scaler IP and DP IP, refer to the [Video Scaler IP User Guide \(FPGA-IPUG-02234\)](#), and the [DisplayPort IP User Guide \(FPGA-IPUG-02236\)](#) respectively.

3. Signal Description

The input/output interface signals for DP_VS_TOP module is shown in Table 3.1.

Table 3.1. Primary I/O

Port Name	I/O	Width	Description
refclk_p_i	In	1	Serdes differential reference clock. The clock frequency is 135 MHz for all lane rates except 1.62 Gbps, for which the clock rate is 81 MHz.
refclk_n_i	In	1	Complementary (negative) input to refclk_p_i
aux_clk_i	In	1	This signal is 100 MHz clock used in AUX interface
in_res_clk	In	1	Pixel clock for Input Resolution
out_res_clk	In	1	Pixel clock for Output Resolution
vs_core_clk_i	In	1	If dynamic reconfiguration is enabled, vs_core_clk_i needs to be connected to the faster clock depending on whether the IP is configured for upscaling or downscaling.
dp_rx_recvrd_clk_o	Out	1	Recovered clock from Serdes receiver
dp_rx_clk_valid_o	Out	1	Output clock valid coming from RX side
rst_i	In	1	Active high asynchronous reset of minimum 100 us duration
dp_tx_aux_o	Out	1	Output signal for AUX channel
dp_tx_aux_oe_o	Out	1	Tri-state control for AUX channel. If the value is '1', the AUX output is driven, otherwise it is undriven and held at high impedance state.
dp_tx_aux_i	In	1	Input signal from AUX channel
dp_tx_hpd_i	In	1	Hot plug detect signal to inform DP source that DP sink is connected
dp_tx_training_done_o	Out	1	Tx output signal to inform that training has been done at Tx side
dp_rx_sd0rxp_i	In	1	This is lane0 serial data_p signal of DP RX main channel
dp_rx_sd0rxn_i	In	1	This is lane0 serial data_n signal of DP RX main channel
dp_rx_sd1rxp_i	In	1	This is lane1 serial data_p signal of DP RX main channel
dp_rx_sd1rxn_i	In	1	This is lane1 serial data_n signal of DP RX main channel
dp_rx_sd2rxp_i	In	1	This is lane2 serial data_p signal of DP RX main channel
dp_rx_sd2rxn_i	In	1	This is lane2 serial data_n signal of DP RX main channel
dp_rx_sd3rxp_i	In	1	This is lane3 serial data_p signal of DP RX main channel
dp_rx_sd3rxn_i	In	1	This is lane3 serial data_n signal of DP RX main channel
dp_tx_sd0txp_o	Out	1	This is lane0 serial data_p signal of DP TX main channel
dp_tx_sd0txn_o	Out	1	This is lane0 serial data_n signal of DP TX main channel
dp_tx_sd1txp_o	Out	1	This is lane1 serial data_p signal of DP TX main channel
dp_tx_sd1txn_o	Out	1	This is lane1 serial data_n signal of DP TX main channel
dp_tx_sd2txp_o	Out	1	This is lane2 serial data_p signal of DP TX main channel
dp_tx_sd2txn_o	Out	1	This is lane2 serial data_n signal of DP TX main channel
dp_tx_sd3txp_o	Out	1	This is lane3 serial data_p signal of DP TX main channel
dp_tx_sd3txn_o	Out	1	This is lane3 serial data_n signal of DP TX main channel
dp_rx_hpd_o	Out	1	Hot plug signal to inform DP source that DP sink is connected
dp_rx_aux_oe_o	Out	1	Tri-state control for AUX channel output. If the value is '1', the AUX output is driven, otherwise it is undriven and held at high impedance state.
dp_rx_aux_i	In	1	AUX channel input
dp_rx_aux_o	Out	1	AUX channel output
vs_frm_invalid_o	Out	1	This signal is asserted high if the SOF of current frame is not aligned to the first pixel data. There will be no output from the IP when this is asserted high. It will be de-asserted on the next frame's SOF if it is correctly aligned.
vs_blanking_data_o	Out	[AXIS_DATA_WIDTH-1:0]	Input data received during blanking period
vs_blanking_valid_o	Out	1	This signal asserts high when valid blanking data passed to output

Port Name	I/O	Width	Description
vs_input_hblank_o	Out	1	Input Frame horizontal blanking period
vs_input_vblank_o	Out	1	Input Frame vertical blanking period
Display Port AXI-Lite Interface			
dp_s_axi_aclk_i	In	1	AXI-Lite interface clock
dp_s_axi_aresetn_i	In	1	AXI reset (active low)
dp_s_axi_awvalid_i	In	1	Write address valid
dp_s_axi_awready_o	Out	1	Write address ready
dp_s_axi_awaddr_i	In	[AXIS_ADDR_WIDTH-1)	Write address
dp_s_axi_awprot_i	In	3	Protection type
dp_s_axi_wvalid_i	In	1	Write data valid
dp_s_axi_wready_o	Out	1	Write data ready
dp_s_axi_wdata_i	In	32	Write data
dp_s_axi_wstrb_i	In	4	Write strobe
dp_s_axi_bvalid_o	Out	1	Write response valid
dp_s_axi_bready_i	In	1	Write response ready
dp_s_axi_bresp_o	Out	2	Write response
dp_s_axi_arvalid_i	In	1	Read address valid
dp_s_axi_arready_o	Out	1	Read address ready
dp_s_axi_araddr_i	In	32	Read address
dp_s_axi_arprot_i	In	3	Read protection type
dp_s_axi_rvalid_o	Out	1	Read data valid
dp_s_axi_rready_i	In	1	Read data ready
dp_s_axi_rdata_o	Out	32	Read data
dp_s_axi_rresp_o	Out	2	Read data response
Video Scaler AXI-Lite Interface			
vs_axi_lite_clk_i	In	1	AXI-Lite clock
vs_axi_lite_rst_n_i	In	1	vs_axi_lite_rst_n_i is an active low global reset signal
vs_aw_valid_i	In	1	Write address valid. This signal indicates that the channel is signaling valid write address and control information.
vs_aw_ready_o	Out	1	Write address ready. This signal indicates that the subordinate is ready to accept an address and associated control signals.
vs_aw_address_i	In	[AXI_LITE_ADDR_WIDTH-1:0]	Write address
vs_aw_prot_i	In	3	Protection type. This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or an instruction access.
vs_w_valid_i	In	1	Write valid. This signal indicates valid write data.
vs_w_ready_o	Out	1	Write ready. This signal indicates that the subordinate can accept the write data.
vs_w_data_i	In	[AXI_LITE_DATA_WIDTH-1:0]	Write data
vs_w_strb_i	In	4	Write strobes. This signal indicates which byte lanes hold valid data. There is one write strobe bit for each eight bits of the write data bus.
vs_b_valid_o	Out	1	Write response valid. This signal indicates that the channel is signaling a valid write response.
vs_b_ready_i	In	1	Response ready. This signal indicates that the manager can accept a write response.
vs_b_response_o	Out	2	Write response. This signal indicates the status of the write transaction.

Port Name	I/O	Width	Description
vs_ar_valid_i	In	1	Read address valid. This signal indicates that the channel is signaling valid read address.
vs_ar_ready_o	Out	1	Read address ready. This signal indicates that the subordinate is ready to accept an address.
vs_ar_address_i	In	[AXI_LITE_ADDR_WIDTH-1:0]	Read address
vs_ar_prot_i	In	3	Protection type. This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or an instruction access.
vs_r_valid_o	Out	1	Read valid. This signal indicates that the channel is signaling the required read data.
vs_r_ready_i	In	1	Read ready. This signal indicates that the Manager can accept the read data and response information.
vs_r_Data_o	Out	[AXI_LITE_DATA_WIDTH-1:0]	Read data
vs_r_response_o	Out	2	Read response. This signal indicates the status of the read transfer.

4. Parameter Settings

This reference design provides the user with the following parameters as shown in [Table 4.1](#).

Table 4.1. Parameters of TB_TOP Module

Parameters	Default Values	Description
VS_ATTACH	1	0 -> No Video Scaler 1 -> With Video Scaler Refer to Figure 2.1 .
PARTIAL_RESOLUTION	1	Integer value with which the Frame Resolutions are divided for faster simulation. Range: [1, 10]
HBLANKIN	370	Video scaler GUI doesn't have an option for input blanking; hence the user needs to give the correct Horizontal Blanking value for the Input Resolution. This value should be modified accordingly if PARTIAL_RESOLUTION is greater than 1.
VBLANKIN	30	Video scaler GUI doesn't have an option for input blanking; hence the user needs to give the correct Vertical Blanking value for the Input Resolution. This value should be modified accordingly if PARTIAL_RESOLUTION is greater than 1.
FPS	60	Frames per second
FRAME_COUNT	4	Number of frames to run for the simulation

If the parameter VS_ATTACH is set to 0, then the reference design works as described in [Figure 4.1](#). If VS_ATTACH is equal to 1, then the reference design works as described in [Figure 2.1](#).

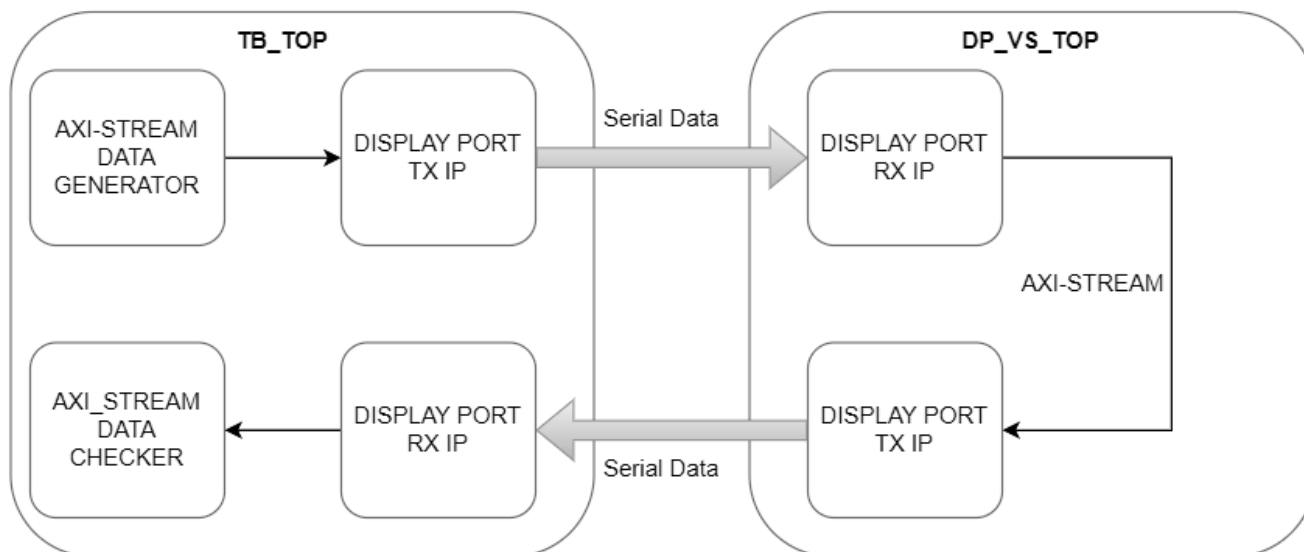


Figure 4.1. DP Pass Through Core Block Diagram

5. Opening and Running the Project

This section provides information on how to open and run the simulation of DisplayPort and Video Scaler Reference Design using Lattice Radiant software. For more details on Lattice Radiant software, refer to the [Lattice Radiant software](#) user guide.

Note: Skip steps 3 to 7 when running the simulation for default resolutions (720p to 1080p and 2 PPC).

5.1. Opening project to run simulation

To run the DP and Video Scaler RD project in Lattice Radiant software, follow these steps:

1. Click **Open Project** on home screen of **Radiant Software** and then open the existing project file, dp_vs_rd.rdf as shown in [Figure 5.1](#).

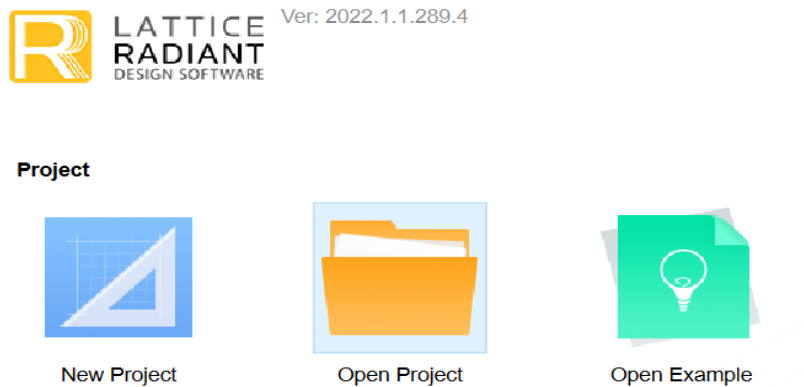


Figure 5.1. Open Project Icon

2. Open the radiant project (.rdf file) in the project directory as shown in [Figure 5.2](#).

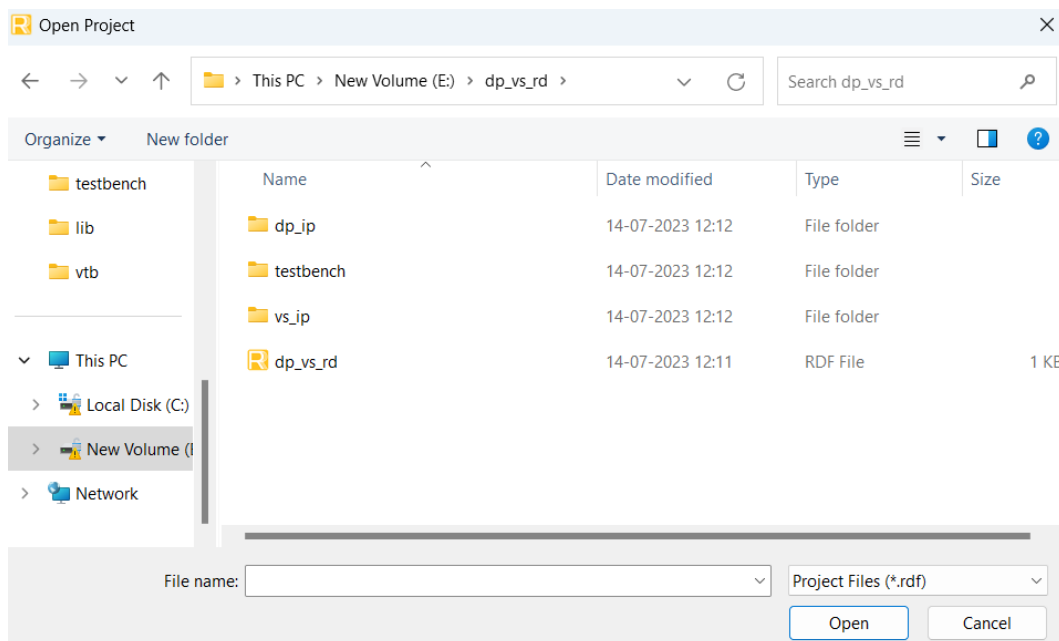


Figure 5.2. Open .rdf project file

- Double click on the **dp_ip.ipx** file to configure the DP IP as shown in Figure 5.3.

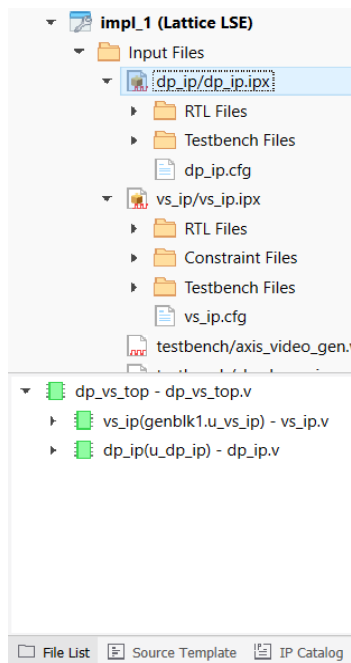


Figure 5.3. Opening dp_ip.ipx

- Select the required parameters as shown in Figure 5.4.

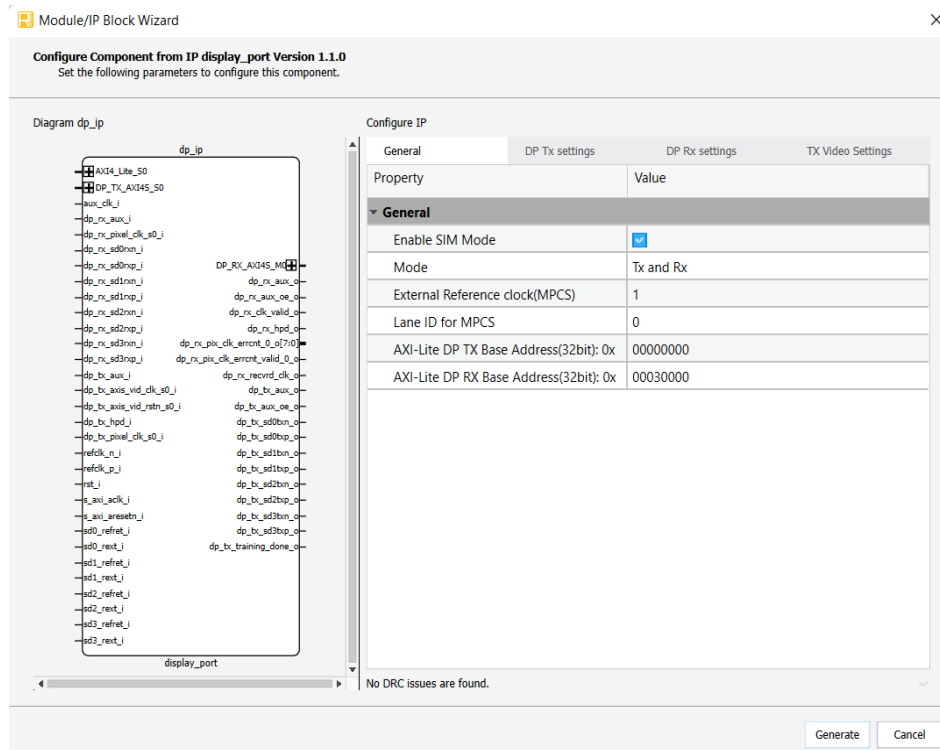


Figure 5.4. Module/IP Block Wizard for dp_ip

Note: Make sure to check Enable SIM Mode parameter in DP IP GUI.

5. Similarly, open the **vs_ip.ipx** file and select the required parameters from the Video Scaler IP GUI as shown in [Figure 5.5](#).

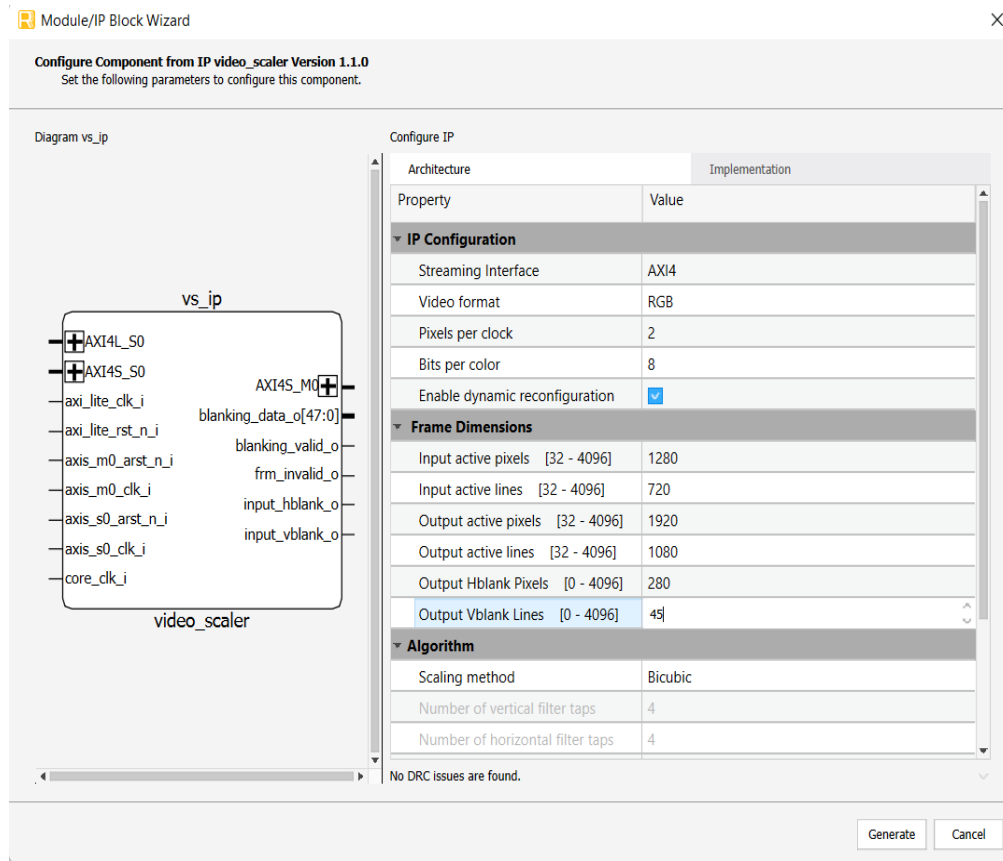


Figure 5.5. Module/IP Block Wizard for vs_ip

Notes:

- Make sure to check Enable dynamic configuration in Video Scaler GUI to avoid errors during simulation.
- Make sure to assign the same values to the common parameters in both IP GUIs. The common parameters in both GUI are mentioned in [Table 5.1](#).

Table 5.1. Common Parameters between DP and Video Scaler

Common Parameters
Pixel Per Clock (PPC)
Bits Per Component (BPC)

- If the value for PARTIAL_RESOLUTION parameter is a number above 1, the Frame Dimensions values must be divided by that parameter. For example, for 720p to 1080p up-scaling with PARTIAL_RESOLUTION set to 5, set the parameters as shown in [Figure 5.6](#). Similarly, divide the parameters (HBLANKIN and VBLANKIN) defined in [Table 4.1](#) by 5.

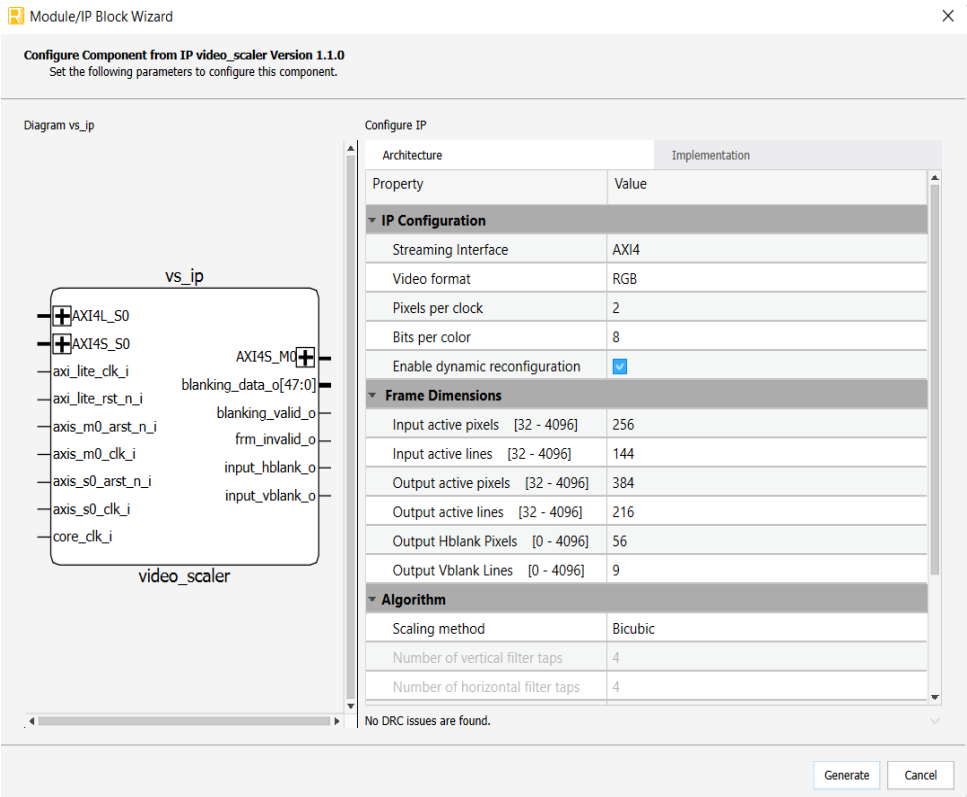


Figure 5.6. Video Scaler IP GUI screen for 720p to 1080p and PARTIAL_RESOLUTION=5

- If the value for PARTIAL_RESOLUTION parameter is a number above 1, make sure to select the *Input FIFO Depth* parameter of Video Scaler as twice its default value. For example, for 720p to 1080p up-scaling with PARTIAL_RESOLUTION set to 5, the Input FIFO Depth is set to 256 in Implementation tab shown in Figure 5.7.

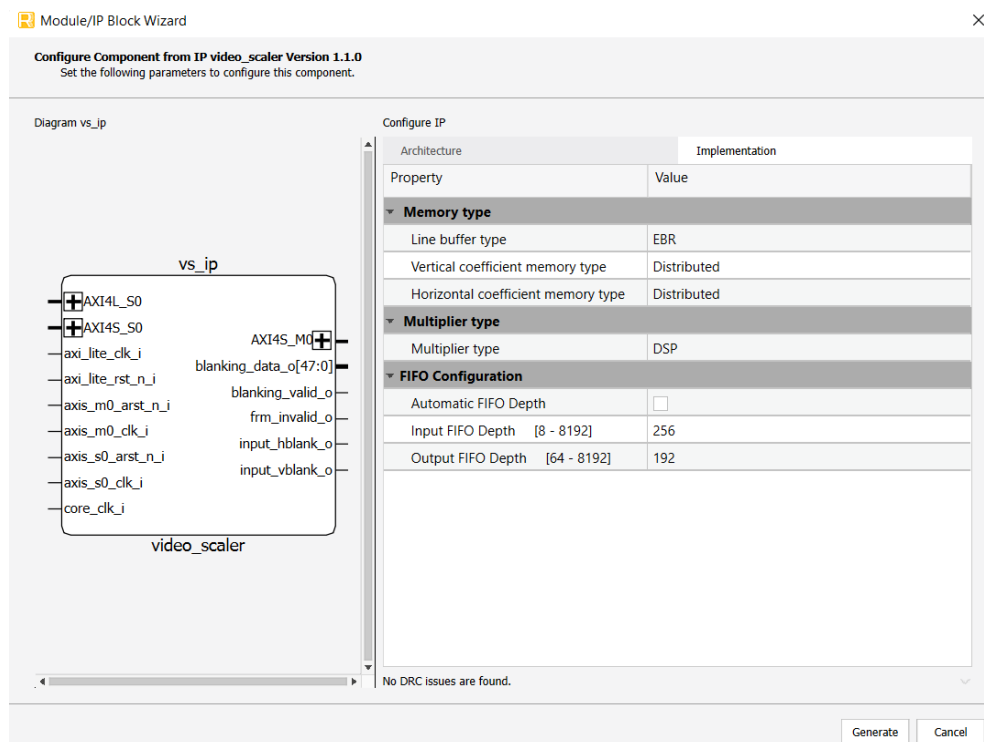


Figure 5.7. Video Scaler IP Implementation tab for 720p to 1080p and PARTIAL_RESOLUTION=5

- Open the **tb_top.v** file as shown in Figure 5.8.

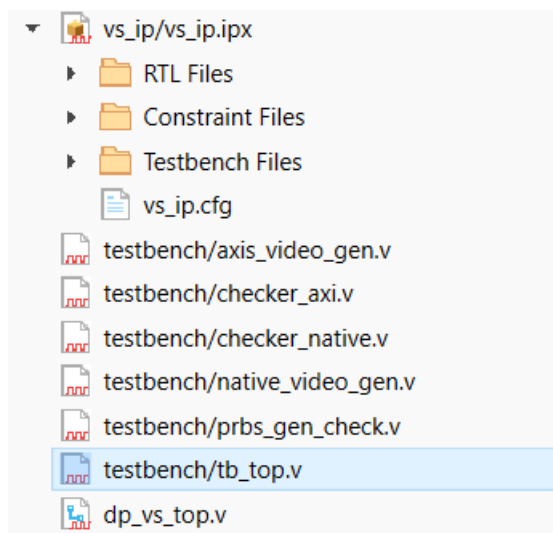


Figure 5.8. Opening tb_top.v file

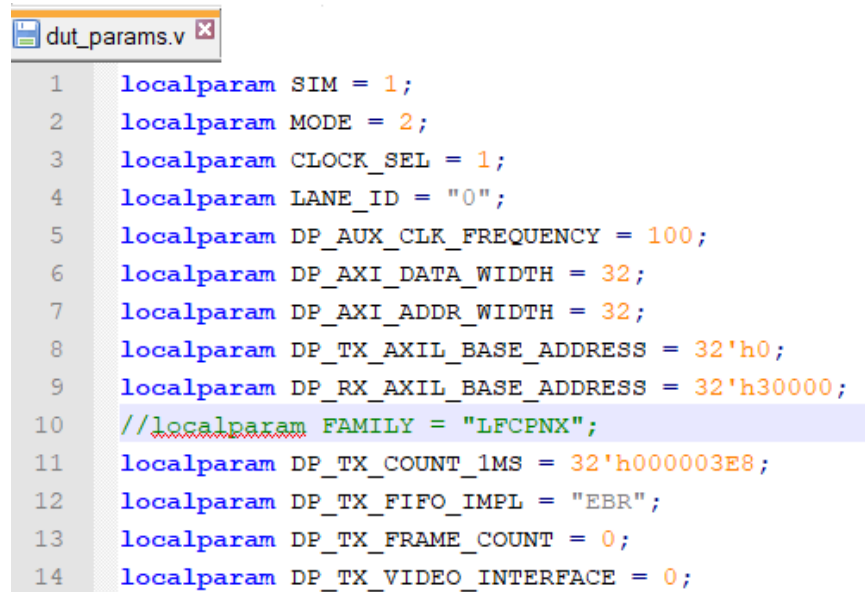
- Set the six parameters defined at the top of the **tb_top** (shown in Figure 5.9) per the required configuration and save the file.

```
`timescale 1ns / 1fs
module tb_top #();
`include "../dp_ip/testbench/dut_params.v"
`include "../vs_ip/testbench/dut_params.v"

parameter VS_ATTACH           = 1 ;
parameter PARTIAL_RESOLUTION  = 5 ;
parameter HBLANKIN           = 74 ;
parameter VBLANKIN           = 6 ;
parameter FRAME_COUNT        = 4 ;
parameter FPS                 = 60 ;
```

Figure 5.9. Setting parameters in tb_top

Note: Comment out the **FAMILY** parameter in any one of the **dut_params.v** files, **dp_ip/testbench/dut_params.v** or **vs_ip/testbench/dut_params.v** as shown in Figure 5.10 to avoid duplicate definition error.



```
dut_params.v
1 localparam SIM = 1;
2 localparam MODE = 2;
3 localparam CLOCK_SEL = 1;
4 localparam LANE_ID = "0";
5 localparam DP_AUX_CLK_FREQUENCY = 100;
6 localparam DP_AXI_DATA_WIDTH = 32;
7 localparam DP_AXI_ADDR_WIDTH = 32;
8 localparam DP_TX_AXIL_BASE_ADDRESS = 32'h0;
9 localparam DP_RX_AXIL_BASE_ADDRESS = 32'h30000;
10 //localparam FAMILY = "LFCPNX";
11 localparam DP_TX_COUNT_1MS = 32'h000003E8;
12 localparam DP_TX_FIFO_IMPL = "EBR";
13 localparam DP_TX_FRAME_COUNT = 0;
14 localparam DP_TX_VIDEO_INTERFACE = 0;
```

Figure 5.10. Commenting FAMILY Parameter

When VS_ATTACH is set to 0, the testbench runs at whatever input resolution is entered into the Video Scaler IP GUI shown in Figure 5.5.

5.2. Running Functional Simulation

To run the functional simulation after the IP is generated, follow the steps:

1. Click the  button located on the toolbar to initiate the **Simulation Wizard** on the top of the Lattice radiant software as shown in [Figure 5.11](#).

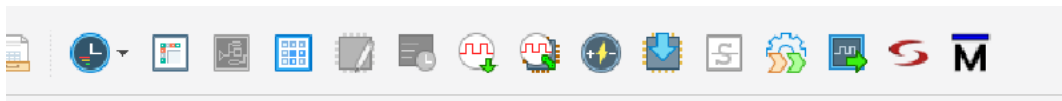


Figure 5.11. Simulation Button Icon

2. Enter the project name in the simulation wizard and click on the **Next** button as shown in [Figure 5.12](#).

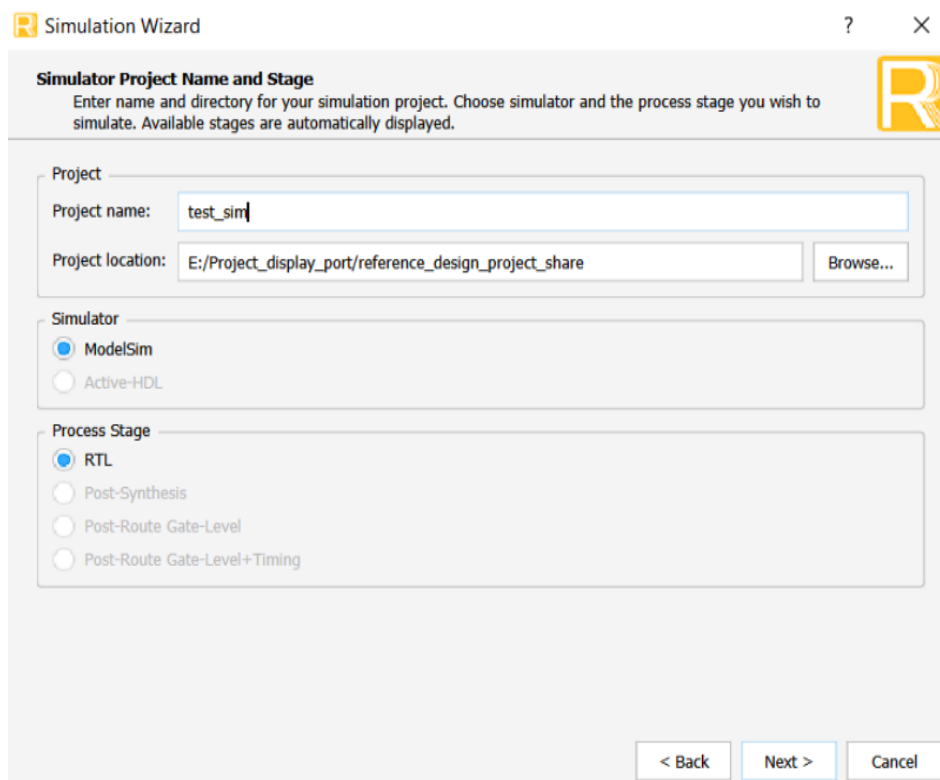


Figure 5.12. Simulation Wizard - I

- A simulation wizard dialog box appears as shown in [Figure 5.13](#). Click on **Yes** button and then click on **Next** subsequently.

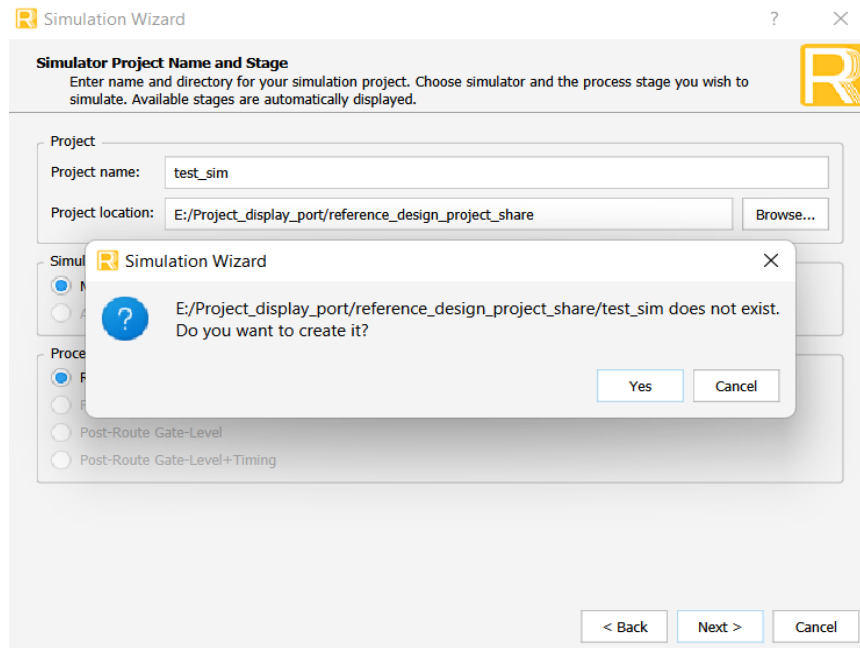


Figure 5.13. Simulation Wizard - II

- Change the simulation time to **0 ns** to run all the simulation as shown in [Figure 5.14](#). Click **Finish** to run the simulation.

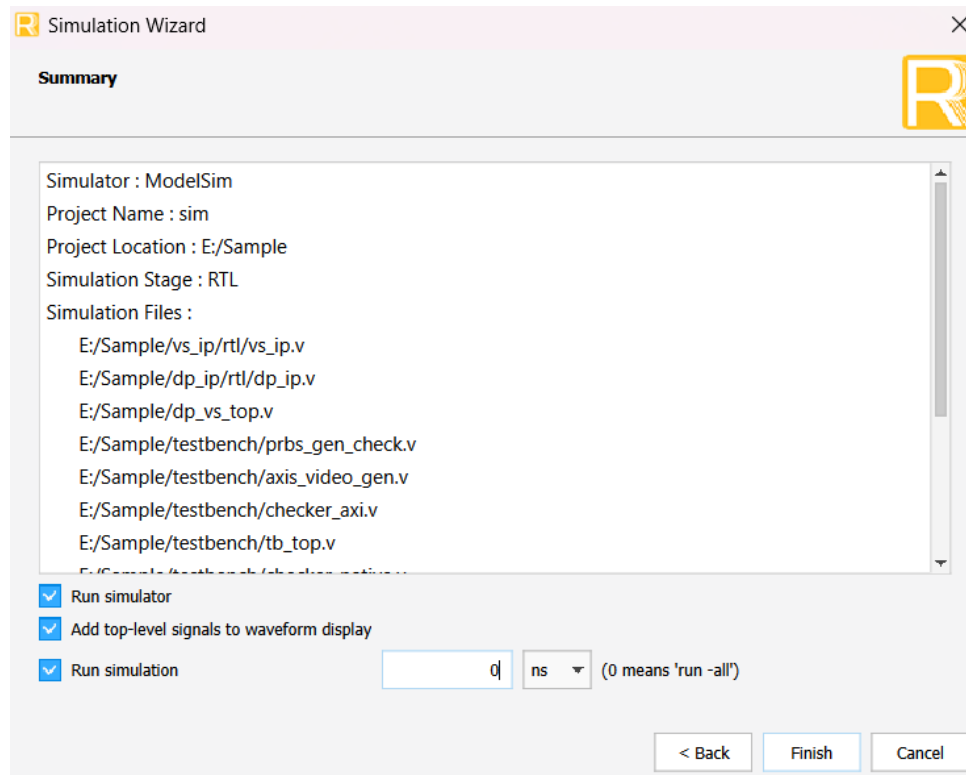


Figure 5.14. Run Simulation value of 0 for Run all

5. The Simulation is opened as shown in Figure 5.15.

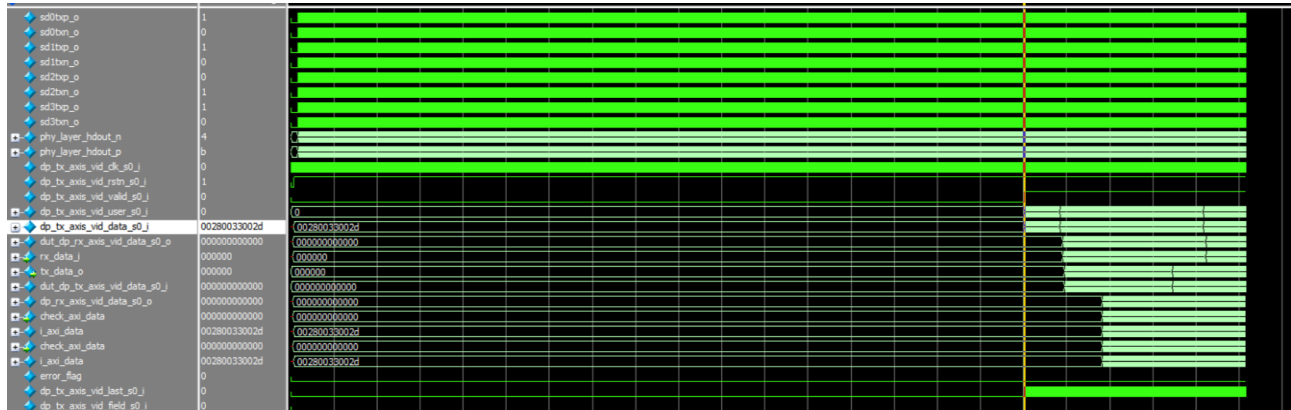


Figure 5.15. Sample Simulation Waveform

Note: Test bench also includes a data comparator/checker. The data check completed indicates the correctness of the test.

6. In the transcript, the simulation result is printed as shown in Figure 5.16.

```
# 3158063000000 INFO:=====TRAINING OF FIRST LINK IS COMPLETED=====
# 3158063000000 INFO:=====TRAINING OF SECOND LINK IS COMPLETED=====
# 3401875000000 INFO:=====DATA BEING GENERATED FROM DP1 TRANSMITTER=====
# 3580000000000 INFO:=====DATA BEING CAPTURED AT DP2 RECEIVER=====
# 3580000000000 INFO:=====DATA BEING GENERATED FROM DP2 TRANSMITTER=====
# 3764863000000 INFO:=====DATA BEING CAPTURED AT DP2 RECEIVER=====
# 4431063000000 INFO: tb_top.report_status: SIMULATION STATUS: PASS
# ***** SIMULATION PASSED *****
#
```

Figure 5.16. Simulation Result in Console

References

For more information, refer to:

- [Lattice Radiant Software 3.1 User Guide](#)
- [Video Scaler IP User Guide \(FPGA-IPUG-02234\)](#)
- [DisplayPort IP User Guide \(FPGA-IPUG-02236\)](#)
- [DisplayPort and Video Scaler Demonstration User Guide \(FPGA-UG-02201\)](#)
- [CertusPro-NX](#) web page
- [Lattice Radiant Software](#) web page
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.2, January 2024

Section	Change Summary
All	- Made editorial fixes. - Minor adjustments to ensure that the document is consistent with Lattice Semiconductor's inclusive language policy.
Inclusive Language	Added boilerplate.
Functional Description	- Added reference to <i>Video Scaler IP User Guide (FPGA-IPUG-02234)</i> document in the AXI-Stream Data Generator section. - Added references to <i>Video Scaler IP User Guide (FPGA-IPUG-02234)</i>, and <i>DisplayPort IP User Guide (FPGA-IPUG-02236)</i> documents in the DP_VS_TOP section.
Opening and Running the Project	- Updated Figure 5.4. Module/IP Block Wizard for dp_ip, Figure 5.5. Module/IP Block Wizard for vs_ip, and Figure 5.6. Video Scaler IP GUI screen for 720p to 1080p and PARTIAL_RESOLUTION=5. - Added Figure 5.7. Video Scaler IP Implementation tab for 720p to 1080p and PARTIAL_RESOLUTION=5 and updated sequence of the following figures accordingly.
References	- Added references to <i>Lattice Radiant Software 3.1 User Guide</i> document. - Replaced the reference to <i>DisplayPort and Video Scaler Demo User Guide (FPGA-UG-02191)</i> with <i>DisplayPort and Video Scaler Demonstration User Guide (FPGA-UG-02201)</i>. - Removed the reference to <i>DisplayPort and Video Scaler Reference Design (FPGA-RD-02276)</i>.

Revision 1.1, December 2023

Section	Change Summary
Disclaimers	Added new disclaimers.
Functional Description	Updated the title of Figure 2.1. DP Video Scaler Reference Design with Testbench.
Signal Description	Updated Table 3.1. Primary I/O.
Opening and Running the Project	- Updated the note in the description of this section. - Corrected the titles of Figure 5.4. Module/IP Block Wizard for dp_ip, Figure 5.5. Module/IP Block Wizard for vs_ip, and Figure 5.16. Simulation Result in Console.
References	Added link to Lattice Insights webpage.

Revision 1.0, August 2023

Section	Change Summary
All	Initial release.



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