# Lattice 5G ORAN Solution Stack 1.1 : Secure IEEE 1588 Precision Timing Protocol (PTP)

## Reference Design

FPGA-RD-02273-1.1

August 2023

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# Acronyms in This Document

A list of acronyms used in this document.

| Acronym | Definition |
|---|---|
| AEAD | Authenticated Encryption with Associated Data |
| AES | Advanced Encryption Standard |
| AHBL | Advanced High-performance Bus-Lite |
| APB | Advanced Peripheral Bus |
| AXI | Advanced eXtensible Interface |
| BC | Boundary Clock |
| CDF | Cumulative Distribution Function |
| CF | Correction Factor |
| CPU | Central Processing Unit |
| DMA | Direct Memory Access |
| ECC | Elliptical Curve Cryptography |
| FIFO | First-In-First-Out |
| FMC | FPGA Mezzanine Card |
| FTDI | Future Technology Devices International |
| GM | Grand Master Clock |
| GNSS | Global Navigation Satellite System |
| HMAC | Hash Message Authentication Code |
| HPC | High Pin Count |
| ICV | Integrity Check Value |
| IRQ | Interrupt Request |
| OCXO | Oven Controlled Crystal Oscillator |
| ORAN | Open Radio Access Network |
| OC | Ordinary Clock |
| OSE | ORAN Security Enclave |
| PCIe | Peripheral Component Interconnect Express |
| PDF | Probability Density Function |
| PKC | Public Key Cryptography |
| PTP | Precision Time Protocol |
| RISC-V | Reduced Instruction Set Computer-V |
| RSA | Rivest–Shamir–Adleman |
| RTL | Register-Transfer Level |
| SHA384 | Secure Hash Algorithm 384 |
| SMBus | System Management Bus |
| TC | Transparent Clock |
| TLV | Type Length Value |
| TSN | Time Sensitive Network |
| UART | Universal Asynchronous Receiver-Transmitter |

# 1. Introduction

This user guide provides instructions for using the Lattice ORAN™ Solution Stack 1.1 – Secure IEEE 1588 Software. The evaluation kit consists of two boards: the 1588PTP Mother Board and the 1588PTP Daughter Board. The 1588PTP Mother Board features the CertusPro™-NX FPGA, which is built on the Lattice Nexus FPGA platform using low power 28 nm FD-SOI technology.

## 1.1. Learning Objectives

By following the steps in this guide, the user will be able to:

- Set up the IEEE 1588 evaluation kit.
- Install and run the IEEE 1588 PTP solution stack application (user interface) to configure and monitor clocks.
- Get the graphical plots (including CDF, PDF) for the synchronization parameters.
- Understand and complete a sample IEEE 1588 PTP setup.

# 2. Hardware and Software Requirements

## 2.1. Hardware Requirements

- Lattice IEEE 1588
  - 1588PTP Mother Board
  - 1588PTP Daughter Board
- PC with Core-i3 fifth generation CPU or higher with Virtualization ON (if supported)
- Motherboard with PCIe-×16, ×8 or ×4 slot supporting Gen2 or above
- 4 GB RAM or higher
- 120 GB ROM or higher.
- Secure boot: Disabled (if available).
- Mini-USB to USB-A cable to program the FPGA
- Two fiber optic cables (3 meters each) to connect the PTP nodes over 10 G Ethernet

## 2.2. Software Requirements

- Operating System: Ubuntu 20.04 LTS (recommended)
- Lattice ORAN 1588 solution stack installer that includes:
  - Kernel modules
  - Daemon application and services
  - Lattice ORAN solution stack application
- Wireshark application
- Lattice Radiant™ software version 2.2 or later to program the FPGAs
- FPGA bit file for the 1588PTP Mother Board (*Lattice_PTP_CC_Demo.bit*)

# 3. Hardware Features and Setup

## 3.1. 1588PTP Mother Board

This section covers the features of the 1588PTP Mother Board and the steps in loading the demo bit file to the SPI flash that is connected to the CertusPro-NX FPGA. On subsequent power up, the 1588PTP Mother Board is configured with the loaded bit file through the MSPI configuration interface.

### 3.1.1. Features

The 1588PTP Mother Board includes the following features:

- CertusPro-NX FPGA (LFCPNX-100-9LFG672I)
- PCIe ×4 Gen3 support
  - Endpoint configuration
  - Root port configuration
- 2× SFP 1 G Ethernet
- 2× SFP 10 G Ethernet
- 2× SerDes channels extended to BOARD TO BOARD connector
- On-board Boot Flash - 512 Mb Serial Peripheral Interface (SPI) Flash, with Quad read feature
- USB-B connection for device programming. UART and Inter-Integrated Circuit Bus ($I^2C$) utility are also available on the same port.
- 7 Segment Display, five-input DIP switch, 8 status LEDs for customer purposes
- Lattice Radiant software programming support

**Caution:** The Lattice 1588PTP Mother Board contains ESD-sensitive components. ESD safe practices should be followed while handling and using the board.

### 3.1.2. Jumper Configuration

Install the jumpers listed in Table 3.1. If this is the first time the board is used, the jumpers should be in the indicated configuration.

**Table 3.1. Jumper Configuration**

| Jumper | Description | Settings |
|---|---|---|
| J5 | FTDI- UART or $I^2C$ selection | Default 1–2 UART, Short 2-3 for $I^2C$ |
| J7 | FTDI- UART or $I^2C$ selection | Default 1–2 UART, Short 2-3 for $I^2C$ |
| J14 | $V_{CCIO}$ selection for Bank 0 | Default short 1-2 for VCCIO=3.3 V, short 2-3 for VCCIO=1.8 V |
| J19 | PCIe link selection | Default Short 2-4 for PCIe X4, Short 1-2 for PCIe X1 |

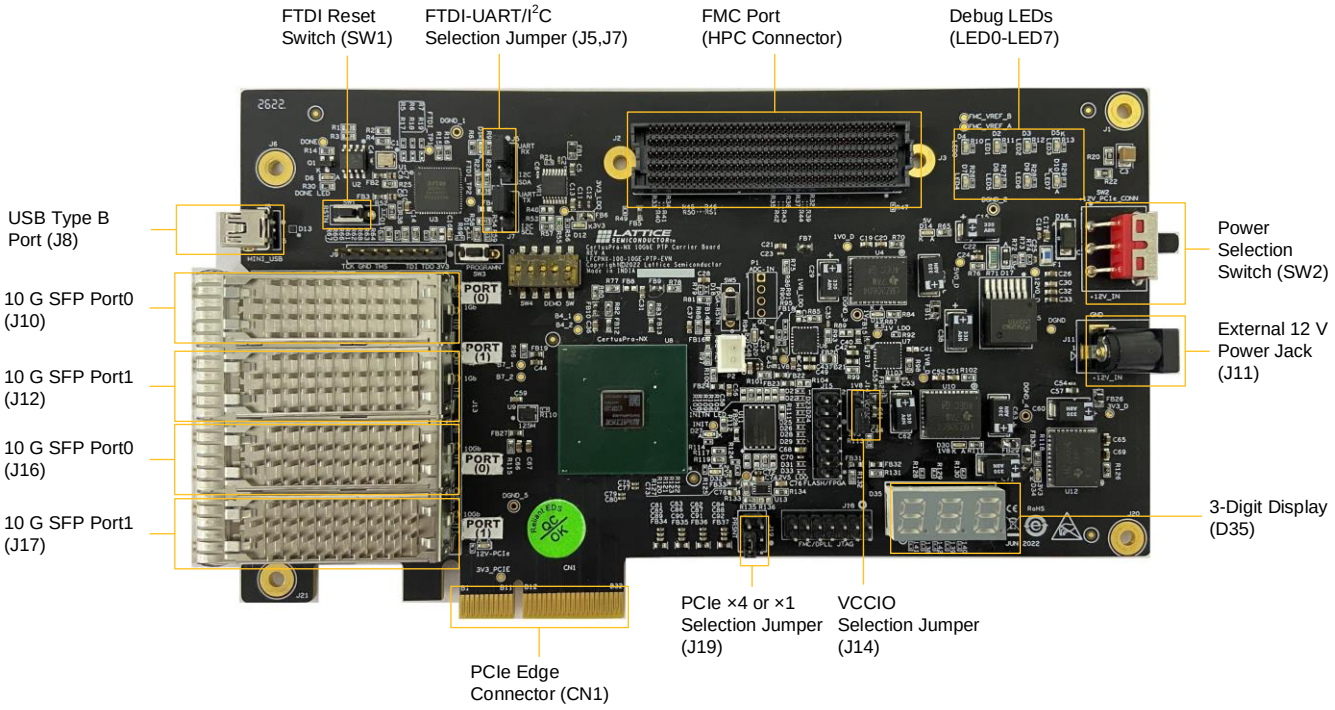


**Figure 3.1. 1588PTP Mother Board Jumper Location**

### 3.1.3. Powering up the 1588PTP Mother Board

For the kit setup, the 1588PTP Mother Board draws power from the PC through the PCIe port.

To power up the 1588PTP Mother Board:

1. Ensure that the power selection switch (SW2) is in the 12V_PCIe_CONN position to receive power from the PCIe port.
2. Connect the 1588PTP Mother Board to the PC through the PCIe port.
3. Verify that power is received through the D36 LED (12V_IN_PCIE), which lights up in green.

**Notes:**

Alternatively, for testing or programming purposes, use an external 12 V adapter to power the 1588PTP Mother Board. In this case, ensure that SW2 is in the 12V_IN position to receive power from the external 12 V adapter.

To program the FPGA/SPI flash, the board is connected to the PC running the Lattice Radiant software using the Mini USB Type-A Cable. See the Programming the FPGA section.

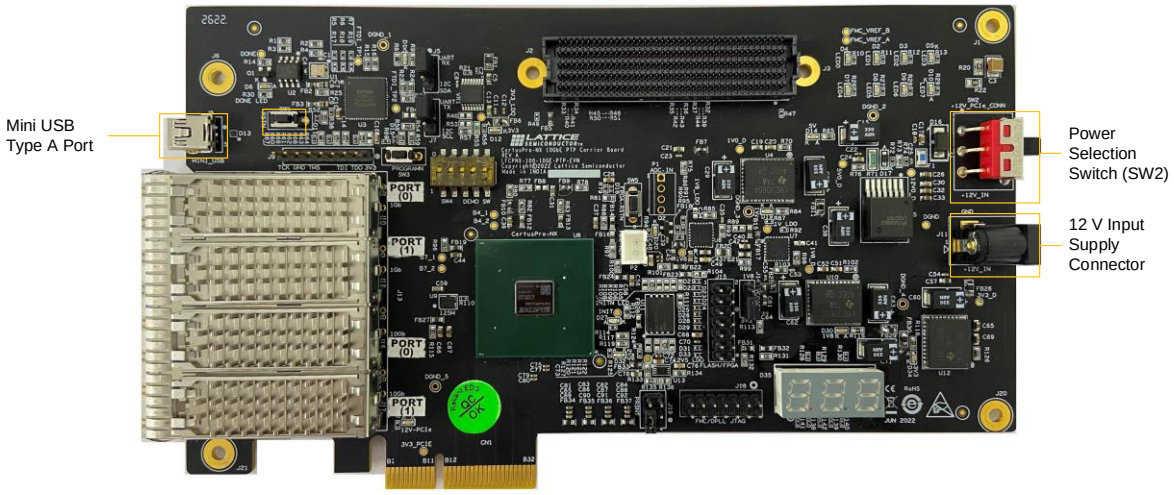


**Figure 3.2. Lattice 1588PTP Mother Board Connection**

## 3.1.4. Control Buses – I²C, UART, and SPI

This section describes the topology of the various configuration and communication buses.

### 3.1.4.1. I²C Topology

This I²C bus has the signal names FTDI_I2C_SCL and FTDI_I2C_SDA. When the jumpers (J5, J7) are closed on pins 2-3, the I²C bus is connected to a dedicated CertusPro-NX GPIO bank 1. I²C and UART share the same output port B on FTDI chip. The I²C connections are summarized in Table 3.2.

**Table 3.2. I²C Bus Connection**

| Signal Name | CertusPro-NX Ball Location | FTDI Chip Ball Location | Jumper |
|---|---|---|---|
| FTDI_I2C_SCL | M7 | 38 | J7 |
| FTDI_I2C_SDA | M6 | 39&40 | J5 |

### 3.1.4.2. UART Topology

The board provides one UART communication interface by providing a flexible connection between the CertusPro-NX device and FTDI chip. Close the two jumpers, J32 and J33, to connect to two general-purpose I/O in Bank 1, as shown in Table 3.3. This UART is alternative to I²C bus by setting FTDI configuration.

**Table 3.3. UART Bus Connection**

| Signal Name | CertusPro-NX Ball Location | FTDI Chip Ball Location | Jumper |
|---|---|---|---|
| FTDI_UART_TXD | L8 | 38 | J7 |
| FTDI_UART_RXD | M9 | 39 | J5 |

#### 3.1.4.3. SPI Topology

One of the major functions of SPI connections on the board is to support CertusPro-NX configuration from the SPI Flash or the Parallel Configuration Header (J15), as shown in Table 3.4. Lattice 1588PTP Mother Board can support both Master SPI (MSPI) and Slave SPI (SSPI) modes for CertusPro-NX configuration.

**Table 3.4. SPI Bus Connections**

| Signal Name | CertusPro-NX Ball | Parallel Configuration Header Pin |
|---|---|---|
| CONN_FLASH_MCLK | G6 | 12 |
| CONN_FLASH _MOSI | H7 | 5 |
| CONN_FLASH _MISO | H6 | 7 |
| CONN_FLASH_CS# | G7 | 2 |
| CONN_FLASH_DQ2 | K5 | 11 |
| CONN_FLASH_DQ3 | H4 | 9 |
| MCSNO | H3 | 3 |
| CONN_PROGRAMN | G4 | 1* |
| DONE | G5 | 4* |
| CONN_INITN | G2 | 6* |

**Note:**

1. These connections are possible if 0 Ω resistors are installed.

## 3.1.5. LEDs and Switches

This section describes the 1588PTP Mother Board LEDs and switches.

### 3.1.5.1. General Purpose LEDs

The Lattice 1588PTP Mother Board provides eight LEDs that are connected to I/O within Bank 1. The LEDs are lighted with green color when the output is driven HIGH. The designated pins are connected as shown in Table 3.5.

**Table 3.5. General Purpose LED Signals**

| Signal Name | CertusPro-NX Ball Location | CertusPro-NX Bank/Color | LED Reference |
|---|---|---|---|
| LED0 | R5 | 1/Green | D4 |
| LED1 | R4 | 1/Green | D2 |
| LED2 | R8 | 1/Green | D3 |
| LED3 | R9 | 1/Green | D5 |
| LED4 | U8 | 1/Green | D7 |
| LED5 | R7 | 1/Green | D8 |
| LED6 | R6 | 1/Green | D9 |
| LED7 | P8 | 1/Green | D10 |

### 3.1.5.2. Seven Segment LED

The Lattice 1588PTP Mother Board provides eight LEDs that are connected to I/O within Bank 1. The LEDs are lighted with green color when the output is driven HIGH.

**Table 3.6. 7-Segment LED Signals**

| Signal Name | CertusPro-NX Ball Location |
|---|---|
| SEG_A | M4 |
| SEG_B | M3 |
| SEG_C | M2 |
| SEG_D | M1 |
| SEG_E | N1 |
| SEG_F | N2 |
| SEG_G | N3 |
| SEG_DP | N4 |
| F_K_DIG1 | L6 |
| F_K_DIG2 | L3 |
| F_K_DIG3 | L2 |

### 3.1.5.3. DIP Switch

Five CertusPro-NX pins are connected to the DIP switch (SW1) to allow manual actuating input to the FPGA. One side of each switch is connected to GPIOs within Bank 5 and is pulled up through 4.7 kΩ resistors. The other side is grounded. The designated pins are connected as shown in Table 3.7.

**Table 3.7. DIP Switch Signals**

| Signal Name | CertusPro-NX Ball Location | CertusPro-NX Bank |
|---|---|---|
| SWITCH1 | AA23 | 5 |
| SWITCH2 | AB22 | 5 |
| SWITCH3 | AC22 | 5 |
| SWITCH4 | AA22 | 5 |
| SWITCH5 | W21 | 5 |

#### 3.1.5.4. Push Buttons

The Lattice 1588PTP Mother Board provides four push button switches, SW2, SW3, SW7, for demo and user applications. One of the buttons is pre-defined functional pin, and the other three are generic pins. Pressing these buttons drive a logic level "0" to the corresponding I/O pins. The designated pins are connected as shown in Table 3.8.

**Table 3.8. Push Buttons Switch Signals**

| Signal Name | CertusPro-NX Ball Location | Push Button Reference | Logic Level at Button Pressed |
|---|---|---|---|
| PROGRAMN | G4 | SW3 | 0 |
| F_RESET_N | N9 | SW5 | 0 |
| FTDI_RESET | — | SW1 | 0 |

### 3.1.6. Headers/Connectors

This section describes Lattice 1588PTP Mother Board headers/connectors and pin mapping.

#### 3.1.6.1. External Flash Configuration Header

**Table 3.9. SPI Flash Configuration Header Pin Connections**

| J15 Pin Number | Signal Name | CertusPro-NX Ball Location |
|---|---|---|
| 1 | CONN_PROGRAMN | G4* |
| 2 | CONN_FLASH_CS# | — |
| 3 | MCSNO | H3 |
| 4 | DONE | G5 |
| 5 | CONN_FLASH_DQ0 | H7* |
| 6 | CONN_INITN | G2* |
| 7 | CONN_FLASH_DQ1 | H6* |
| 8 | — | — |
| 9 | CONN_FLASH_DQ3 | H4* |
| 10 | VCCIO0 | — |
| 11 | CONN_FLASH_DQ2 | K5* |
| 12 | CONN_FLASH_MCLK | G6* |
| 13 | GND | — |
| 14 | GND | — |

**Note:**

1. These connections are possible if 0 Ω resistors are installed.

#### 3.1.6.2. ADC Test Header

The 1588PTP Mother Board has onboard header connectors to feed in ADC input signals to the Certus Pro-NX FPGA.

**Table 3.10. ADC Test Header Pin Details – P1**

| P1 Pin Number | Signal Name | CertusPro-NX Ball Location |
|---|---|---|
| 1 | AF2 | AF2 |
| 2 | AE2 | AE2 |
| 3 | AE1 | AE1 |
| 4 | AD1 | AD1 |

**Table 3.11. ADC Test Header Pin Details – P2**

| P2 Pin Number | Signal Name | CertusPro-NX Ball Location |
|---|---|---|
| 1 | AC1 | AF2 |
| 2 | AC2 | AE2 |

#### 3.1.6.3. SFP Connectors

**Table 3.12. SFP Connector Pin Details – 1 G Ethernet – 1**

| J12 Pin Number | Signal Name | CertusPro-NX Ball Location |
|---|---|---|
| 1 | GND | — |
| 2 | F_SFP3_TX_FAULT | T20 |
| 3 | F_SFP3_TX_DISABLE | T19 |
| 4 | F_SFP3_I2C_SDA | T18 |
| 5 | F_SFP3_I2C_SCL | U19 |
| 6 | F_SFP3_ABS | U22 |
| 7 | 3V3_OUT | — |
| 8 | F_SFP3_LOS | U18 |
| 9 | 3V3_OUT | — |
| 10 | GND | — |
| 11 | GND | — |
| 12 | F_SFP3_RX_N | V25 |
| 13 | F_SFP3_RX_P | V24 |
| 14 | GND | — |
| 15 | 3V3_OUT | — |
| 16 | 3V3_OUT | — |
| 17 | GND | — |
| 18 | F_SFP3_TX_P | U26 |
| 19 | F_SFP3_TX_N | V26 |
| 20 | GND | — |

**Table 3.13. SFP Connector Pin Details – 1 G Ethernet – 2**

| J10 Pin Number | Signal Name | CertusPro-NX Ball Location |
|---|---|---|
| 1 | GND | — |
| 2 | F_SFP4_TX_FAULT | U24 |
| 3 | F_SFP4_TX_DISABLE | U25 |
| 4 | F_SFP4_I2C_SDA | V18 |
| 5 | F_SFP4_I2C_SCL | V19 |
| 6 | F_SFP4_ABS | V21 |
| 7 | 3V3_OUT | — |
| 8 | F_SFP4_LOS | V20 |
| 9 | 3V3_OUT | — |
| 10 | GND | — |
| 11 | GND | — |
| 12 | F_SFP4_RX_N | V22 |
| 13 | F_SFP4_RX_P | V23 |
| 14 | GND | — |
| 15 | 3V3_OUT | — |
| 16 | 3V3_OUT | — |
| 17 | GND | — |
| 18 | F_SFP4_TX_P | AE24 |
| 19 | F_SFP4_TX_N | AF24 |
| 20 | GND | — |

**Table 3.14. SFP Connector Pin Details – 10 G Ethernet – 1**

| J16 Pin Number | Signal Name | CertusPro-NX Ball Location |
|---|---|---|
| 1 | GND | — |
| 2 | F_SFP1_TX_FAULT | P26 |
| 3 | F_SFP1_TX_DISABLE | P25 |
| 4 | F_SFP1_I2C_SDA | P23 |
| 5 | F_SFP1_I2C_SCL | P22 |
| 6 | F_SFP1_ABS | P21 |
| 7 | 3V3_OUT | — |
| 8 | F_SFP1_LOS | R20 |
| 9 | 3V3_OUT | — |
| 10 | GND | — |
| 11 | GND | — |
| 12 | F_SFP1_RX_N | B13 |
| 13 | F_SFP1_RX_P | C12 |
| 14 | GND | — |
| 15 | 3V3_OUT | — |
| 16 | 3V3_OUT | — |
| 17 | GND | — |
| 18 | F_SFP1_TX_P | A12 |
| 19 | F_SFP1_TX_N | A11 |
| 20 | GND | — |

**Table 3.15. SFP Connector Pin Details – 10 G Ethernet – 2**

| J17 Pin Number | Signal Name | CertusPro-NX Ball Location |
|---|---|---|
| 1 | GND | — |
| 2 | F_SFP2_TX_FAULT | R21 |
| 3 | F_SFP2_TX_DISABLE | R19 |
| 4 | F_SFP2_I2C_SDA | R18 |
| 5 | F_SFP2_I2C_SCL | R22 |
| 6 | F_SFP2_ABS | T22 |
| 7 | 3V3_OUT | — |
| 8 | F_SFP2_LOS | R25 |
| 9 | 3V3_OUT | — |
| 10 | GND | — |
| 11 | GND | — |
| 12 | F_SFP2_RX_N | B10 |
| 13 | F_SFP2_RX_P | C10 |
| 14 | GND | — |
| 15 | 3V3_OUT | — |
| 16 | 3V3_OUT | — |
| 17 | GND | — |
| 18 | F_SFP2_TX_P | A9 |
| 19 | F_SFP2_TX_N | A8 |
| 20 | GND | — |

### 3.1.6.4. PCIe Edge Connectors

**Table 3.16. PCIe Edge Connector Pin Details**

| CN1 Pin Name | Signal Name | CertusPro-NX Ball | CN1 Pin Name | Signal Name | CertusPro-NX Ball |
|---|---|---|---|---|---|
| A1 | PCIe_EC_PRSNT#1 | — | B1 | 12V_IN_PCIE | — |
| A2 | 12V_IN_PCIE | — | B2 | 12V_IN_PCIE | — |
| A3 | 12V_IN_PCIE | — | B3 | 12V_IN_PCIE | — |
| A4 | GND | — | B4 | GND | — |
| A5 | No Connection | — | B5 | No Connection | T8 |
| A6 | No Connection | — | B6 | No Connection | T7 |
| A7 | No Connection | — | B7 | GND | — |
| A8 | No Connection | — | B8 | 3V3_PCIe | — |
| A9 | 3V3_PCIe | — | B9 | No Connection | P9 |
| A10 | 3V3_PCIe | — | B10 | No Connection | — |
| A11 | F_PCIe_EC_PRSNT | R26 | B11 | No Connection | P19 |
| A12 | GND | — | B12 | No Connection | — |
| A13 | F_PCIe_EC_100MHz_CLK_P | F20[1] | B13 | GND | — |
| A14 | F_PCIe_EC_100MHz_CLK_N | E20[1] | B14 | EP_PCIe_RXD0_P | G24[1] |
| A15 | GND | — | B15 | EP_PCIe_RXD0_N | G25[1] |
| A16 | EP_PCIe_TXD0_P | F26[1] | B16 | GND | — |
| A17 | EP_PCIe_TXD0_N | E26[1] | B17 | PCIe_EC_PRSNT#2 | — |
| A18 | GND | — | B18 | GND | — |
| A19 | No Connection | — | B19 | EP_PCIe_RXD1_P | E24[1] |
| A20 | GND | — | B20 | EP_PCIe_RXD1_N | D25[1] |
| A21 | EP_PCIe_TXD1_P | C26[1] | B21 | GND | — |
| A22 | EP_PCIe_TXD1_N | B26[1] | B22 | GND | — |
| A23 | GND | — | B23 | EP_PCIe_RXD2_P | C24[1] |
| A24 | GND | — | B24 | EP_PCIe_RXD2_N | B23[1] |
| A25 | EP_PCIe_TXD2_P | A25[1] | B25 | GND | — |
| A26 | EP_PCIe_TXD2_N | A24[1] | B26 | GND | — |
| A27 | GND | — | B27 | EP_PCIe_RXD3_P | C21[1] |
| A28 | GND | — | B28 | EP_PCIe_RXD3_N | C22[1] |
| A29 | EP_PCIe_TXD3_P | A22[1] | B29 | GND | — |
| A30 | EP_PCIe_TXD3_N | A21[1] | B30 | No Connection | — |
| A31 | GND | — | B31 | PCIe_EC_PRSNT#2 | — |
| A32 | No Connection | — | B32 | GND | — |

**Note**:

1. Connects to CertusPro-NX if Endpoint PCIe is selected.

## 3.2. 1588PTP Daughter Board

This section covers the features of the 1588PTP Daughter Board.

### 3.2.1. Features

The 1588PTP Daughter Board has the following features:

- Network clock synchronizer - DPLL (SiT95147).
- Stratum 3E OCXO (SiT5711).
- GNSS timing module (LEA-M8T-0).
- 2xRJ48 ports for ToD/pps In & Out.
- 2xSMA ports for DPLL Frequency In and Out.

**Caution:** The 1588PTP Daughter Board contains ESD-sensitive components. ESD safe practices should be followed while handling and using the development board.

### 3.2.2. Clock Sources

The 1588PTP Daughter Board has four clock sources for the DPLL. Refer to Table 3.17 and Figure 3.3 for more details regarding the clock sources.

DPLL has four input clock sources, IN0, IN1, IN2, IN3, which generates the required output clocks from one of these inputs. The circuit is designed such that the input IN0 of DPLL can be connected to either SyncE_Recovered_Clock or Freq_In (Test input clock on SMA port 17) or GNSS timepulse2 clock. All these provisions are for testing and debugging purposes.

SyncE_Recovered_Clock is a recovered clock that is recovered from either Port-0 or Port 1 as shown in Figure 3.4. Freq_In is the external input clock that can be connected to SMA port J7.

The inputs IN1 of DPLL is connected to GNSS, IN2 is connected to SyncE_Recovered_Clk1, and IN3 is connected to OCXO. IN1, IN2, IN3 are the ones that are required for PTP functionality.

**Table 3.17. Clock Sources**

| Clock Frequency | Signal Name | Clock Sources | DPLL PIN | Type | Description |
|---|---|---|---|---|---|
| 8 kHz-10 MHz | GNSS_TIME_PULSE_2_DPLL | U1 (GNSS) | 63 | Single ended | Connected to FPGA (Optionally Connected to IN0) |
| 10 MHz | Freq_In | Test Input (SMA port J7) | 63 | Single Ended | Test Frequency input to DPLL (Connected to IN0) |
| 161.1328 MHz | FPGA_CLKOUT_10MHz_P FPGA_CLKOUT_10MHz_N | 1588PTP Mother Board | 63/64 | Differential | 10 MHZ clock output from FPGA[1] (Connected to IN0) |
| 8 kHz-10 MHz | GNSS_TIME_PULSE_1_DPLL | U1 (GNSS) | 61 | Single ended | Connected to IN1 |
| 161.1328 MHz | SyncE_Recovered_Clk_FMC_P SyncE_Recovered_Clk_FMC_N | 1588PTP Mother Board | 14/15 | Differential | SyncE recovered clock[2] (Connected to IN2) |
| 10 MHz | OCXO_DPLL_CLK_IN | U7 | 61 | Single Ended | (Connected to IN3) |

**Notes:**

1. The input clock on IN0 of DPLL can be selected through jumper J13. The default setting is FPGA_CLKOUT_10MHz_P connected as single ended clock .
2. SyncE recovered clock from Port 0 or Port 1 is routed to DPLL as SyncE_Recovered_Clk1_FMC_P/N. The selection of SyncE Master Port is through the user interface.

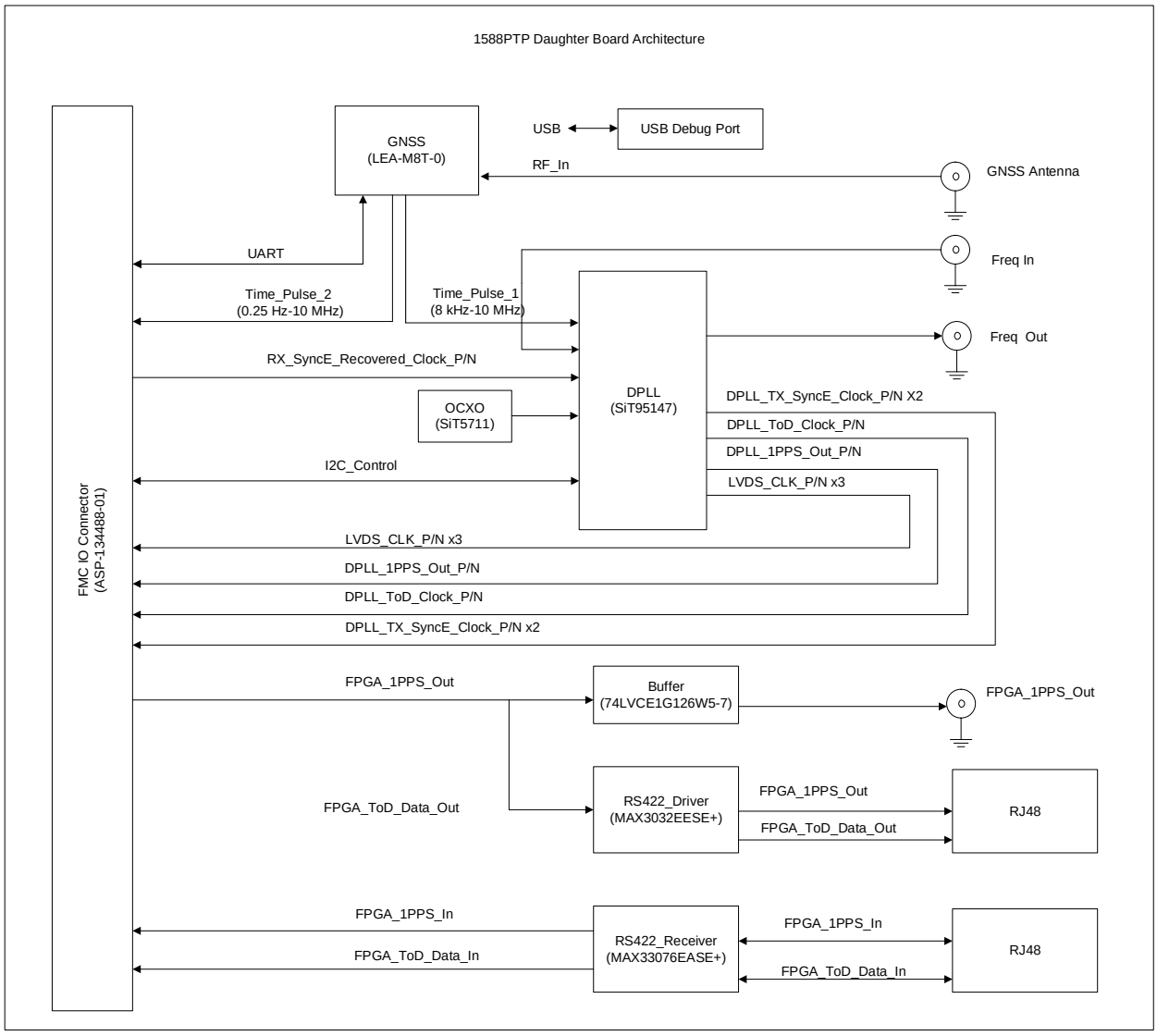


**Figure 3.3. 1588PTP Daughter Board Clock Diagram**

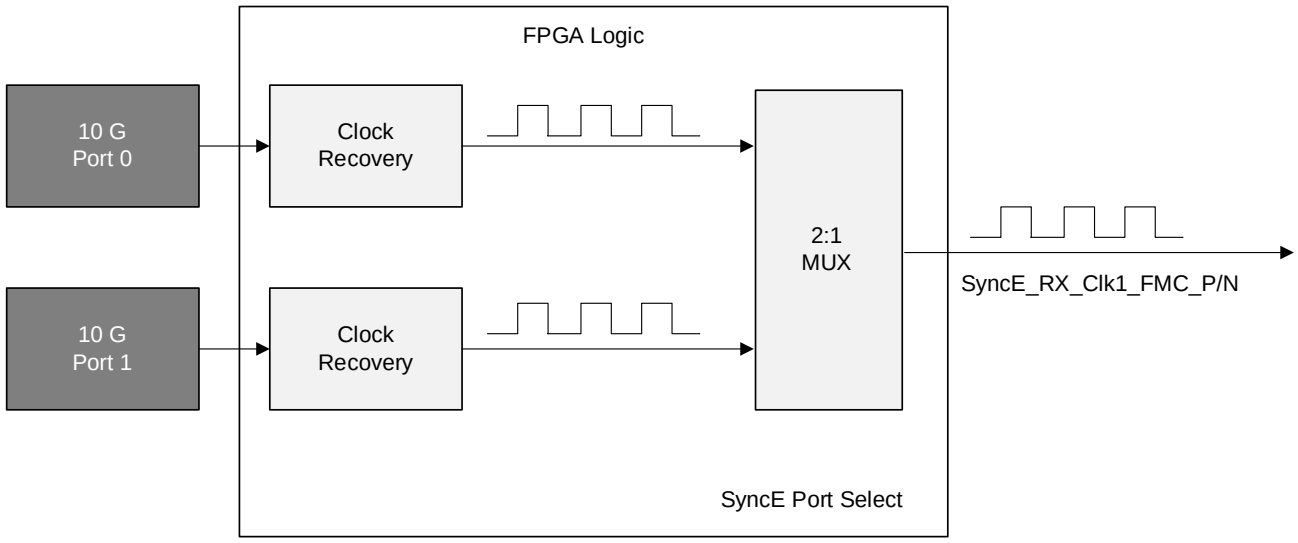


**Figure 3.4. SyncE Recovered Clock – Port 0 and Port 1**

### 3.2.3. Powering up the 1588PTP Daughter Board

Before powering up the 1588PTP Daughter Board, ensure that it is firmly plugged into the 1588PTP Mother Board. The 1588PTP Daughter Board draws power from the 1588PTP Mother Board through the FMC port.

Switch J2 on the 1588PTP Daughter Board should be set to the 12V_IN position. However, to use an external 12V adapter to power the 1588PTP Daughter Board, the switch J2 should be set to the EXT_12V position.

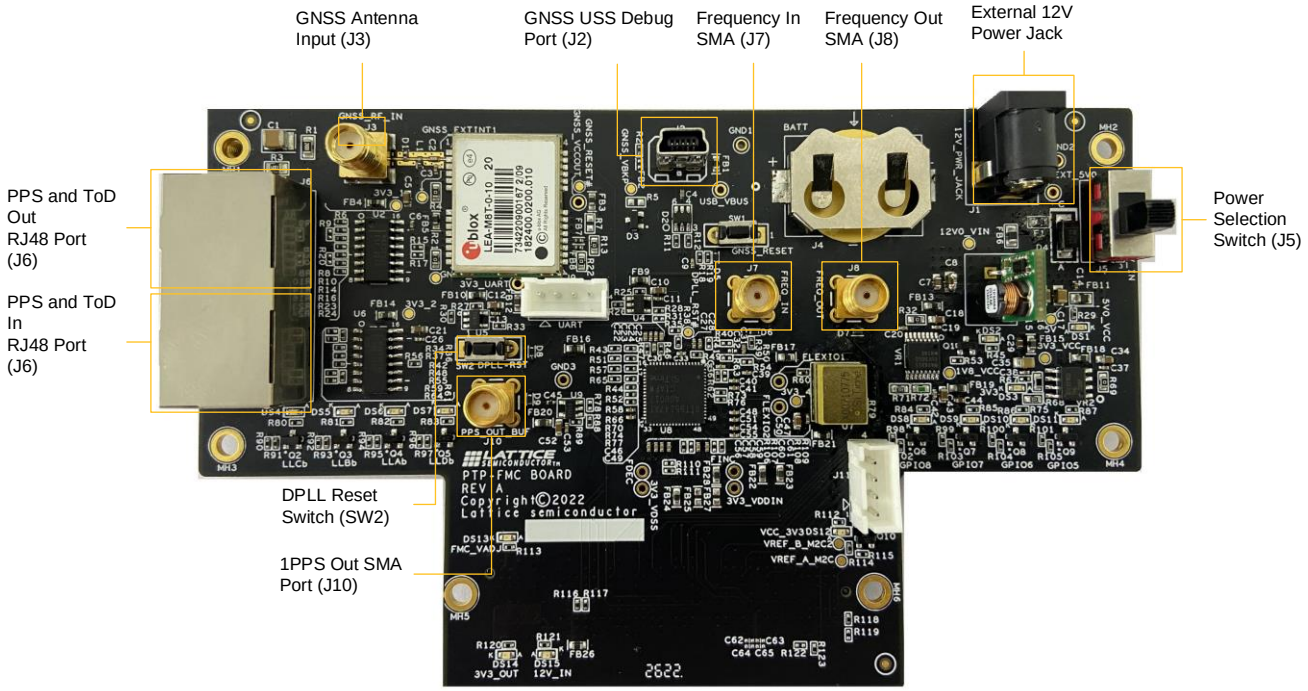


**Figure 3.5. Lattice 1588PTP Daughter Board Connection**

#### 3.2.3.1. 1588PTP Daughter Board Power Scheme

The 1588PTP Daughter Board has most of the onboard regulators powered by an external 12 V power.

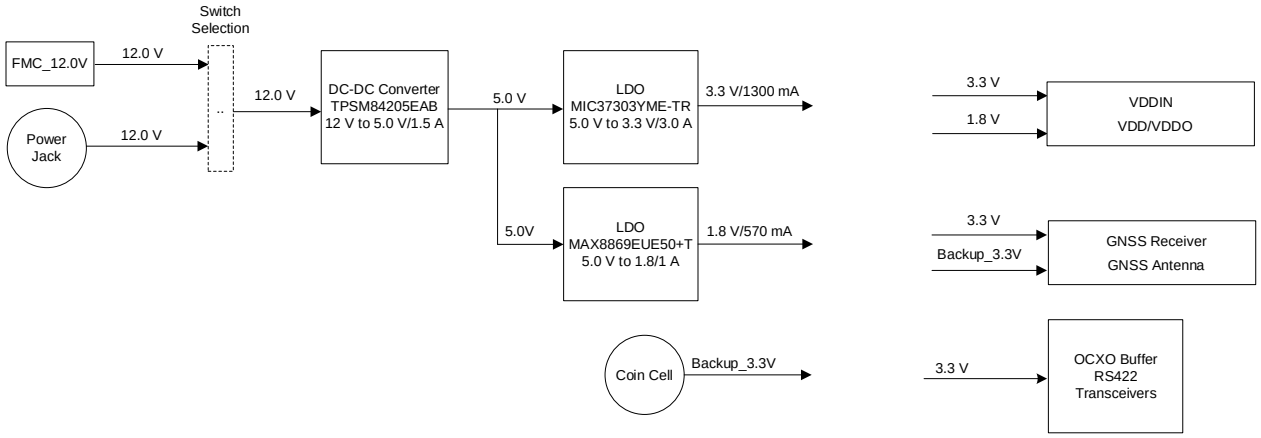


**Figure 3.6. 1588PTP Daughter Board Power Architecture**

**Table 3.18. Power Supply Options**

| Part | Supply Name | 3.3 V | 1.8 V |
|---|---|---|---|
| DPLL | VDDIN | Fixed | -- |
| — | VDD | — | Fixed |
| — | VDDS | Fixed | -- |
| — | VDDO1 | — | Fixed |
| — | VDDO2 | — | Fixed |
| — | VDDO3 | — | Fixed |
| — | VDDO5 | Selectable | Selectable |
| — | VDDO6 | — | Fixed |
| — | VDDO7 | — | Fixed |
| — | VDDO0T | — | Fixed |
| — | VDDOB | Selectable | Selectable |
| GNSS | VCC | Fixed | — |
| — | VCCBCKP | Fixed | — |
| OCXO | VCC | Fixed | — |
| Buffer | VCC | Fixed | — |
| RS422 Transceivers | VCC | Fixed | — |

## 3.2.4. LEDs and Switches

### 3.2.4.1. PLL Lock LEDs

The 1588PTP Daughter Board has four LEDS to indicate the Loss of Lock in DPLL. The details are shown in Table 3.19.

**Table 3.19. PLL Lock LED Definition**

| LED Designator | Color/Status | Signal indication |
|---|---|---|
| DS6 | Red/Loss of Lock | LLAb |
| DS5 | Red/Loss of Lock | LLBb |
| DS4 | Red/Loss of Lock | LLCb |
| DS7 | Red/Loss of Lock | LLDb |
| DS6 | Red/Loss of Lock | LLAb |

### 3.2.4.2. Power Status LEDs

The 1588PTP Daughter Board status LEDs provide a visual indication of power status as shown in Table 3.20.

**Table 3.20. Power Status LED Definition**

| LED Designator | Color | Description |
|---|---|---|
| DS1 | Green | 5V0_VCC |
| DS3 | Green | VCC_3V3 |
| DS2 | Green | VCC_1V8 |
| DS12 | Red | VCC_3V3 |
| DS15 | Green | 12V_IN |
| DS14 | Green | 3V3_OUT |
| DS13 | Green | FMC_VADJ_3V3 |

### 3.2.4.3. Push Buttons

The 1588PTP Daughter Board provides two push button switches, SW1, SW2, for reset purposes. The designated pins are connected as shown in Table 3.21.

**Table 3.21. Push Button Signal Definition**

| Signal Name | Push Button Reference | Logic Level at Button Pressed |
|---|---|---|
| GNSS_RESET_N | SW1 | 0 |
| DPLL_RST | SW2 | 0 |

## 3.2.5. Headers/Connectors

The headers and connectors of 1588PTP Daughter Board are as shown in Table 3.22.

**Table 3.22. SMA Connections**

| SMA Designator | Signal Name | Description |
|---|---|---|
| J7 | Freq_IN | Frequency input (IN0) to DPLL |
| J8 | Freq_Out | Frequency out (Out5) from DPLL |
| J3 | GNSS_RF_IN | GNSS antenna to GNSS module |
| J10 | 1PPS_Out | 1PPS output from FPGA/DPLL |

## 3.3. Assembling the 1588PTP Mother Board and 1588PTP Daughter Board

The 1588PTP Daughter Board is plugged into the 1588PTP Mother Board through the FMC connector. The receptacle J2 on the 1588PTP Mother Board and plug J12 on the 1588PTP Daughter Board are connected. Figure 3.7 shows the assembly.

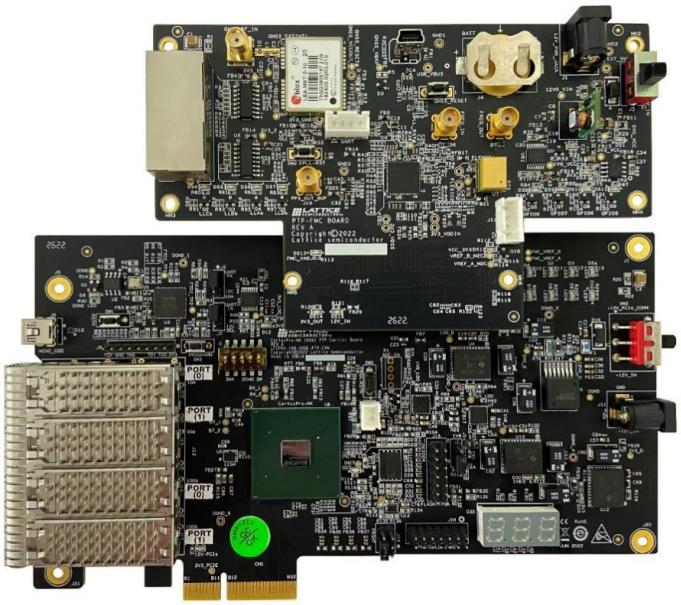

**Figure 3.7. 1588PTP Mother Board and 1588PTP Daughter Board Assembly**

The 1588PTP Mother Board can be plugged into the PCIe (×4 or ×16) of the PC through the PCIe ×4 or ×16 cable. Power ON the 1588PTP Mother Board as indicated in the Powering up the 1588PTP Mother Board section.

## 3.4. Programming the FPGA

The USB port on the 1588PTP Mother Board is used to flash the firmware to the card as shown in Figure 3.8. The 1588PTP Mother Board has a built-in download controller for programming the CertusPro-NX device. It uses an FT2232H Future Technology Devices International (FTDI) part to convert USB to JTAG. The USB is connected to PC with Lattice Radiant Programmer tool installed and the latter is used to flash and download firmware to the card.

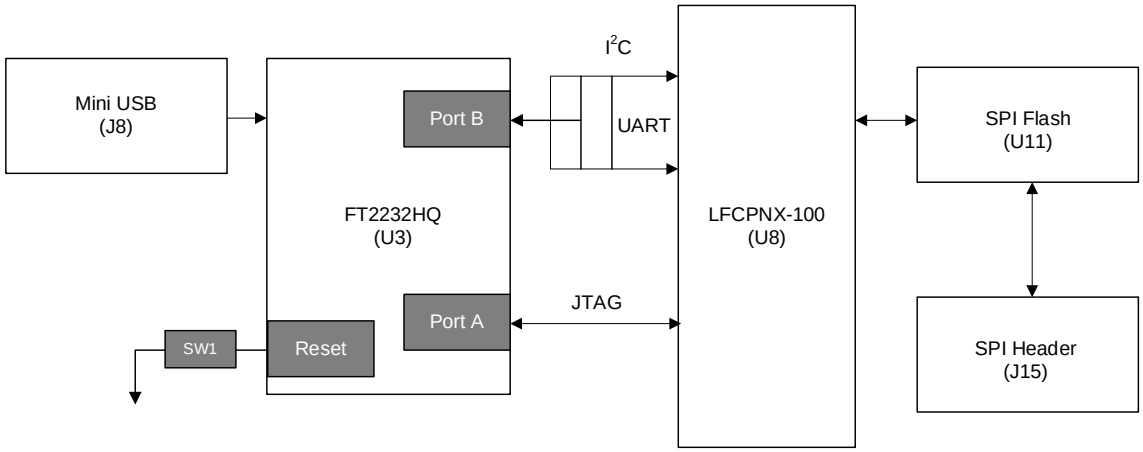


**Figure 3.8. 1588PTP Mother Board Serial Interface**

To program the CertusPro-NX FPGA device:

1. Connect the board to the PC running the Lattice Radiant software using the Mini USB Type-A cable.
2. Open the Lattice Radiant Programmer software and create a new project. In the **Getting Started** dialog box, enter the **Project Name** and **Project Location** as shown in Figure 3.9.
3. Select **Create a new project from scan** and choose the settings for the **Cable**, **Port**, and TCK Divider Setting (0-30×) fields.
4. Click **OK**.

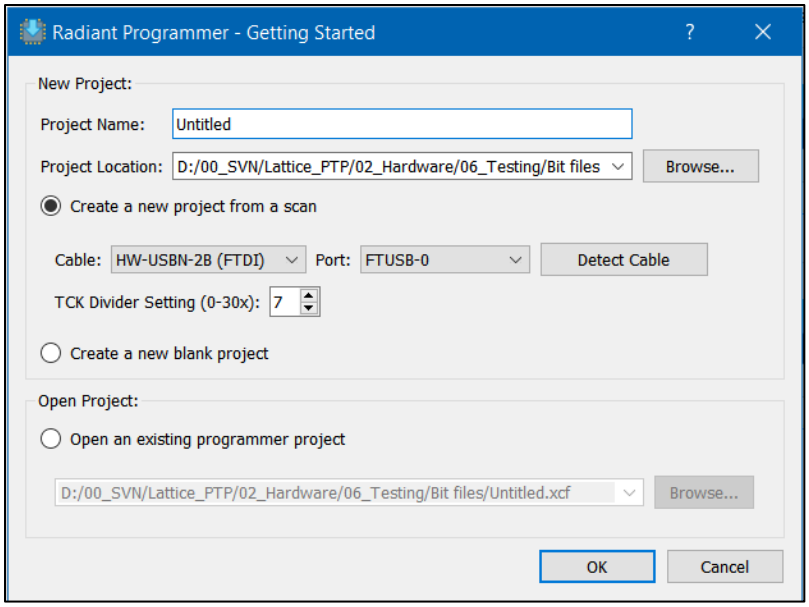


**Figure 3.9. Creating a New Project from Scan**

5. In the **Device Properties** dialog box, the **LFCPNX** (Device Family) and **LFCPNX-100** (Device) are indicated on the title bar. Select **Operation: Erase, Program** under **Device Operation** as shown in Figure 3.10.

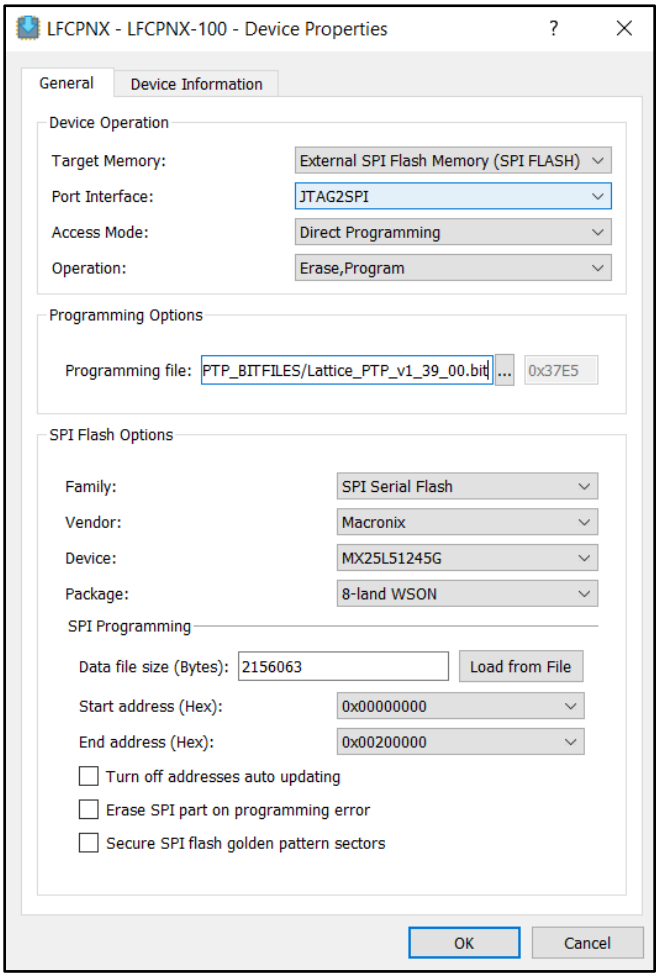


**Figure 3.10. Device Properties Window for SPI Flash Programming**

6. Select the *.bit* file in **Programming file**.
7. Click **OK**.
8. In the main interface, click the **Programming** button from the menu bar to start programming.

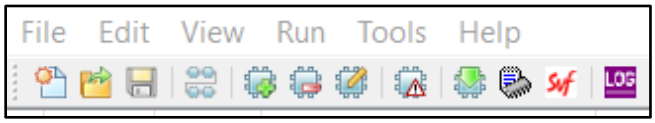


**Figure 3.11. Programmer Menu Bar**

If the FPGA programming is successful, the output console displays an *Operation Successful* message.

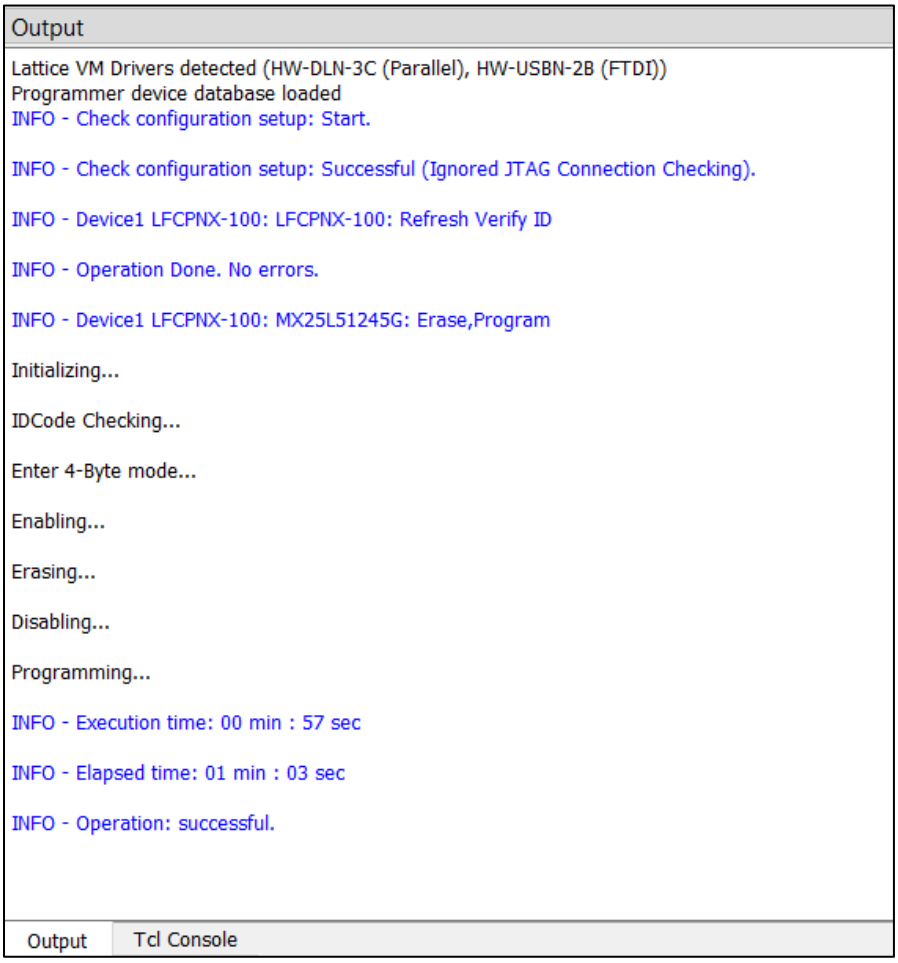


**Figure 3.12. Programmer Output Window**

If the programming operation fails, refer to the troubleshooting section of the document.

After programming, power cycle the board and check the status LEDs on the board according to Table 3.23 and Table 3.24.

### 3.4.1. Status LEDs

The description of each status LED is provided in Table 3.23 and Table 3.24.

**Table 3.23. 1588PTP Mother Board Status LED Description**

| Sl. No | LED Reference | Name | Description |
|---|---|---|---|
| 1 | D1 | FTDI_UART_RXD | Green: blinks when UART is receiving data |
| 2 | D6 | Done | Green: lights up when SPI Boot is successful |
| 3 | D12 | FMC_VADJ_3V3 | Green: lights up when 3.3 V is generated |
| 4 | D14 | 5V | Green: lights up when 5 V is generated |
| 5 | D20 | 3V3_OUT | Green: lights up when 1.8 V is generated |
| — | D27 | INITN | Red: blinks when SPI boot is happening |
| 6 | D30 | 5V | Green: lights up when 5 V is generated |
| 7 | D32 | 3V3_OUT | Green: lights up when 3.3 V is generated |
| 8 | D34 | 5V | Green: lights up when 5 V is generated |
| 9 | D36 | 12V_IN_PCIE | Green: lights up when 12 V is derived from PCIe port |

**Table 3.24. 1588PTP Daughter Board Status LED Description**

| Sl. No | LED Reference | Name | Description |
|---|---|---|---|
| 1 | DS1 | VCC_5V0 | Green: lights up when 5 V is generated |
| 2 | DS2 | VCC_1V8 | Green: lights up when 1.8 V is generated |
| 3 | DS3 | VCC_3V3 | Green: lights up when 3.3 V is generated |
| 4 | DS4 | LLCb | Red: lights up when Loss of Lock in PLL C has happened |
| 5 | DS5 | LLBb | Red: lights up when Loss of Lock in PLL C has happened |
| 6 | DS6 | LLAb | Red: lights up when Loss of Lock in PLL C has happened |
| 7 | DS7 | LLDb | Red: lights up when Loss of Lock in PLL C has happened |
| 8 | DS13 | FMC_VADJ_3V3 | Green: lights up when 3.3 V is received form 1588PTP Mother Board |
| 9 | DS14 | 3V3_OUT | Green: lights up when 3.3 V is received form 1588PTP Mother Board |

# 4. Installing the Software on the Host Machine

This section outlines the process for installing the software onto the host machine. Before you begin, ensure that the system has an active internet connection.

To install the application on the host machine:

1. Extract the compressed software package to a folder using the *tar* command.
2. The installer downloads the required packages from the repository provided by Linux and Ubuntu.
3. Right-click the *installer.sh* file in the folder and change its permissions to *Executable*.

   **Note:** This can also be done using the *chmod* command.
4. Run the *installer.sh* using the command *./installer.sh.*
5. The installer installs the kernel, modules, services, and user interface on the system.
6. After the installation is completed with no errors, restart the system.
7. When the system starts, open the terminal (Ctrl + Alt + T) and run the application using the command *sudo lattice_ORAN_1588_Solution*.
8. When the application starts, it checks for the hardware. If hardware is found, the user can configure and run the clock. If hardware is not found, the user can only perform post-processing on previously saved data.

## 4.1. Wireshark Packet Verification

To verify the PTP packets:

1. Open the Wireshark application to capture Ethernet data from all available ports.
2. Capture PTP packets to verify the various fields and parameters that were set by the PTP packet generator.

# 5. IEEE 1588 PTP Overview

## 5.1. Theory of Operation

### 5.1.1. PTP Profiles

The IEEE 1588-2019 standard includes the concept of PTP profiles to describe the network parameters, allowed clock types, clock domain number, and others.

The Lattice ORAN solution stack supports the following profiles:

- IEEE 1588-2019 default profile
- ITU-T Telecom profile for frequency (G.8265.1)
- ITU-T Telecom profile for time with full timing support (G.8275.1)
- ITU-T Telecom profile for time with Partial timing support (G.8275.2)
- IEEE 802.1AS-(gPTP)

The Lattice ORAN solution stack conforms to the following timing characteristics:

- ITU-T G.8273: Framework of phase and time clocks
- ITU-T G.8273.2: Timing characteristics of telecom boundary clocks and telecom time slave clocks for use with full timing support from the network
- ITU-T G.8273.3: Timing characteristics of telecom transparent clocks for use with full timing support from the network
- ITU-T G.8273.4: Timing characteristics of telecom boundary clocks and telecom time slave clocks for use with partial timing support from the network
- ITU-T G.8262: Timing characteristics of synchronous equipment slave clock
- ITU-T G.8262.1: Timing characteristics of enhanced synchronous equipment slave clock

### 5.1.2. PTP Port Roles

- Master – The entity distributing time to slave ports.
- Slave – The device that synchronizes itself to the PTP master.

### 5.1.3. PTP Clock Types

The following clocks are defined in IEEE 1588 PTP:

- Ordinary Clock (OC)
  It only has one clock port. For an Ordinary Clock, a clock port may not necessarily correspond to a physical port. Ordinary clock can be GM to distribute time.
  - Master – this distributes PTP time to slaves.
  - Slave – this synchronizes PTP time with the master.
- Boundary Clock (BC)
  Boundary clock requires a minimum of two PTP ports. At least one port must be slave and others are master. The Boundary clock synchronizes its clock from Slave Port using PTP messages. The Master Port acts as master for the clocks connected on the Master Port.
- Transparent Clock (TC)
  A Transparent Clock assists in the delay measurement between a master and a slave by including a Correction Factor (CF) that tells the slave how much delay the Transparent Clock added. This in general applies to Layer 2 bridges, and a TC's clock ports correspond to physical interfaces.

Other clock types are defined as per ITU-T and IEEE profiles defined in PTP Profiles.

## 5.2. Software Design Overview

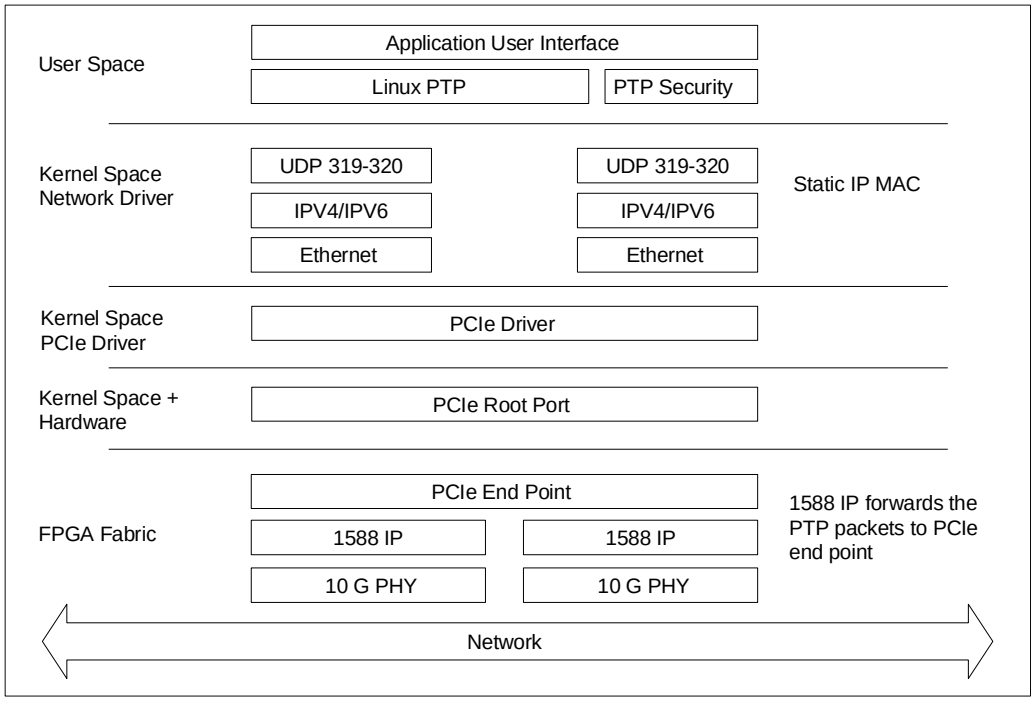


**Figure 5.1. Software Solution Overview**

### 5.2.1. User Space Application

- Lattice ORAN 1588 solution stack user interface to configure, run and monitor the clocks.
- linuxptp engine for the PTP messages and servo.
- PTP security, which implements security based on the integrated security processing conformant to Section 16.14.1 in IEEE 1588-2019.
- Configuration and Control modules to communicate/provide hardware settings to FPGA.

### 5.2.2. Kernel Space Drivers

- NIC driver with 2×10 G ports with TCP/IP protocol suite
- PTP hardware clock driver
- PCIe driver with ×4 Gen 2 support
- GNSS driver
- Supporting character drivers for debugging, configuration, and data transfer

# 6. IEEE 1588 PTP Solution Stack Application User Interface

This section describes the user interface for configuring, running, and monitoring the clocks. The steps for configuring the clocks are also provided.

## 6.1. Main Navigation Menu

The main navigation menu includes the following:

- *Home*: The application landing page (profile selection page)
- *Dashboard*: Data table showing the synchronization parameters
- *Data Plots*: Graph plots for the obtained data
- *Stats. Analysis*: Statistical plots for some of the key performance parameters
- *About*: General information, Application usage tips, and Glossary

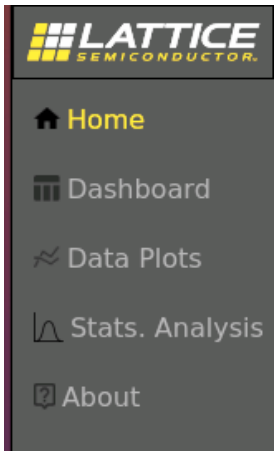


**Figure 6.1. Main Navigation Menu**

## 6.2. Getting Started – Home

The Home interface provides option for selecting/loading the configuration file, setting up the Profile and editing the configuration settings among others.

### 6.2.1. Configuration File Selection

To create/load a configuration file:

1. Under **Create/Load File**, select **New File** or **Load File**.
2. Enter the file name without spaces.
3. Click the **Apply** button.

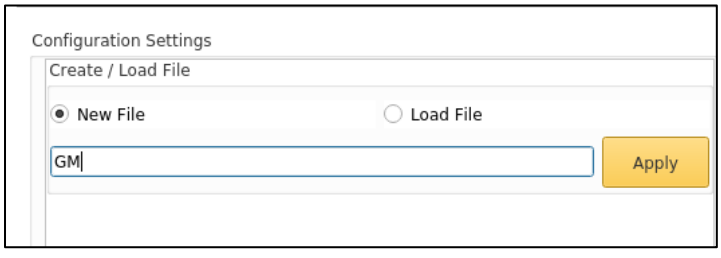


**Figure 6.2. Configuration File Selection**

### 6.2.2. Profile Options

To set up the profile, select the options available from the drop-down menu under:

- Profile
- Profile Clock
- IEEE 1588 Clock


**Figure 6.3. Profile Setup**

### 6.2.3. Configuration Settings

After selecting the required profile clocks and IEEE 1588 clock, a configuration setting is generated with the default values, which the user can edit if needed.

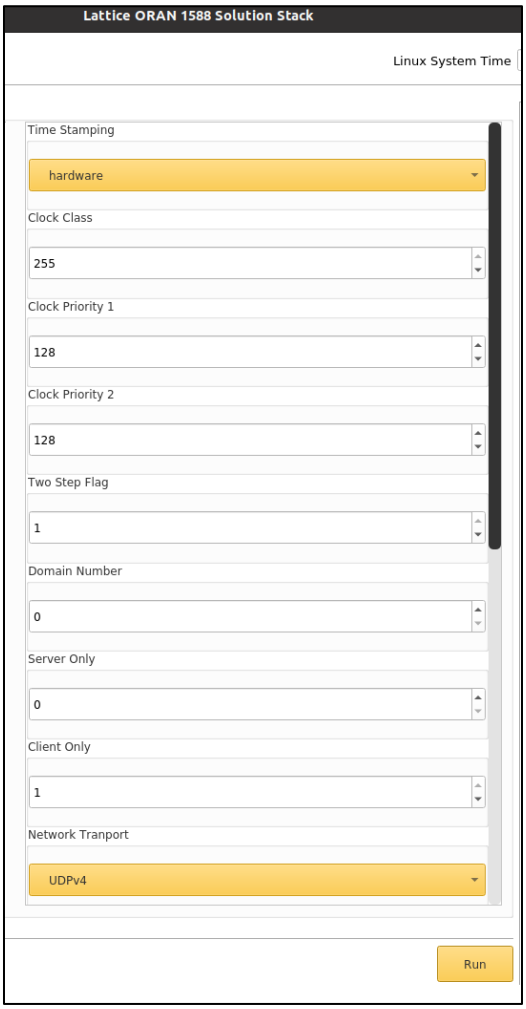


**Figure 6.4. Configuration Settings**

Once the user is done with editing the configuration settings, the user must save the configurations. All the configurations are saved in the */home/lattice/Profile_clocks/* folder. After the configuration is saved, the PTP engine can be started.

To start the PTP engine, click the *Run* button.

To stop the process, click the *Stop* button.

Once stopped, the user can only clear the previous configurations and set up a new configuration afresh.

To clear all the input fields, click on the *Clear* button.

To change the required configuration, click the *Stop* button first and then click the *Edit* button.


**Figure 6.5. Edit and Stop Buttons**

To save the inputs, click the *Save* button and then click *Run* to start the PTP engine.

To clear all the input fields, click the *Clear* button.


**Figure 6.6. Save, Clear, and Run Buttons**

### 6.2.4. VLAN Settings

VLAN has three modes:

- *Disable*: VLAN is disabled.
- *VLAN*: Sends single VLAN tag
- *QinQ*: Sends double VLAN tag

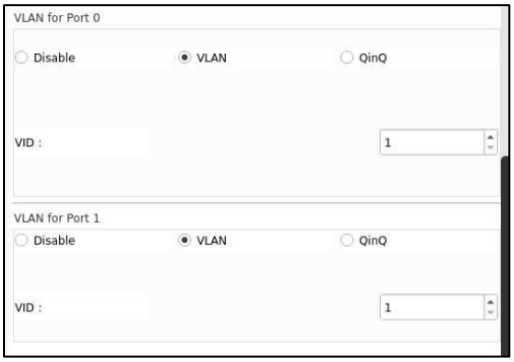


**Figure 6.7. VLAN Options**

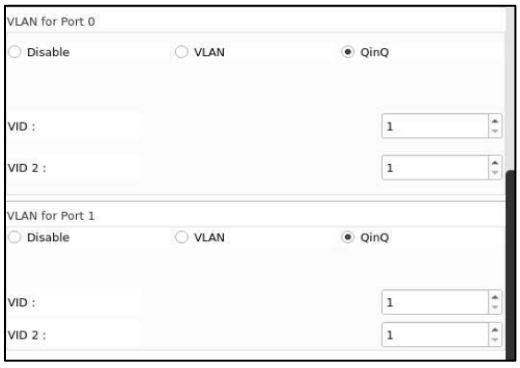

**Figure 6.8. QinQ Options**

### 6.2.5. ARP Settings

A few default ARP entries are added during the installation process. To use different IP and MAC addresses, the user can manually add the IP and MAC addresses in the *ARP Entries* section.

- Select Network: Network type IPv4 or IPv6.
- *IP*: IP address
- *MAC*: MAC address
- Add ARP
- ARP Table

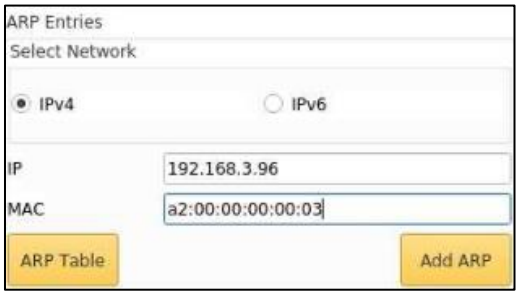


**Figure 6.9. ARP Entries for IPv4**


**Figure 6.10. ARP Entries for IPv6**

ARP is used only for unicast message transmission and supports only IPv4 and IPv6.

If using a tester, the tester's IP and MAC addresses must be entered manually in all the machines (nodes).

## 6.3. Dashboard

In the *Dashboard* interface, the data generated by the PTP engine can be viewed in tabular form.
If the PTP engine is running, the table is updated at an interval of 1 sec.

- *Load File*: Loads any previous data
- *Time Error PHC*: If the PHC clock is running, the data is displayed in this section.
- *Stop*: Stops the PTP engine
- *Save Data*: Saves the data

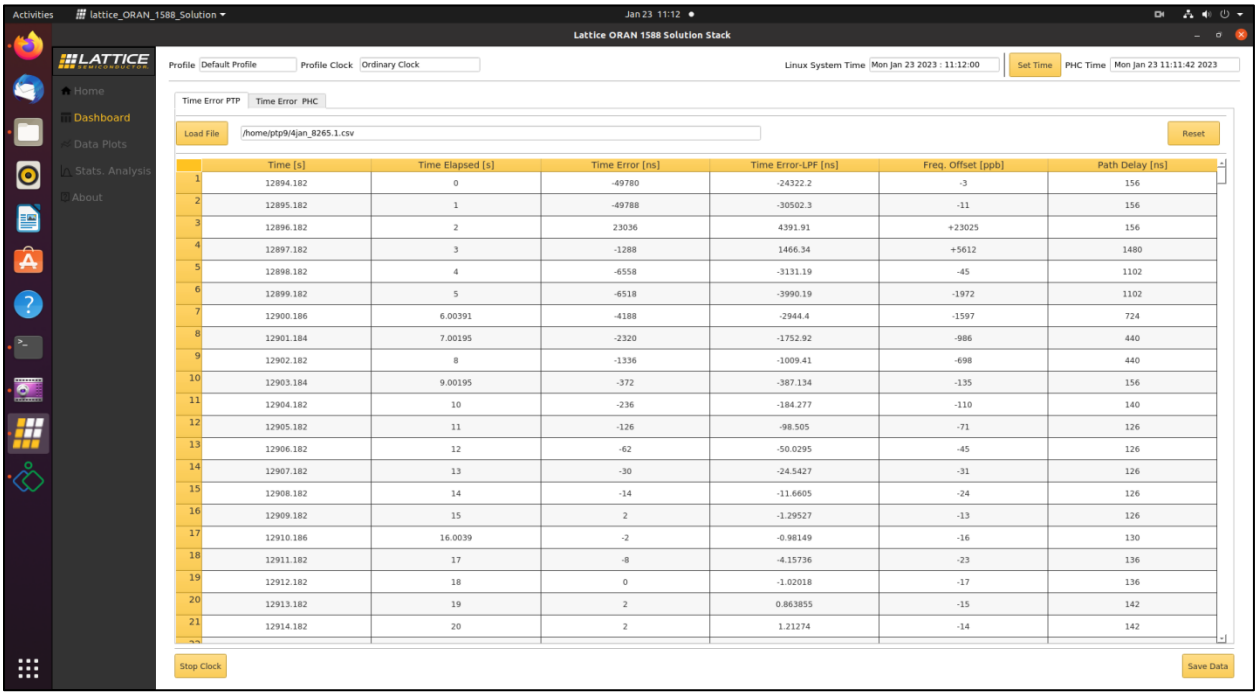


**Figure 6.11. Dashboard Table**

## 6.4. Data Plots

In the *Data Plots* interface, the *Time Error Vs Time Elapsed* graph is plotted using the data from the dashboard table.

Enter the required range using the *Start/End* fields and click ***Set Range***.

Click *Calculate* to show *Max |TE|* and *CTE* for the selected range.

Click *MTIE Plot* and *TDEV Plot* to plot graphs for the selected range.

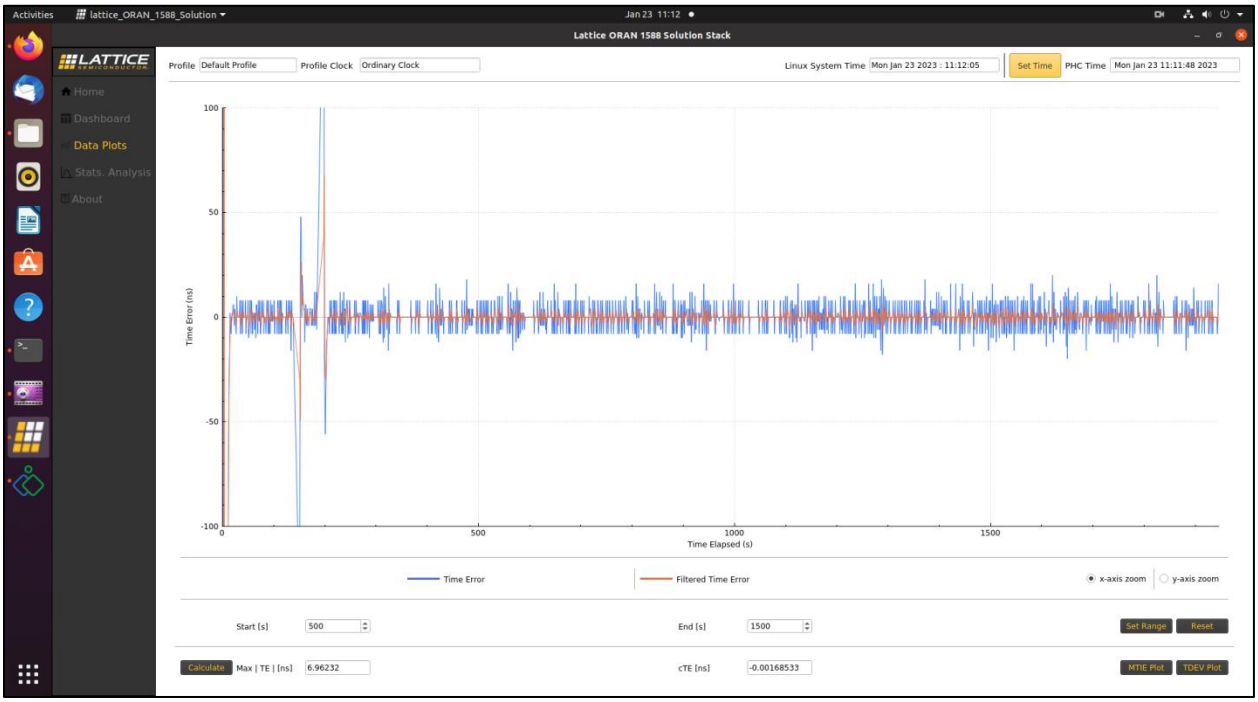


**Figure 6.12. Data Plots**

## 6.5. Stats. Analysis

The *Stats. Analysis* interface features four statistical plots:

- Time Error/Freq. Offset/Path Delay
- Histogram
- PDF of Histogram and PDF of Normal Distribution
- CDF of Histogram and CDF of Normal Distribution

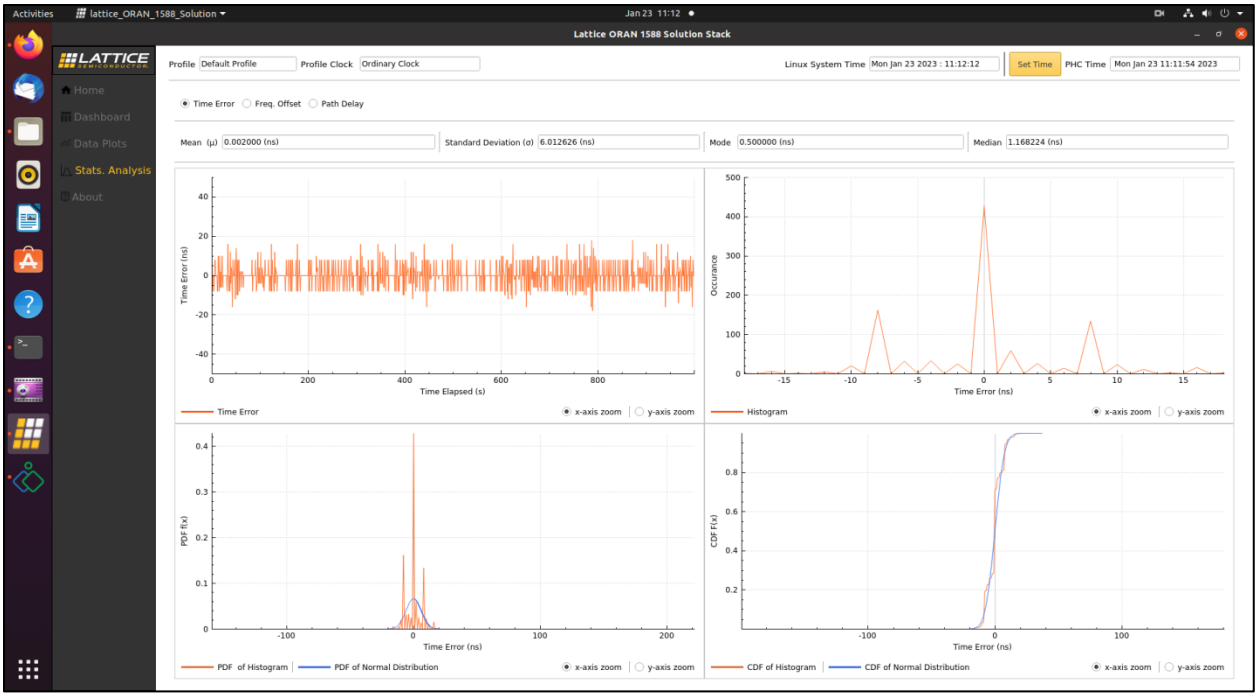


**Figure 6.13. Statistical Analysis Plots**

## 6.6. Status and Configuration Settings

The status and configuration settings are read back from the FPGA and displayed in the rightmost section of the *Home* interface.

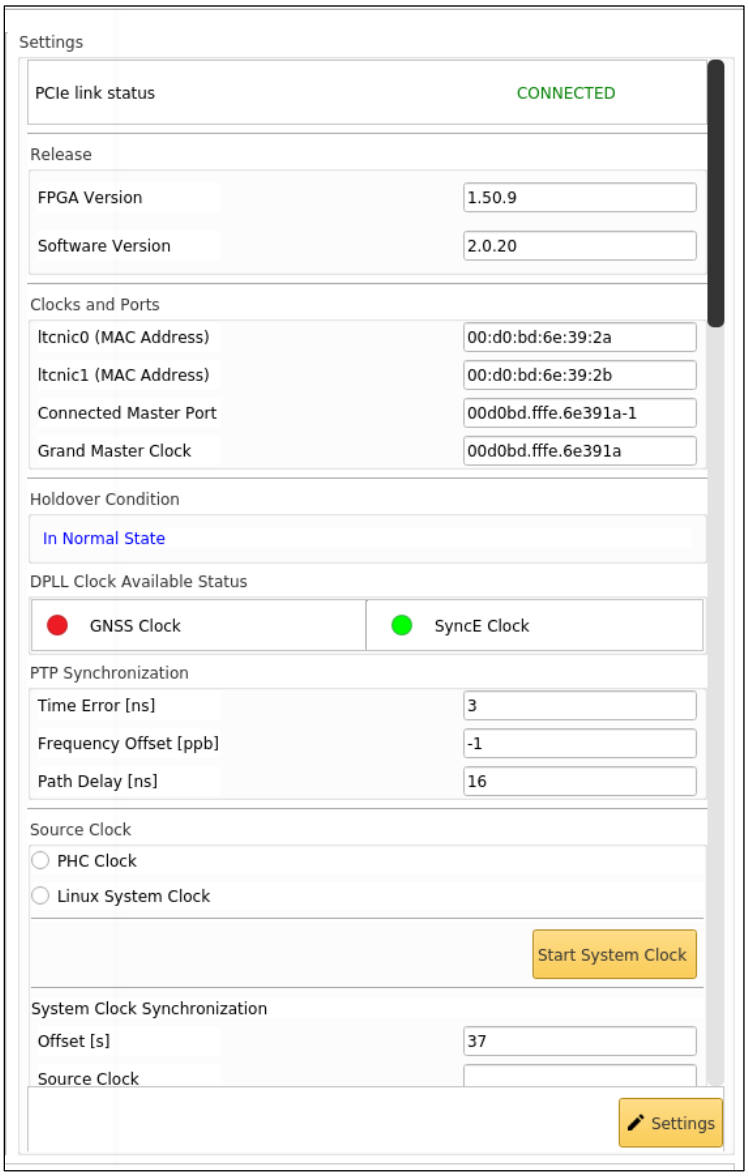


**Figure 6.14. Configuration Settings**

### 6.6.1. Configuration Settings

- *PCIe link status*: Shows the link status between the DUT and the Linux system.
- *Release*: Displays the FPGA Version and the Software Version.
- *Clocks and Ports*: Displays the *MAC Address* of both the ports. If the PTP engine is running, the *Connected Master Port* and *Grand Master Clock* identities are also displayed.


**Figure 6.15. Clocks and Ports**

- *PTP Synchronization*: If the PTP engine is running, this section shows the *Time-Error*, *Frequency-Offset*, and *Path Delay* data.


**Figure 6.16. PTP Synchronization**

- Source Clock: This section provides the option to synchronize the Linux system clock with the PHC (running in FPGA). Source Clock indicates the clock with which the other clock is synchronized.
- In the case of Grand Master with GNSS as clock source, the Linux system has the GNSS time. So, the Source clock should be Linux system clock. The PHC keeps synchronizing itself with the *Linux System Clock*.
- In the case of T-BC or T-TSC, the PHC should be the source clock. *Linux System Clock* keeps synchronizing itself with PHC.
- Clicking the *Start System Clock* starts the synchronization.
- The synchronization parameters for these clocks are displayed in the system clock synchronization section.
- *System Clock Synchronization*: This section shows the parameters for the PHC - Linux system clock synchronization. These are *Time Error*, *Frequency Offset*, and *Path Delay*.

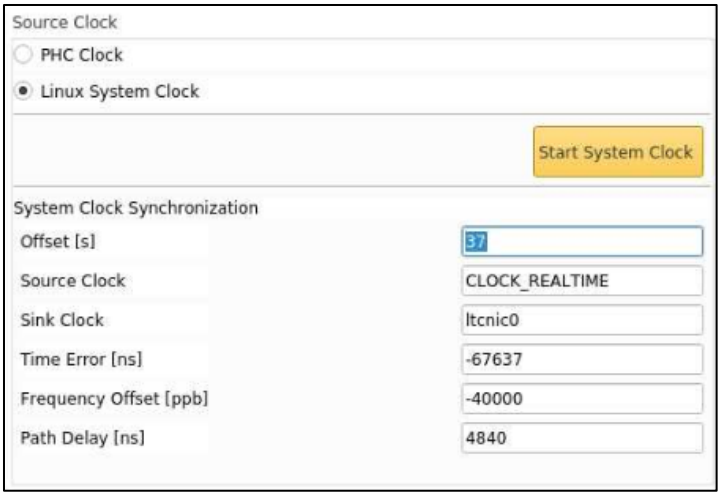


**Figure 6.17. System Clock Synchronization**

- *Port Statistics*: This section displays the number of received and transmitted packets of both the PTP and non-PTP traffic. A PTP node has two 10 G ports. PTP and non-PTP traffic at these ports in both RX and TX directions are displayed.

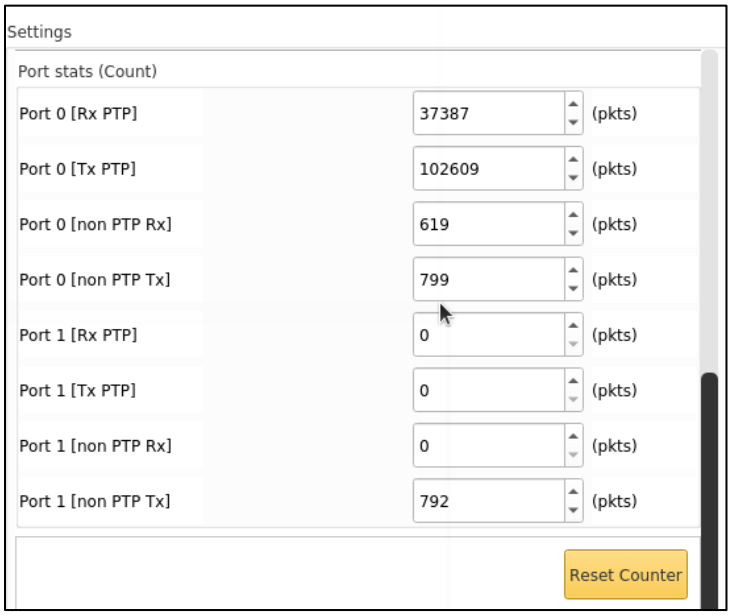


**Figure 6.18. Port Statistics**

- *Port Stats (Rate)*: This section shows the rate at which the packets of both the PTP and non-PTP traffic are received and transmitted.

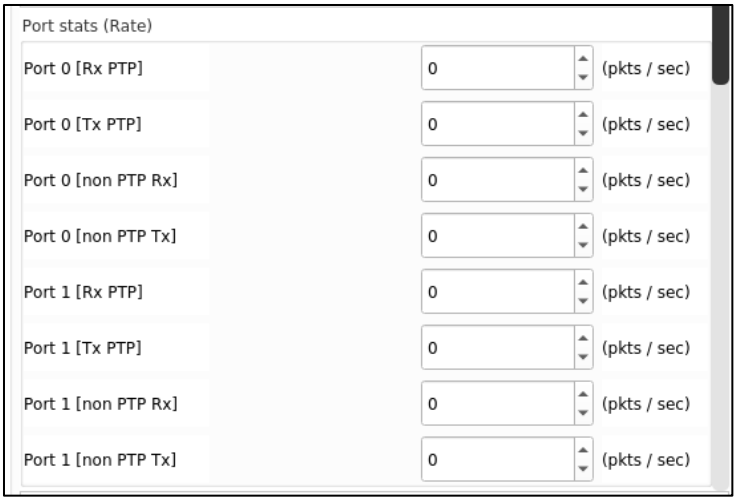


**Figure 6.19. Port Stats (Rate)**

- *Clock Type*: Displays the clock type configuration. Whether the clock is set to **One Step or Two Step**.


**Figure 6.20. Clock Type**

- *Message Transmission*: Displays the network layer used for the PTP transmission. Supports **L2, IPv4, IPv6**.

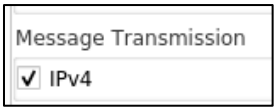


**Figure 6.21. Message Transmission**

- *TC Type*: Displays the configuration setting if the PTP node is set as a **TC**, **E2E TC**, **P2P TC**, or **Not set as TC**.

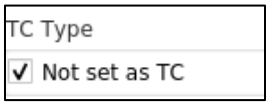


**Figure 6.22. TC Type**

### 6.6.2. Advanced Configuration Settings

There are a few advanced configuration settings that can be applied for the PTP node. These can be directly configured using the user interface in run time.

- Port Delay and 1pps Compensation
- DPLL Clock Source Selection
- GNSS Settings
- Traffic selection MUX

To edit these fields, click the *Edit* button, make the necessary modifications, and then click the *Update* button to apply the changes.

- Delay Compensation:
  - *Egress* – to compensate the Egress delay for the port.
  - *Ingress* – to compensate the Ingress delay for the port.
  - *pps*– to compensate phase error of the pps output w.r.t ToD.

To accurately synchronize the slave clock to the Grand Master, the clocks must be compensated with appropriate path delays. The Egress and Ingress delays are added to the total path delay. When compensated, these delays are excluded from the path delay. Then, the cable delay becomes the path delay and the same is displayed in the user interface. Upon changing the *pps* value, the clock's phase is change. The user interface shows the default values set for the PTP node. The user can edit these values if required.


**Figure 6.23. Delay Compensation**

- *GNSS*: For Grand Master application, GNSS can be used as the time reference. A GNSS module is present on the FMC board. This GNSS can be started or stopped using the enable /disable radio buttons.


**Figure 6.24. GNSS Settings**

- *DPLL Clock*: DPLL is used for jitter attenuation of the SyncE recovered clock. It provides the necessary clocks for the ToD counter and 10 G Ethernet. The clock source can be selected based on the user requirement.
- Clock Priority order is set to GNSS >> SyncE >> OCXO
  There are four input clock sources.
  - *Stratum 3E Ovenized Crystal Oscillator (OCXO)*: An onboard OCXO with 10MHz output can be set as the input clock for the DPLL. OCXO provides a stable clock and is primarily used for Grand Master Clock or Holdover scenario.
    **Note:** The default DPLL input clock source is *OCXO*.
  - *SyncE Port 0*: For ITU-T G.8275.1 profile, SyncE is used as frequency assist. To provide SyncE support, clock is recovered from the upstream port and provided to the downstream port. The recovered clock is fed to the DPLL for jitter attenuation. The selection of upstream and downstream ports is up to the user. The recovered clocks from both the ports are connected to the DPLL. When SyncE Port 0 is set as the clock source, the recovered clock from Port 0 is considered as the input for DPLL to generate the required output clocks.

**Note:** When the user selects ***ITU-T G.8275.1***, SyncE is manually set depending upon the upstream/downstream port configuration.

- *SyncE Port 1*: When SyncE Port 1 is set as the clock source, the recovered clock from Port 1 is considered as the input for DPLL to generate the required output clocks.
- *GNSS*: GNSS also provides 8 KHz-10 MHz clock on its TimePulse output. This clock can be set as the input clock to DPLL to generate the required output clocks. In Grand Master Clock scenario, this clock can be used as the reference clock to generate the required output clocks. To configure the TimePulse clock output, detailed steps are provided in the GNSS section.

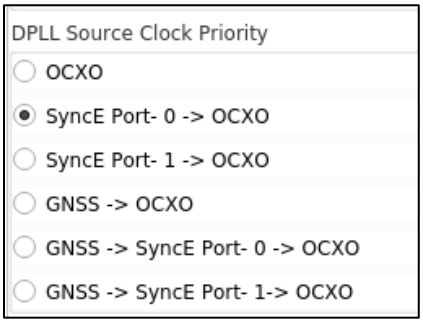


**Figure 6.25. DPLL Clock Source**

**Table 6.1. Clock Source Description**

| Clock Source Options | Clock Source Description |
|---|---|
| OCXO | GNSS clock and SyncE clock are disabled in FPGA logic.<br>DPLL locks to OCXO |
| SyncE Port0 >> OCXO | GNSS clock is disabled<br>DPLL locks to SyncE recovered clock (from Port 0)<br>If SyncE is lost, DPLL falls back to OCXO |
| SyncE Port1 >> OCXO | GNSS clock is disabled<br>DPLL locks to SyncE recovered clock (from Port 1)<br>If SyncE is lost, DPLL falls back to OCXO |
| GNSS >> SyncE Port0 >> OCXO | DPLL locks to GNSS clock (8 MHz)<br>SyncE recovered clock (from Port 0) and OCXO are available for fall back<br>If GNSS clock is lost, SyncE will be the fallback option<br>If SyncE is also lost, DPLL locks to OCXO reference |
| GNSS >> SyncE Port1 >> OCXO | DPLL locks to GNSS clock (8 MHz)<br>SyncE recovered clock (from Port 1) and OCXO are available for fall back<br>If GNSS clock is lost, SyncE will be the fallback option<br>If SyncE is also lost, DPLL locks to OCXO reference |
| GNSS >> OCXO | DPLL locks to GNSS clock (8 MHz)<br>If GNSS is lost, DPLL locks to OCXO |

- When the clock moves from *Normal State* to *Holdover State* due to loss of PTP, it is displayed in the user interface, as shown in Figure 6.26 and Figure 6.27.


**Figure 6.26. Holdover Status Indicator - Normal State**


**Figure 6.27. Holdover Status Indicator – Holdover State**

- The clock source to which DPLL is locked is displayed in the user interface, as shown in Figure 6.28.
- When GNSS and SyncE are lost, OCXO is always the fallback option.
- This indication also serves the *Alarm* requirement on clock switchover during noise tolerance tests.


**Figure 6.28. DPLL Clock Alarm**

- *Traffic at Port*: To mix the PTP and non-PTP traffic in the transmit direction, a traffic mixer block is provided that can mix non-PTP traffic with the PTP traffic. The non-PTP traffic can be routed from Port 0 or Port 1 or User Logic. The mixer block helps emulate network scenarios where PTP and non-PTP traffic coexist.
  The PTP traffic always exists in the transmit path. To add non-PTP traffic, the options below are provided for each of the ports.
  - *PTP traffic (PCIe)*: To transmit only PTP traffic received on the PCIe port.
  - *PTP traffic (PCIe) + Port (0) non-PTP traffic*: To add non-PTP traffic received on Port (0) to the PTP traffic.
  - *PTP traffic (PCIe) + Port (1) non-PTP traffic*: To add non-PTP traffic received on Port (1) to the PTP traffic.
  - *PTP traffic (PCIe) + User traffic*: To add the non-PTP traffic from the User logic to the PTP traffic.

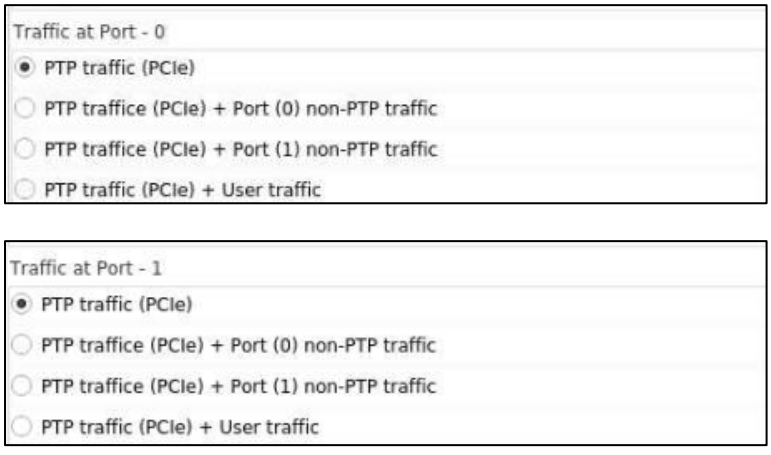


**Figure 6.29. Traffic Settings for Port 0 and Port 1**

# 7. GNSS

## 7.1. GNSS Configurations (Read/Write)

The GNNS module in the 1588PTP Daughter Board is LEA-M8T from u-blox. It is a GNSS positioning module featuring the high-performance u-blox M8 positioning engine and easy to integrate and combine exceptional positioning performance with highly flexible power, design, and connectivity options.

For setting up the GM clock, GNSS can be used as the source of clock and UTC time. GNSS module can be configured using the u-center application provided by u-blox. The configuration can be loaded into the non-volatile memory. These are auto loaded after every power cycle.

The u-center can be used to create configuration file of a u-blox GNSS positioning module and store it as an ASCII text file containing hexadecimal records. Such a file can be loaded to or retrieved from the u-blox GNSS module.

In u-center Tools menu, select GNSS configuration to open the GNSS configuration dialog box.

The following functions are available:

- Specify the name of a new configuration file to store current configuration from the u-blox GNSS module.
- Specify the name of an existing configuration file and load this configuration into the u-blox GNSS module.
- A flag can be set to force storing the configuration into a battery-backed RAM (BBR) or flash, applicable for u-blox 5 to u-blox 8/M8 only.

## 7.2. Reading/Writing Configuration Files

To read and write configuration files:

1. Connect the PTP hardware to a PC running the u-center application.

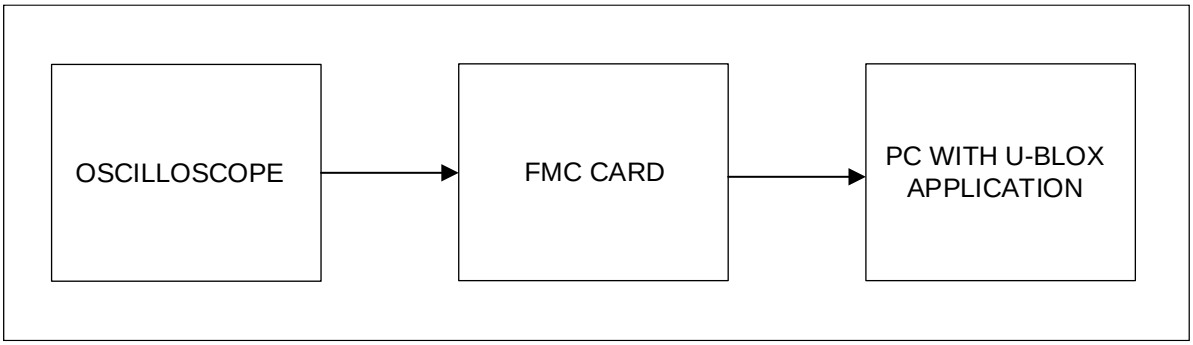


**Figure 7.1. GNSS Configuration Setup**

2. Power ON the 1588PTP Mother Board using either an external 12V adapter or PCIe cable. The 1588PTP Daughter Board can be powered from 1588PTP Mother Board through the FMC connector by toggling the power selection switch J5.
3. Connect the 1588PTP Daughter Board to the PC through USB Type-A to Type B mini-Cable at port J2.

4. In the u-center application, select **Receiver > Connection** and the appropriate COM port to access the GNSS module.

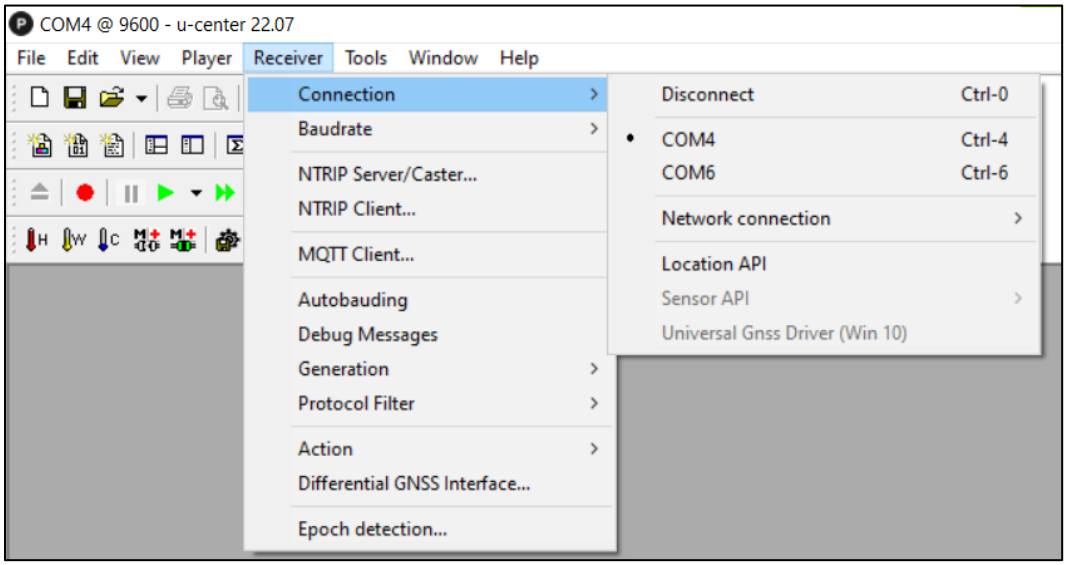


**Figure 7.2. COM Port Selection**

5. Select **Tools > Receiver Configuration**.

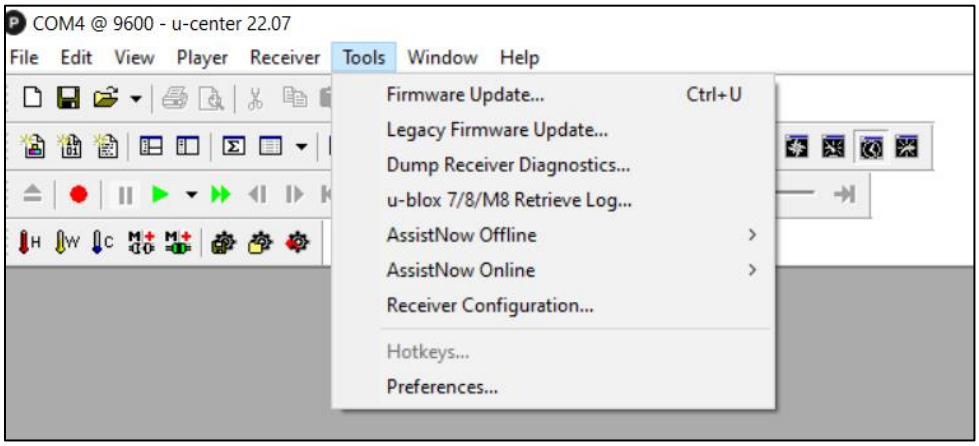


**Figure 7.3. Tools Selection**

The **Load/Save Receiver Configuration** GNSS configuration dialog box opens.

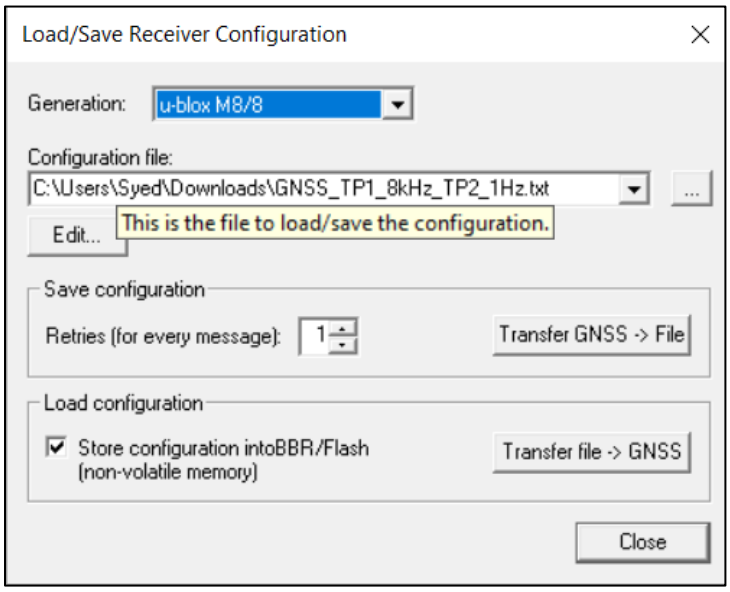


**Figure 7.4. GNSS Configurations**

6. In **Generation**, select **u-blox M8/8**.

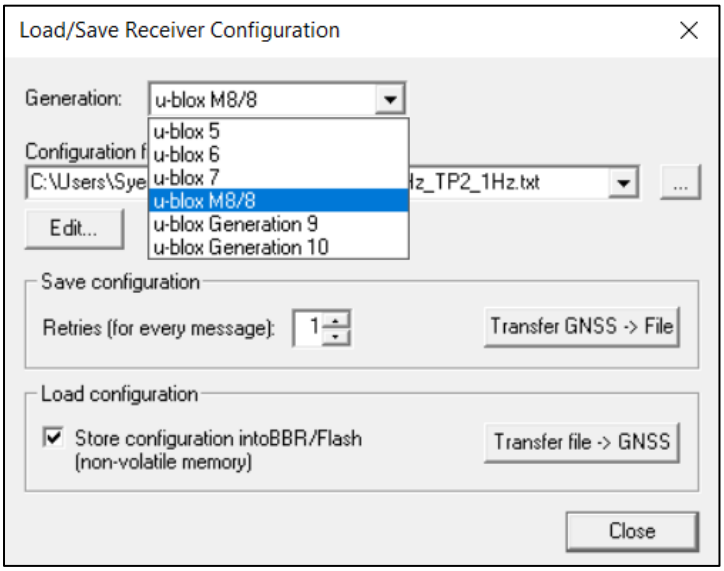


**Figure 7.5. GNSS Generation Selection**

7. In **Configuration file**, load the GNSS configuration file from the right path.

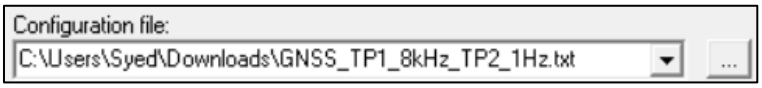


**Figure 7.6. GNSS Configuration File Path**

**Note:** Make sure to reset the GNSS in the hardware.

8. Click **Transfer file-> GNSS**.

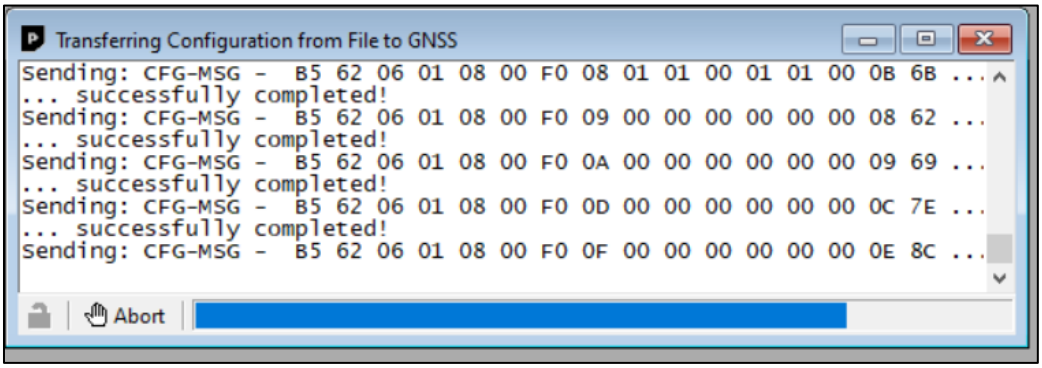


**Figure 7.7. File Transfer Status**

**Note:** Make sure to check the configuration version details.

9. Once the configuration file is uploaded, a Successfully Completed message is displayed and GNSS configuration window automatically closes.
10. To read an existing configuration file, select the name of the file, and click the **Transfer file > GNSS** button. The GNSS configuration window closes. The progress window shows the status of the operation and the closes after a successful transfer.
11. To write a new configuration file, click **Transfer GNSS > File**. The GNSS configuration window closes. The progress window shows the configurations being pulled and stored into a local file in ASCII format.
12. Select the **Store configuration into BBR/Flash** checkbox if the parameters need to be stored into the device's non-volatile memory (BBR/Flash). This option is applicable for u-blox 5 to u- blox 8/M8 generation receivers.

The user can abort the transfer by clicking the **Abort** button. It is not possible to close the window unless the transfer is completed or aborted.

It is not recommended to read/write configuration while the u-blox GNSS device is in sleep mode.

# 8. Secure IEEE 1588 PTP

The Lattice ORAN solution stack implements added security based on the integrated security processing conformant to Section 16.14.1 in IEEE 1588-2019. The security feature provides source authentication, message integrity, and replay attack protection for PTP messages. Security implements an authentication TLV which contains an Integrity Check Value (ICV). The ICV can be used to authenticate the PTP message sender on the fly. ICV implements HMAC-SHA256-128 algorithm. In this algorithm, the output is truncated to 128 bits. The key size is the size of hash value produced by SHA-256 (256 bits).

Secure IEEE 1588 PTP performs the following:

- Generates Authentication TLV (Type Length Value) that carries the information required for cryptographic verification.
- Generates and verifies ICV.
- ICV is computed as HMAC-SHA256 truncated to 128 bits.
- Supports two-step clocks. (One-step clock is not supported).

  **Note:** Works only when secure PTP is enabled at all the nodes.

# 9. IEEE 1588 PTP Node Setup Example

## 9.1. IEEE 1588 Default Profile

### 9.1.1. Profile Overview

This standard defines the PTP protocol that provides precise synchronization of clocks in packet-based networked systems. The Precision Time Protocol (PTP) generates a master–slave relationship among the PTP Instances in the system. The clocks in all PTP Instances ultimately derive their time from a clock known as the *Grand Master Clock*.

The standard allows multicast communication, unicast communication, or both. The standard specifies requirements for mapping the protocol to specific network implementations and defines such mappings, including User Datagram Protocol (UDP)/Internet Protocol (IP versions 4 and 6), and layer-2 IEEE 802.3 Ethernet.

### 9.1.2. Setup Objective

To demonstrate time synchronization between four PTP nodes: GM (Grand Master), BC (Boundary Clock), TC (Transparent Clock), and OC (Ordinary Clock). All the clocks are configured as two-step clocks.

### 9.1.3. Setup

The setup has four PTP nodes connected as shown in Figure 9.1.

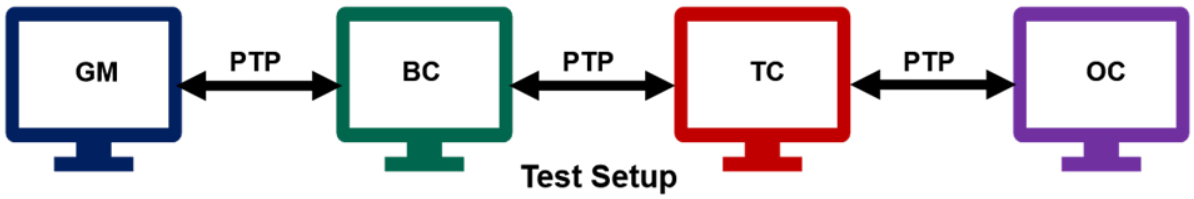


**Figure 9.1. PTP Setup for IEEE 1588 Default Profile**

To perform time synchronization between four PTP nodes:

1. Open the Lattice ORAN 1588 solution application.
2. In **Configurations Settings**, under **Profile**, select **Default Profile**.

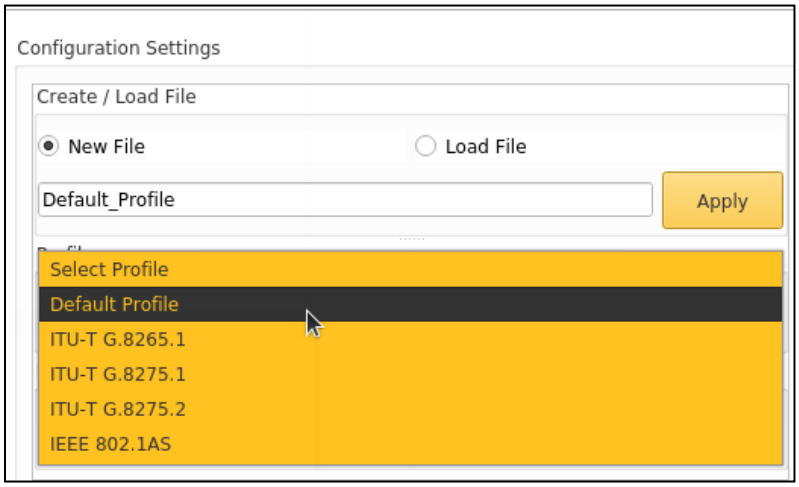


**Figure 9.2. Profile Selection**

3. Under **Profile Clock**, select any option (**Ordinary Clock**, **Boundary Clock**, **Grand Master Clock**, or **Transparent Clock**).

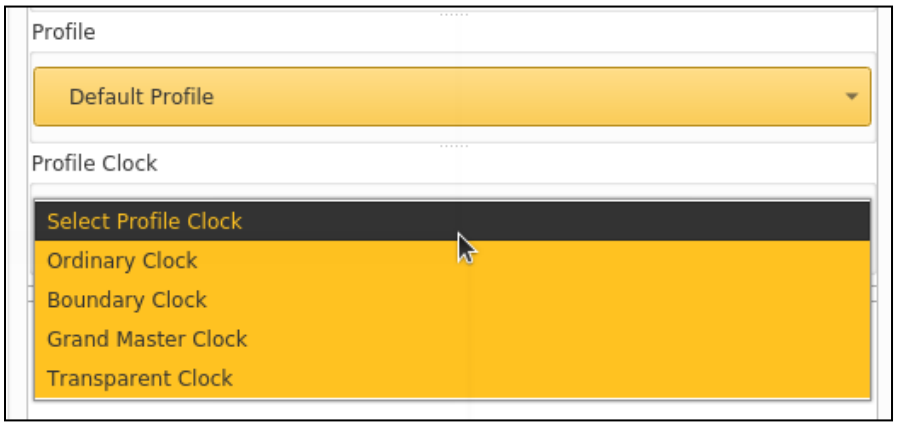


**Figure 9.3. Profile Clock Selection**

4. Select the **IEEE 1588 Clock**.


**Figure 9.4. IEEE 1588 Clock Selection**

5. Run the PTP4L process by clicking on the **Run** button.

### 9.1.4. Profile Settings

The profile settings are provided in this section.

**Table 9.1. Grand Master Clock (GM) Setting**

| Parameter | Value | Comments |
|---|---|---|
| [global] | — | — |
| verbose | 0 | Print messages to the standard output if enabled. The default is 0 (disabled) |
| time_stamping | hardware | Hardware timestamping |
| clock_type | OC | Clock type as per 1588 standard |
| twoStepFlag | 0 | 1-step clock enabled |
| domainNumber | 0 | Domain Number of the clock |
| serverOnly | 1 | PTP Node set to packet master |
| network_transport | UDPv4 | Message transmission type is UDP |
| logSyncInterval | 0 | Sync interval of $2^{-0}$ i.e. 1 sync message per second |
| logMinDelayReqInterval | 0 | Minimum value of Delay request interval = $2^{-0}$ i.e. 1 delay request per second |
| logAnnounceInterval | 1 | Announce interval of $2^{-1}$ i.e. 1 Announce message every 2 seconds |
| [ltcnic0] | — | — |
| delay_mechanism | E2E | Select the delay mechanism. Possible values are E2E, P2P and Auto. The default is E2E |

**Table 9.2. Ordinary Clock (OC) Setting**

| Parameter | Value | Comments |
|---|---|---|
| [global] | — | — |
| verbose | 0 | Print messages to the standard output if enabled. The default is 0 (disabled) |
| time_stamping | Hardware | Hardware timestamping |
| clock_type | OC | Clock type as per 1588 standard |
| twoStepFlag | 0 | 1-step clock enabled |
| clockClass | 255 | The OC which can only become slave with clockClass equal to 255 |
| domainNumber | 0 | Domain number of the clock |
| network_transport | UDPv4 | Message transmission type is UDP |
| logSyncInterval | 0 | Sync interval of $2^{-0}$ i.e. 1 sync message per second |
| logMinDelayReqInterval | 0 | Minimum value of Delay request interval = $2^{-0}$ i.e. 1 delay request per second |
| logAnnounceInterval | 1 | Announce interval of $2^{-1}$ i.e. 1 Announce message every 2 seconds |
| [ltcni0] | — | — |
| delay_mechanism | E2E | Select the delay mechanism. Possible values are E2E, P2P and Auto. The default is E2E |

**Table 9.3. Boundary Clock (BC) Setting**

| Parameter | Value | Comments |
|---|---|---|
| [global] | — | — |
| verbose | 0 | Print messages to the standard output if enabled. The default is 0 (disabled) |
| time_stamping | hardware | Hardware timestamping |
| clock_type | BC | Clock type as per 1588 standard |
| twoStepFlag | 1 | 1-step clock enabled |
| domainNumber | 0 | Domain Number of the clock |
| logSyncInterval | 0 | Sync interval of $2^{-0}$ i.e. 1 sync message per second |
| logAnnounceInterval | 1 | Announce interval of $2^{-1}$ i.e. 1 Announce message every 2 seconds |
| logMinDelayReqInterval | 0 | Minimum value of Delay request interval = $2^{-0}$ i.e. 1 delay request per second |
| network_transport | UDPv4 | Message transmission type is UDP |
| [ltcnic0] | — | — |
| boundary_clock_jbod | 1 | Just a bunch of devices. The PTP node takes this node and synchronizes the PHC clock, if it is a slave. |
| delay_mechanism | E2E | Select the delay mechanism. Possible values are E2E, P2P and Auto. The default is E2E. |
| [ltcnic1] | — | — |
| boundary_clock_jbod | 1 | Just a bunch of devices. The PTP node takes this node and synchronizes the PHC clock, if it is a slave. |
| delay_mechanism | E2E | Select the delay mechanism. Possible values are E2E, P2P and Auto. The default is E2E. |

**Table 9.4. Transparent Clock (TC) Setting**

| Parameter | Value | Comments |
|---|---|---|
| [global] | — | — |
| verbose | 0 | Print messages to the standard output if enabled. The default is 0 (disabled) |
| time_stamping | hardware | Hardware timestamping |
| clock_type | E2E_TC | Clock type as per 1588 standard |
| twoStepFlag | 0 | 1-step clock enabled |
| domainNumber | 0 | Domain Number of the clock |
| logAnnounceInterval | 1 | Announce interval of 2-1 i.e. 1 Announce message every 2 second |
| logSyncInterval | 0 | Sync interval of 2-0 i.e. 1 sync message per second |
| logMinDelayReqInterval | 0 | Minimum value of Delay request interval = 2-0 i.e. 1 delay request per second |
| free_running | 1 | The clock source of PHC is free running OCXO if it is the best master |
| network_transport | UDPv4 | Message transmission type is UDP |
| [ltcnic0] | — | — |
| delay_mechanism | E2E | Select the delay mechanism. Possible values are E2E, P2P and Auto. The default is E2E |
| [ltcnic1] | — | — |
| delay_mechanism | E2E | Select the delay mechanism. Possible values are E2E, P2P and Auto. The default is E2E |

### 9.1.5. Wireshark Snapshot

Wireshark snapshots are shown below Sync message, Follow-up and Delay-Resp message are shown below.

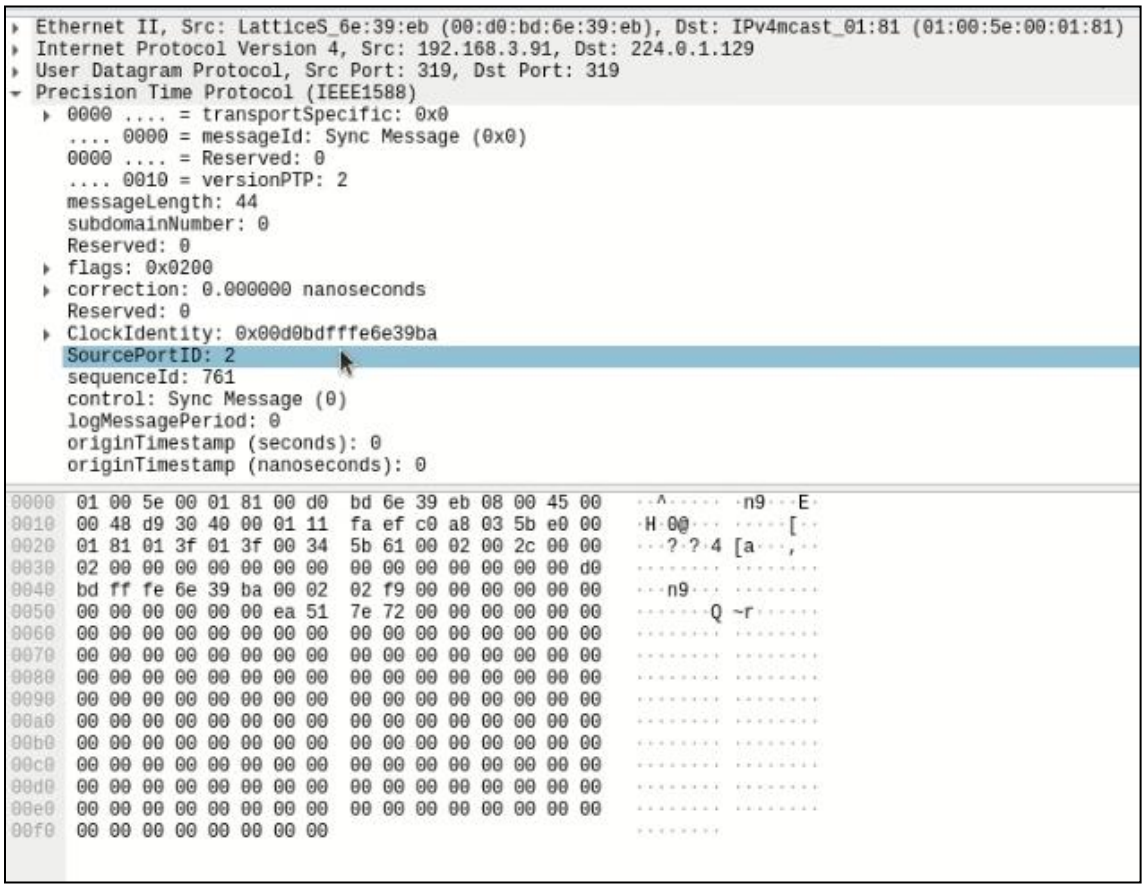


**Figure 9.5. Sync Message in IEEE 1588 Default Profile**

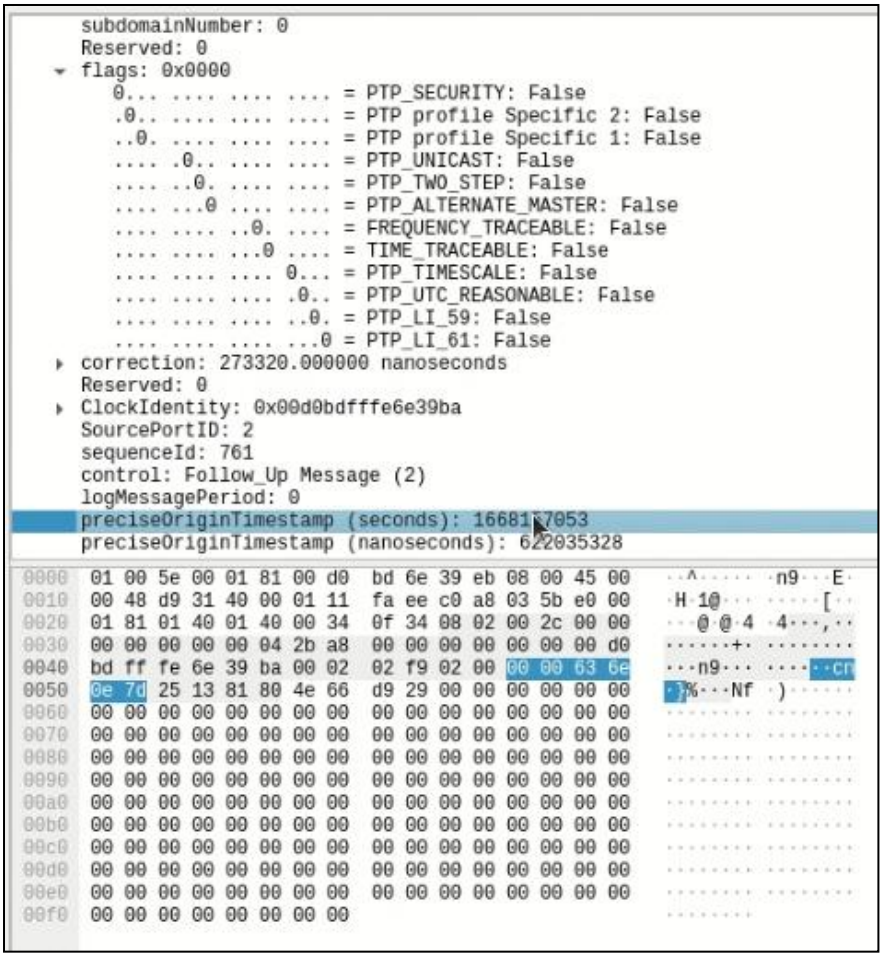


**Figure 9.6. Follow Up Message in IEEE 1588 Default Profile**

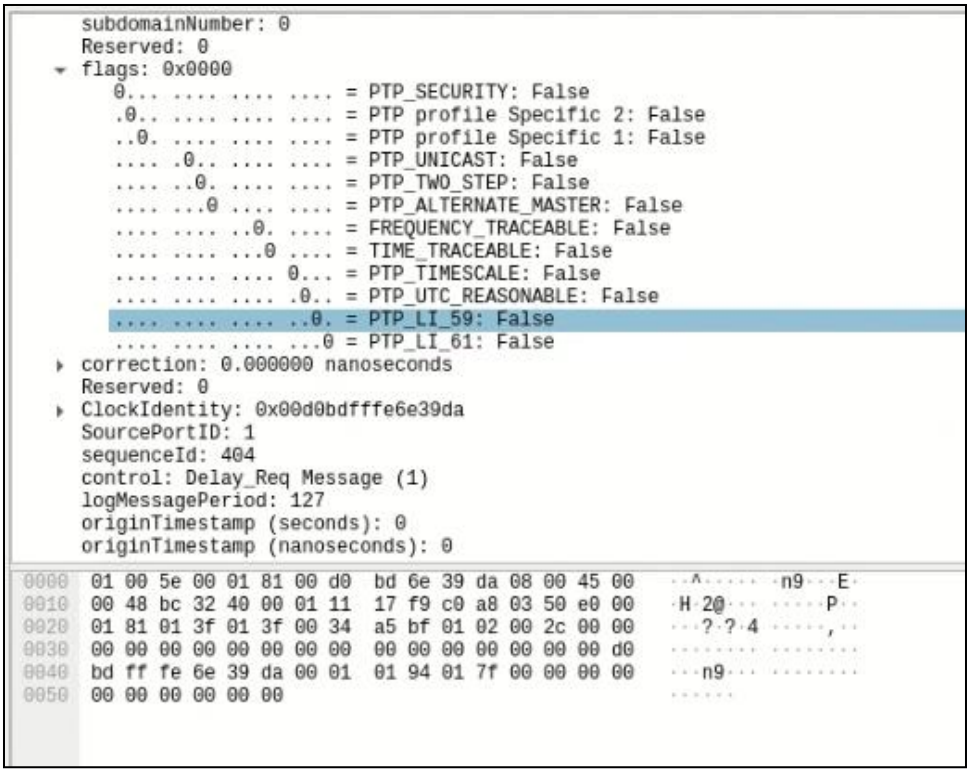


**Figure 9.7. Delay-Req Message**

Table 9.5 shows a summary of all the required power supplies.

**Table 9.5. CertusPro-NX FPGA Power Supplies**

| Supply | Voltage (Nominal Value[2]) | Description |
|---|---|---|
| $V_{CC}$ | 1.2 V | FPGA core power supply |
| $V_{CCGPLL}$ | 1.2 V | General Purpose PLL Supply Voltage. Should be isolated from excessive noise. |
| $V_{CCAUX25VPP}$ | 2.5 V | Auxiliary Supply Voltage for Bank 1, 2 and NVCM programming. |
| $V_{CCIO[2, 1, 0]}$ | 1.2 V to 3.3 V | I/O Driver Supply Voltage for Bank 0, 1, or 2. Each bank has its own $V_{CCIO}$ supply: $V_{CCIO0}$ is used in conjunction with pins dedicated and shared with device configuration. |
| $V_{CC\_DPHYx}$[1] | 1.2 V | Digital Supply Voltage for D-PHY. Should be isolated from excessive noise. |
| $V_{CCA\_DPHYx}$[1] | 1.2 V | Analog Supply Voltage for D-PHY. Should be isolated and from excessive noise. |
| $V_{CCPLL\_DPHYx}$[1] | 1.2 V | PLL Supply voltage for D-PHY. Should be isolated and *clean* from excessive noise. |
| $V_{CCMU\_DPHYx}$[1] | 1.2 V | $V_{CC\_DPHY1}$, $V_{CCA\_DPHY1}$ and $V_{CCPLL\_DPHY1}$ ganged together in the WLCSP36 package. Should be isolated from excessive noise. |

**Notes**:
1. X denotes bank number.
2. Refer to CertusPro-NX Family Data Sheet (FPGA-DS-02086) for recommended minimum and maximum values.

# References


- IEEE Std 1588-2019, “IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems”
- ITU-T G.8265.1, “Precision time protocol telecom profile for frequency synchronization”, June 2021
- ITU-T G.8275.1, “Precision time protocol telecom profile for phase/time synchronization with full timing support from the network”, March 2020
- ITU-T G.8275.2, “Precision time protocol telecom profile for phase/time synchronization with partial timing support from the network”, March 2020
- IEEE Std 802.1AS-2020. “Timing and Synchronization for Time-Sensitive Application”
- ITU-T G.8273, “Framework of phase and time clocks”, March 2018
- ITU-T G.8273.2, “Timing characteristics of telecom boundary clocks and telecom time slave clocks for use with full timing support from the network”, October 2020
- ITU-T G.8273.3, “Timing characteristics of telecom transparent clocks for use with full timing support from the network”, October 2020
- ITU-T G.8273.4, “Timing characteristics of telecom boundary clocks and telecom time slave clocks for use with partial timing support from the network”, March 2020
- ITU-T G.8262, “Timing characteristics of synchronous equipment slave clock”, November 2018
- ITU-T G.8262.1, “Timing characteristics of enhanced synchronous equipment slave clock”, November 2022
- Lattice ORAN web page
- Calnex Solutions, https://www.calnexsol.com/en/product-detail/1295-paragon-neo-4
- Lattice 5G ORAN Solution Stack 1.1 : Secure IEEE 1588 Precision Timing Protocol (PTP) – *NDA Only*, (FPGA-RD-02275).
- Bringing Security to 5G ORAN Deployments
- Lattice Insights for Lattice Semiconductor training courses and learning plans

# Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at https://www.latticesemi.com/Support/AnswerDatabase.

# Revision History

**Revision 1.1, August 2023**

| Section | Change Summary |
|---|---|
| All | General update: Renamed boards to 1588PTP Mother Board and 1588PTP Daughter Board. |
| Introduction | Renamed boards to 1588PTP Mother Board and 1588PTP Daughter Board. |
| Hardware and Software Requirements | • Renamed boards to 1588PTP Mother Board and 1588PTP Daughter Board.<br>• Removed Kernel 5.10.154 (custom Build) Deb package from Software Requirements subsection. |
| Hardware Features and Setup | • Renamed boards to 1588PTP Mother Board and 1588PTP Daughter Board.<br>• Updated feature to *2× SerDes channels extended to BOARD TO BOARD connector*.<br>• Updated Table 3.17. Clock Sources.<br>• Modified the details for 161.1328 MHz and 161.1328 MHz clock frequencies.<br>• Modified footnote 1. |
| Installing the Software | Modified the procedure for installing the application to the host machine. |
| IEEE 1588 PTP Solution Stack Application User Interface | • Added information on clearing all input fields or previous configurations and setting up a new configuration.<br>• Updated Figure 6.5. Edit and Stop Buttons.<br>• Updated Figure 6.14. Configuration Settings.<br>• Update the Advanced Configuration Settings subsection.<br>  • Added bullet item Clock Priority order is set to GNSS >> SyncE >> OCXO.<br>  • Updated Figure 6.25. DPLL Clock Source.<br>  • Added Table 6.1. Clock Source Description.<br>  • Added information on clock holdover state and DPLL clock.<br>  • Added Figure 6.26. Holdover Status Indicator - Normal State; Figure 6.27. Holdover Status Indicator – Holdover State; and Figure 6.28. DPLL Clock Alarm. |
| GNSS | Renamed boards to 1588PTP Mother Board and 1588PTP Daughter Board. |
| References | Removed *FPGA Design and Implementation of Secure IEEE 1588 Precision Timing Protocol for ORAN and 5G New Radio Applications* and added *Lattice Insights*. |

**Revision 1.0, June 2023**

| Section | Change Summary |
|---|---|
| All | Initial release. |


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