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FPGA Design and Implementation of Secure IEEE 1588 Precision Timing Protocol for ORAN and 5G New Radio Applications

IEEE 1588 PTP

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***Abstract*— The 5G Open Radio Access Network (O-RAN) concept is changing the landscape of cellular and mobile networks for 5G New Radio (NR) deployments. O-RAN consists of three units; Radio Unit (RU), Distributed Unit (DU), and Centralized Unit (CU). For the three units to communicate and function together, a timing and synchronization source is required. IEEE 1588 Precision Timing Protocol (PTP) provides the mechanism for synchronizing the distributed clock in a distributed system. As critical as tight synchronization is needed, it is also an attack target to bring the whole O-RAN units down by compromising their synchronization. Therefore, there is a growing need for a hardware-security solution for protecting this critical network function. In this paper, we present Lattice advanced solution to the design and interface of the IEEE 1588 PTP using FPGA for timing and synchronizing the RU, DU, and CU. This solution goes further by securing the IEEE 1588 through mutual authentication and making it resistant to the attacks by nefarious actors. This unique secure synchronization solution is designed to be used for 5G Radio Equipment (RE) such as the RU and Radio Equipment Controller (REC) such as the CU and DU. The secure IEEE 1588 PTP is implemented using Lattice advanced FPGA solution and supports different configuration of the IEEE 1588 such as Ordinary Clock (OC), Boundary Clock (BC), and Transparent Clock (TC). It also supports different ITU profiles for wireless networking such as ITU G8265.1, ITU G8275.1, and ITU G8275.2. It is then protected by "Lattice Secure the Wire™" solution where encryption and mutual authentication are used to implement secure synchronization. We present how the FPGA solution securely achieves frequency, phase, and timing synchronization and achieves an accuracy of average time error of less than 10ns.**

Keywords*— *1588, 5G, ORAN, TSN, SyncE, Frequency, Phase, Time

I. INTRODUCTION

IEEE 1588 precision time protocol (PTP) is an essential networking technology used to synchronize clocks throughout a distributed system. Originally developed in 2002, the protocol's recent version is the IEEE 1588v2-2019 which is the most recent specification released by IEEE.

IEEE 1588 provides a single source of timing to distributed units and acts as an alternative to using GPS clocks on endpoint devices, which may not have easy access to radios or satellite signals. A packet-based, bidirectional communication protocol, IEEE 1588 precisely synchronizes distributed clocks in Ethernet and IP-based networks with nanosecond accuracy. The protocol is widely used for timing synchronization in 5G and O-RAN cellular networks, data centers, industrial process control, audio-video networks, smart energy distribution, industrial IoT networking, and time-sensitive services such as autonomous driving and financial trading.

IEEE 1588 comes with other extensions called profiles and released by ITU [2-5]. These profiles extend the functionalities of IEEE 1588 to cover telecommunication equipment synchronization, supports time sensitive networks (TSN), and deliver time, frequency, and phase synchronization.

Implementing the IEEE 1588 protocol in real-time networking applications and on hardware, such as Field Programmable Gate Array (FPGA), can be a complex task. In this paper, we introduce the design and implementation of IEEE 1588v2 using Lattice FPGA targeted for 5G and O-RAN applications. The IEEE 1588 hardware solution is ideal for deployments such as 5G/6G infrastructure, data centers, Clouds, and next-generation automotive systems. Accurate and reliable time synchronization underpins the stable operations of time-sensitive networks.

O-RAN consists of three major components: the remote radio unit (RU), distribution unit (DU), and central unit (CU). The RU serves as the consumer's access point to the network. The DU acts as the connection to the centralized unit (CU) and the mobile core. The three units need precise synchronization to avoid data packet loss and network interruptions when communicating between them. IEEE 1588 is used to synchronize transmitted and received signals. While time-based synchronization is becoming more common in the network, frequency-based Synchronous Ethernet (SyncE) and phase-based synchronization remain an underlying technology critical to high-precision timing

applications such as the physical layer of the radio units in 5G/6G systems. Additionally, both PTP and SyncE are robust alternatives to GPS synchronization. Depending on the network architecture, O-RAN networks can use PTP, SyncE, or both for synchronization.

The hardware platform for Lattice ORAN™ 1588 solution stack is designed to demonstrate PTP protocol and ITU profiles as per IEEE and ITU specifications [1-5].

II. IEEE 1588 PTP Solution Stack and Hardware Platform

A. Lattice IEEE 1588 Solution

Lattice IEEE 1588 solution is part of Lattice ORAN stack and is a compliant design and implementation of IEEE standards and ITU profiles for 1588 PTP which is fully embedded on Lattice FPGA. IEEE 1588v2 standard includes the concept of PTP profiles to describe the network parameters, allowed clock types, and configurations. The IEEE 1588 solution stack supports the following [1-5]:

- IEEE 1588v2-2019 default profile
- ITU-T G.8265.1 telecom profile for frequency synchronization
- ITU-T G.8275.1 telecom profile for phase and time synchronization with full timing support
- ITU-T G.8275.2 telecom profile for phase and time synchronization with partial timing support
- IEEE 802.1AS-(gPTP) for Time Sensitive network (TSN)

The solution stack realizes a compliant design and implementation of the procedures, messages, events, and configurations as specified in [1-5] embedded on FPGA.

B. CertusPro-NX™ FPGA Cards

The FPGA platform for Lattice ORAN 1588 solution stack is designed to fully embed the PTP protocol as per IEEE 1588 and ITU standards. The hardware consists of two cards namely PTP carrier card and PTP FPGA Mezzanine Card (FMC). The first card is powered by Lattice CertusPro-NX FPGA.

CertusPro-NX device is a low-power general purpose FPGA which can be used in a wide range of applications across multiple markets and is optimized for bridging and processing needs in edge applications.

The PTP FMC allows the user to generate multiple clock sources for the carrier card from external and on-board clock sources. The FMC card is pluggable to the carrier card through an FMC connector.

C. Lattice 1588 PTP Carrier Card

The Lattice 1588 PTP carrier card is shown in Figure 1. It features the CertusPro-NX FPGA and has the following on-boards peripherals:

- CertusPro-NX FPGA (LFCPNX-100)
- PCIe Gen 2 with x4 lanes
- 2 x SFP 10G Ethernet
- 2 x SFP 1G Ethernet
- 2 x SerDes channels extended to FMC Connector
- On-board 512 Mb Serial Peripheral Interface (SPI) Boot flash, with quad read feature
- USB-B, UART and I2C ports
- Seven Segment Display, five-input DIP switch, 8 status LEDs for customer purposes
- HPC FMC
- Lattice Radiant® software programming [6]

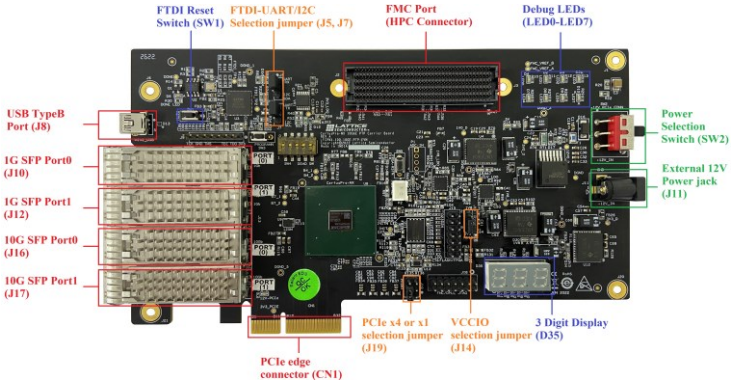

Fig. 1. Lattice 1588 PTP carrier card.

D. IEEE 1588 PTP Firmware

The USB port on the PTP carrier card is used to flash the firmware to the card as shown in Figure 2.

The carrier card has a built-in download controller for programming the CertusPro-NX device. It uses an FT2232H Future Technology Devices International (FTDI) part to convert USB to JTAG. The USB is connected to PC with Lattice Radiant Programmer tool installed and the latter is used to flash and download firmware to the card.

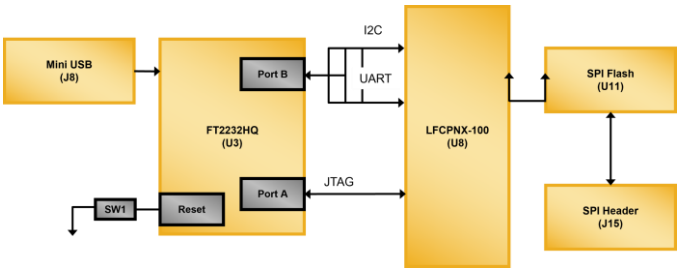

Fig. 2. Lattice 1588 PTP carrier card serial interface.

E. Lattice FMC

The PTP FMC, as shown in Figure 3, consists of a DPLL to generate clock sources which are used by FPGA on carrier card as reference clocks. DPLL is fed with four inputs: one from GNSS, one from Ovenized Crystal Oscillator (OXCO), one from external frequency (through SMA port), and one from FPGA (SyncE clock). The FMC card has multiple ports to output Pulse Per Second (PPS) and Time of Day (ToD) clocks. The PTP FMC has the following on-board peripherals:

- Network clock synchronizer
- Stratum 3E OCXO
- GNSS timing module
- 2 x RJ48 ports for ToD/PPS In & Out
- 2 x SMA ports for DPLL Frequency In & Out

F. Carrier and FMC Integration

The FMC is plugged on top of the carrier card through the FMC connector. Two supporting mounting holes are provided on both carrier and FMC cards for mechanical support. Figure 4 shows the assembly of FMC to the carrier card.

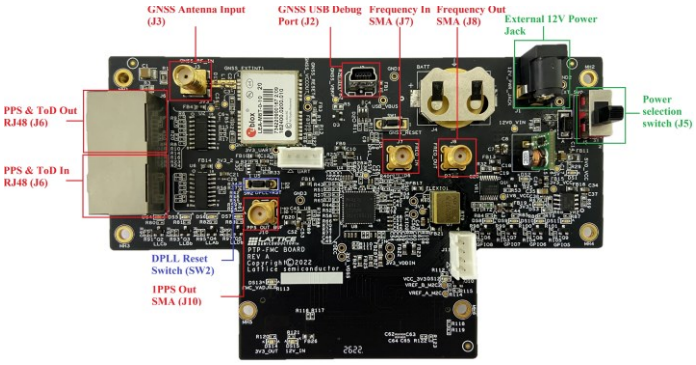

Fig. 3. Lattice 1588 PTP FMC card.

III. FPGA AND SOFTWARE ARCHITECTURE

A. CertusPro-NX FPGA Architecture

The IEEE 1588 solution stack is an embedded solution that runs on CertusPro-NX FPGA and implement the IEEE 1588 protocol and ITU profiles [1-5] in Verilog/RTL codes. The soft and hard IPs implemented on the FPGA are shown in Figure 5.

The FPGA solution, which is abstracted in Figure 5, has the following hardware blocks:

- 2 x 10G Ethernet PCS/PMA IP cores
- 2 x 10G Ethernet MAC IP cores
- 2 x 10G Ethernet SFP Ports
- 2 x Time stamping unit
- 1 x Time of Day (ToD) counter/PTP Hardware Clock (PHC)
- Network synchronizer which is used to generate clocks for PTP and SyncE
- I2C interface for network synchronizer
- GNSS timing module
- UART for receiving data from GNSS timing module
- PCIe x4 interface
- RISC-V

The time stamping unit block is used to detect PTP and non PTP packets, parse PTP packet, timestamp event message, and do the CRC for 1-step PTP messages. TSU contains the following hardware blocks:

- Rx Packet Parser, Rx time-stamp buffer, and Rx residence timestamp buffer
- Tx Packet Parser, Tx time-stamp buffer, and time-stamp inserter
- Correction Field Inserter (CFI) and CRC correction

B. Software Architecture

The IEEE 1588 solution stack can be run as either fully embedded stack on FPGA or can be split where the lower-stack of IEEE 1588 runs on FPGA and higher-stack runs on a Linux Ubuntu PC. In the latter configuration, the higher-stack software is shown in Figure 6.

The software is communicating with the FPGA over PCIe bus interface. IEEE 1588 protocol is running on UDP on top of either IPv4 or IPv6. Finally, there is a GUI application used to configure and monitor the IEEE 1588 stack. Due to lack of space, reader is referred to technical documents on Lattice website [6] for further details.

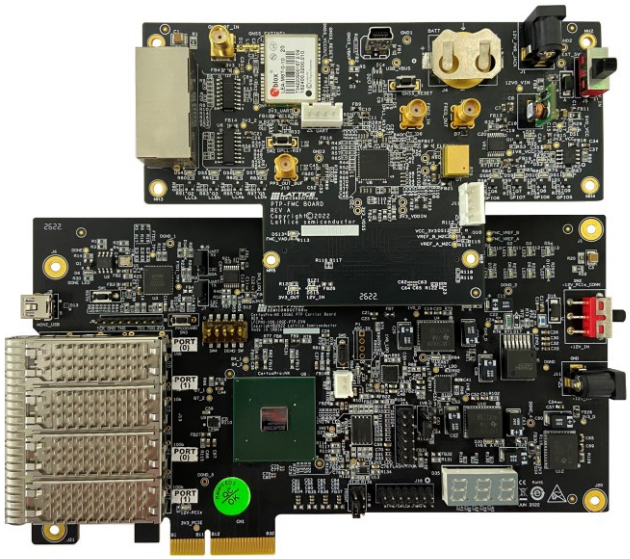

Fig. 4. Lattice 1588 PTP assembled carrier and FMC cards.

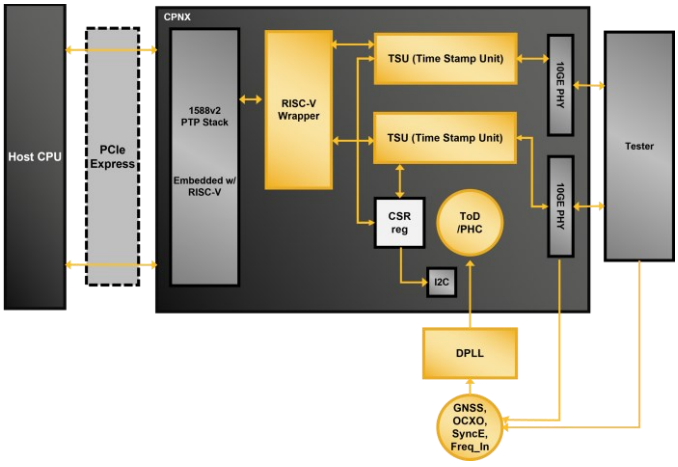

Fig. 5. Lattice embedded IEEE 1588 PTP FPGA hardware blocks (for illustrative purposes).

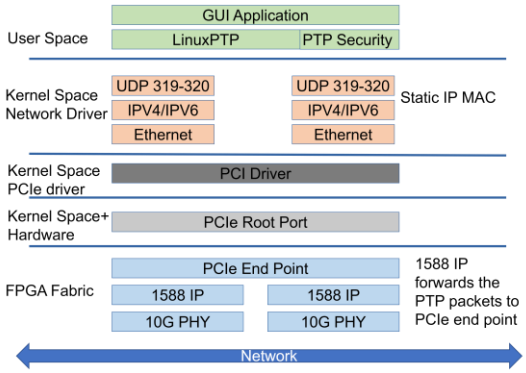

Fig. 6. Lattice 1588 PTP software architecture.

C. IEEE 1588 Security

The IEEE 1588 solution stack implements security based on the integrated security processing conformant to Section 16.14.1 in [1] and as illustrated in Figure 6. The security feature provides source authentication, message integrity, and replay attack protection for PTP messages. Security implements an authentication TLV which contains an Integrity Check Value (ICV). The ICV can be used to authenticate the PTP message sender on the fly. ICV implements HMAC-SHA256-128 algorithm. In this algorithm, the output is truncated to 128 bits. The key size is the size of hash value produced by SHA-256 (256 bits). A key management and distribution procedure is implemented where a shared secret is made available at all PTP nodes to generate and verify the ICV. In future release of the IEEE 1588 solution stack, it integrates with MACSEC [6].

IV. Performance Results

Test bed of the IEEE 1588 solution stack is setup which runs different type of clocks and IEEE 1588 default profiles in and ITU-T profiles. Test and measurement of the IEEE 1588 PTP solution stack is done using Paragon-neo Calnex tester [7]. Results of the 2-way time error using 2-step IEEE 1588 default profile is shown in Figure 7.

Lattice ORAN solution stack for IEEE 1588 is a timing and synchronization platform with class C accuracy. Class C accuracy achieves less than 30ns of the maximum absolute 2-way time error and less than of 10ns of the average 2-way time error. 2-way time error plot shown in Figure 7 illustrates that Lattice ORAN stack achieves a maximum absolute 2-way time error of 9ns (Min value) and an average 2-way time error of -1.8 ns. The filtered 2-way time error is shown in Figure 8, and it shows that the Lattice ORAN stack achieves a maximum absolute 2-way time error (filtered) of 2.2ns (Min value) and an average 2-way time error (filtered) of -0.7ns.

For the ITU-T G.8275.1 profile, the Class C performance result is shown in Figure 9. In Figure 9, it shows that the maximum dynamic 2-way time error (low pass-filtered) is at about 3ns which is much less the target Class C dynamic timing error of 10ns.

The test results show that the Lattice ORAN IEEE 1588 solution stack meets Class C accuracy and empirically achieves better than the target Class C accuracy.

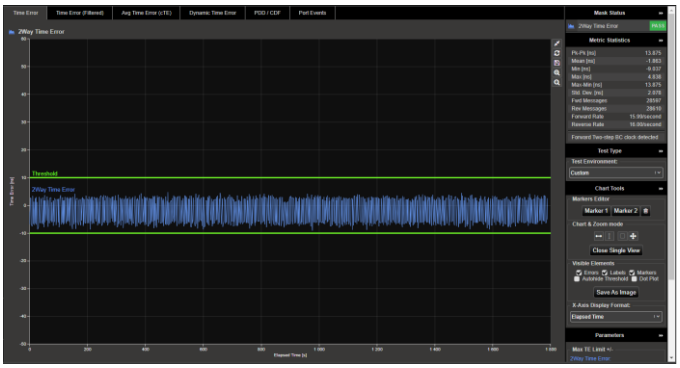

Fig. 7. Plot of 2-way time error versus elapsed time.

Fig. 8. Plot of 2-way time error (filtered) versus elapsed time.

Fig. 9. Plot of 2-way dynamic time error (filtered) against class C target.

References

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